Resume

Cécile Braunstein

Born 19.10.1979 in Paris (France)
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Current Situation

I'm holding a position as Associate Professor in the System on chip (SOC) department of the computer science laboratory of Paris 6 (LIP6) in the Pierre et Marie Curie University (UPMC). I'm a member of the ALSOC team (architecture and software for embedded system on chip). I'm also teaching in the Paris 6 engineering school Polytech'Paris UPMC.
Research interests: Hardware design, SoC, protocol converter, formal verification, Model Checking, BDD, SAT, Abstraction, CEGAR.

Education

2003 - 2007 **PhD thesis in computer science** (Pierre et Marie Curie University) with high honors, under the supervision of Emmanuelle Encrenaz, in the System on Chip team. Dissertation titled: **"Incremental Design Process, Verification of Hardware Components and Abstraction Method for the Verification of System on Chip"**
Committee in charge:
Prof. Dominique Borionne (TIMA Grenoble France), Prof. Béatrice Bérard (LAMSADE Paris France), Prof. Alix Munier-Kordon (LIP6 Paris France), Prof. Dr.-Ing Hans Eveking (TU-Darmstadt Germany) Prof. Alain Greiner (LIP6 Paris France)

2002 - 2003 **M.Sc. in Computer Science**(Pierre et Marie Curie University) specialization in system on chip with high honors

2001 - 2002 **B.Sc. in Computer Science**(Pierre et Marie Curie University) with high honors

Academic Career

2008 - **Associate Professor** in LIP6-SOC of Pierre et Marie Curie University

2007 - 2008 **Post-doctoral fellow** University of Bremen, Germany, in the AGRA group of Prof. Rolf Drechsler

2006 - 2007 **Temporary assistant professor**, Pierre et Marie Curie University

2003 - 2006 **Teaching assistant** Pierre et Marie Curie University

Teaching

Lectures

2009 - 2012 Computer Architecture

2008 - 2011 C++ programming

2008 - 2011 Programming initiation with VBA

Tutorials and exercises

2009 - 2012 Embedded system project

2009 - 2012 Computer Architecture

2008 - 2012 C++ programming

2008 - 2011 Programming initiation with VBA

2009 - 2010 Formal method model checking

2006 - 2007 Architecture and representation

2004 - 2007 C programming

2004 - 2007 Computer science project

Collaborations and Projects

2012 - 2013 **EquIPA**: Equivalence checking for Analog IP, collaboration with the CIAN team of the LIP6.

2009 - 2010 **DeAR**: Debug with Abstraction-Refinement, collaboration with AGRA group of Bremen University.

2008 - 2011 **FME3**: Enhancing the Evaluation of Error consequences using Formal Method, collaboration with the TIMA from Grenoble and the team MOVE of LIP6.

Responsibilities

Since 2011 **Coordinator** of the 1st year Electronic/Computer science engineering study of Polytech'Paris-UPMC.

Since 2010 **Elected delegate** of the teachers in the educational council of Polytech'Paris-UPMC.

Since 2010 **Webpage management** for ALSOC Team.

Since 2009 **Seminar organizing** for the interns seminars of the SoC department.

Languages

French (native), English (fluent), German (basis B1)

Selected Publications

The following documents can be downloaded at
http://www-soc.lip6.fr/users/cecilebraunstein/research

[1] Souheib Baarir, Cécile Braunstein, Emmanuelle Encrenaz, Jean-Michel Ilié, Isabelle Mounier, Denis Poitrenaud, and Sana Younes. Feasibility analysis for robustness quantification by symbolic model checking. *Formal Methods in System Design*, 39(2):165–184, 2011.

[2] Souheib Baarir, Cécile Braunstein, Emmanuelle Encrenaz, Jean-Michel Ilié, Tun Li, Isabelle Mounier, Denis Poitrenaud, and Sana Younes. Quantifying robustness by symbolic model checking. In *1st Hardware Verification Workshop (CAV workshop)*, pages 1–12, July 2010.

[3] Souheib Baarir, Cécile Braunstein, Ranaud Clavel, Emmanuelle Encrenaz, Jean-Michel Ilié, Régis Leveugle, Isabelle Mounier, Laurence Pierre, and Denis Poitrenaud. Complementary formal approaches for dependability analysis. In *Proc. 24th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, pages 331–339. IEEE Computer Society, October 2009.

[4] A. Suelflow, G. Fey, C. Braunstein, U. Kuehne, and R. Drechsler. Increasing the accuracy of sat-based debugging. In *DATE Design Automation and Test in Europe Conference*, pages 1326–1331, 2009.

[5] C. Braunstein and E. Encrenaz. Ctl-property transformations along an incremental design process. *International Journal on Software Tools for Technology Transfer (STTT)*, 9 1:77–88, 2007.

[6] C. Braunstein and E. Encrenaz. Using ctl formulae as component abstraction in a design and verification flow. In *ACSD IEEE International Conference on Application of Concurrency to System Design*, page NONE, 2007.

[7] C. Braunstein and E. Encrenaz. Formalizing the incremental design and verification process of a pipelined protocol converter. In *RSP International Workshop on Rapid System Prototyping*, pages 103–109, 2006.

[8] C. Braunstein and E. Encrenaz. A further step in the incremental design process: Incorporation of an increment specification. In *LPAR IEEE International Conference on Logic for Programming Artificial Intelligence and Reasoning*, page NONE, 2006.

[9] C. Braunstein and E. Encrenaz. Ctl-property transformations along an incremental design process. In *AVOCS International Workshop on Automated Verification of Critical Systems*, pages 263–278, 2004.