Haralampos-G. Stratigopoulos

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Personal Data

Born in Athens, Greece, November 1978

Academic Degrees

Habilitation à Diriger des Recherches, Institut polytechnique de Grenoble, France, Jul '15

Ph.D., Yale University, USA, Dec '06

M.S. in Electrical Engineering, Yale University, USA, May '03

Diploma in Electrical and Computer Engineering, National Technical University of Athens, Greece, Jul '01

Professional Position

Researcher with the French National Center for Scientific Research (CNRS) since Oct '07:

- Université Grenoble Alpes, CNRS, Laboratoire Techniques de l'Informatique et de la Microélectronique pour l'Architecture des systèmes intégrés (TIMA), Grenoble, France, Oct '07 - May '15
- Sorbonne Universités, Université Pierre et Marie Curie (Université Paris 6), CNRS, Laboratoire d'Informatique de Paris 6 (LIP6), Paris, France, May '15 - present

Research Interests

Design-for-test, built-in self-test, self-healing, on-line test, diagnosis and failure analysis techniques for analog, mixed-signal, and RF circuits and systems, hardware security and trust, machine learning applications in electronic design automation, computer-aided design, brain-inspired computing

Sponsored Research

Marie Curie MIRG-CT-2007-209653, "Machine Learning-Based Test Solutions for Reliable Mixed-Signal/RF Integrated Devices," Nov '07 - '11

Catrene CT-302 TOETS, "Towards One European Test Solution," Apr '09 - '12

Research contract with Infiniscale, “Calcul de haut rendement global,” Jun ’11 - ’12

ANR SACSO, “Solutions for the self-Adaptation of Communicating Systems in Operation,” Jan ’12 - ’15

ENIAC No. 296112-2 ELESIS , “European Library-based flow of Embedded Silicon test Instruments,” Apr ’12 - ’15

CNRS/INS2I Projet P-SoC , “Self-healing and self-adapting RF circuits,” 2013

Research contract with ams AG, “Adaptive Test of Semiconductor Devices,” May ’16 - ’17

Penta HADES, “Hierarchy-Aware and secure embedded test infrastructure for Dependability and performance Enhancement of integrated Systems,” Apr ’17-’20

ANR EDITSoC, “Electrical Diagnosis for IoT SoCs in automotive,” Jan ’18-’21

ANR STEALTH, “Secure and TrustEd AnaLog hardware TecHnology,” Jan ’18-’21

Awards and Fellowships

Best Paper Award, *2015 IEEE European Test Symposium*

Best Paper Award, *2012 IEEE European Test Symposium*

Best Student Paper Award, *2011 IEEE International Mixed-Signals, Sensors, and Systems Test Workshop*

Best Paper Award, *2009 IEEE European Test Symposium*

Yale University Fellowship, Sep ’01 - Sep ’06

Yale Conference Travel Fund (CTF) Award, 2006

IEEE Computer Society Test Technology Technical Council Doctoral Thesis Award, third place winner, 2005

Stavros S. Niarchos Research Fellowship, summer 2003

Commercial Bank of Greece Award for Academic Excellence, 1998-2001

Publications

Peer-Reviewed Journal Papers:

1. H.-G. Stratigopoulos and C. Streitwieser, “Adaptive Test with Test Escape Estimation for Mixed-Signal ICs,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2017 (to appear)
2. A. Ahmadi, H.-G. Stratigopoulos, K. Huang, A. Nahar, B. Orr, M. Pas, J. M. Carulli Jr., and Y. Makris, “Yield Forecasting Across Semiconductor Fabrication Plants and Design Generations,” *IEEE Transactions on Computer-Aided Design of Integrated*

Circuits and Systems, vol. 36, no. 12, pp. 2120-2133, 2017

3. M. Andraud, H.-G. Stratigopoulos, and E. Simeu, "One-Shot Non-Intrusive Calibration Against Process Variations for Analog/RF Circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 11, pp. 2022-2035, 2016
4. M. Barragan, R. Alhakim, H.-G. Stratigopoulos, M. Dubois, S. Mir, H. Le Gall, N. Bhargava, and A. Bal, "A Fully-Digital BIST Wrapper Based on Ternary Test Stimuli for the Dynamic Test of a 40nm CMOS 18-bit Stereo Audio $\Sigma\Delta$ ADC," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 11, pp. 1876-1888, 2016
5. M. Barragan, H.-G. Stratigopoulos, S. Mir, H. Le-Gall, N. Bhargava, and A. Bal, "Practical Simulation Flow for Evaluating Analog and Mixed-Signal Test Techniques," *IEEE Design & Test of Computers*, vol. 33, no. 6, pp. 46-54, 2016
6. G. Renaud, M. Barragan, A. Laraba, H.-G. Stratigopoulos, S. Mir, H. Le-Gall, and H. Naudet, "A 65nm CMOS Ramp Generator Design and its Application Towards a BIST Implementation of the Reduced-code Static Linearity Test Technique for Pipeline ADCs," *Journal of Electronic Testing: Theory & Applications*, Springer, vol. 32, no. 4, pp. 407-421, 2016
7. A. Laraba, H.-G. Stratigopoulos, S. Mir, and H. Naudet, "Exploiting Pipeline ADC Properties for a Reduced-Code Linearity Test Technique," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 10, pp. 2391-2400, 2015
8. A. Dimakos, H.-G. Stratigopoulos, A. Siligaris, S. Mir, and E. De Foucauld, "Parametric Built-In Test for 65nm RF LNA Using Non-Intrusive Variation-Aware Sensors," *Journal of Electronic Testing: Theory & Applications*, Springer, vol. 31, no. 4, pp. 381-394, 2015
9. H.-G. Stratigopoulos and S. Sunter, "Fast Monte Carlo-Based Estimation of Analog Parametric Test Metrics", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no. 12, pp. 1977-1990, 2014
10. A. Laraba, H.-G. Stratigopoulos, S. Mir, H. Naudet, and G. Bret, "Reduced Code Testing of Pipeline ADCs," *IEEE Design & Test of Computers*, vol. 30, no. 6, pp. 80-88, 2013
11. K. Huang, H.-G. Stratigopoulos, S. Mir, C. Hora, Y. Xing, and B. Kruseman, "Diagnosis of Local Spot Defects in Analog Circuits," *IEEE Transactions on Instrumentation and Measurement*, vol. 61, no. 10, pp. 2701-2712, 2012
12. H.-G. Stratigopoulos, "Test Metrics Model for Analog Test Development," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 31, no. 7, pp. 1116-1128, 2012
13. H.-G. Stratigopoulos and S. Mir, "Adaptive Alternate Analog Test," *IEEE Design & Test of Computers*, vol. 29, no. 4, pp. 71-79, 2012
14. L. Abdallah, H.-G. Stratigopoulos, S. Mir, and C. Kelma, "RF Front-End Test Using Built-In Sensors," *IEEE Design & Test of Computers*, vol. 28, no. 6, pp. 76-84, 2011
15. A. Bounceur, S. Mir, and H.-G. Stratigopoulos, "Estimation of Analog Parametric Test Metrics Using Copulas," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 30, no. 9, pp. 1400-1410, 2011
16. H.-G. Stratigopoulos, P. Drineas, M. Slamani, and Y. Makris, "RF Specification Test Compaction Using Learning Machines," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 18, no. 6, pp. 998-1002, 2010
17. H.-G. Stratigopoulos, S. Mir, and A. Bounceur, "Evaluation of Analog/RF Test Measurements at the Design Stage," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 28, no. 4, pp. 582-590, 2009
18. H.-G. Stratigopoulos, Y. Makris, "Error Moderation in Low-Cost Machine Learning-Based Analog/RF Testing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 27, no. 2, pp. 339-351, 2008

19. H.-G. Stratigopoulos, Y. Makris, "An Adaptive Checker for the Fully-Differential Analog Code," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 6, pp. 1421-1429, 2006
20. H.-G. Stratigopoulos, Y. Makris, "Concurrent Detection of Erroneous Responses in Linear Analog Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 25, no. 5, pp. 878-891, 2006
21. H.-G. Stratigopoulos, Y. Makris, "Non-Linear Decision Boundaries for Testing Analog Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, no. 11, pp. 1760-1773, 2005
22. H.-G. Stratigopoulos, Y. Makris, "An Analog Checker with Input-Relative Tolerance for Duplicate Signals," *Journal of Electronic Testing: Theory & Applications*, Kluwer Academic Publishers (now Springer), vol. 20, no. 5, pp. 479-488, 2004

Peer-Reviewed Conference Papers:

23. H.-G. Stratigopoulos and C. Streitwieser, "Adaptive test flow for mixed-signal ICs," *IEEE VLSI Test Symposium*, Las Vegas, NV, USA, April 2017
24. A. Ahmadi, H.-G. Stratigopoulos, A. Nahar, B. Orr, M. Pas, and Y. Makris, "Harnessing Fabrication Process Signature for Predicting Yield Across Designs," *IEEE International Symposium on Circuits and Systems*, Montreal, Canada, May 2016
25. A. Dimakos, H.-G. Stratigopoulos, A. Siligaris, S. Mir, and E. De Foucauld, "Built-in Test Paradigm for Millimeter-Wave Circuits Based on Non-Intrusive Sensors," *Design, Automation and Test in Europe Conference*, Dresden, Germany, March 2016
26. A. Ahmadi, H.-G. Stratigopoulos, A. Nahar, B. Orr, M. Pas, and Y. Makris, "Yield Forecasting in Fab-to-Fab Production Migration Based on Bayesian Model Fusion," *IEEE/ACM International Conference on Computer-Aided Design*, Austin, TX, USA, November 2015
27. H.-G. Stratigopoulos, M. J. Barragan, S. Mir, H. Le Gall, N. Bhargava, and A. Bal, "Evaluation of Low-Cost Mixed-Signal Test Techniques for Circuits with Long Simulation Times," *IEEE International Test Conference*, Anaheim, CA, USA, October 2015
28. H. Le Gall, R. Alhakim, M. Valka, S. Mir, H.-G. Stratigopoulos, and E. Simeu, "High Frequency Jitter Estimator for SoC," *IEEE European Test Symposium*, Cluj-Napoca, Romania, May 2015
29. J. Liaperdos, H.-G. Stratigopoulos, L. Abdallah, Y. Tsiatouhas, A. Arapoyanni, and X. Li, "Fast Deployment of Alternate Analog Test Using Bayesian Model Fusion," *Design, Automation and Test in Europe Conference*, Grenoble, France, March 2015
30. A. Serhan, L. Abdallah, H.-G. Stratigopoulos, and S. Mir, "Low-cost EVM built-in test of RF transceivers," *IEEE International Design & Test Symposium*, Algiers, Algeria, December 2014
31. M. Dubois, H.-G. Stratigopoulos, S. Mir, and M. J. Barragan, "Evaluation of Digital Ternary Stimuli for Dynamic Test of ΣΔ ADCs," *22nd IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Playa del Carmen, Mexico, September 2014
32. J. Altet, E. Aldrete-Vidrio, F. Reverter, D. Gomez, J.-L. Gonzalez, M. Onabajo, J. Silva-Martinez, B. Martineau, X. Perpina, L. Abdallah, H.-G. Stratigopoulos, X. Aragones, X. Jorda, M. Vellvehi, S. Dilhaire, S. Mir, and D. Mateo, "Review of temperature sensors as monitors for RF-MMW built-in testing and self-calibration schemes", *IEEE 57th International Midwest Symposium on Circuits and Systems*, College Station, TX, USA, August 2014
33. M. Andraud, A. Deluthault, M. Dieng, F. Azais, S. Bernard, P. Cauvet, M. Comte, T. Kervaon, V. Kerzerho, S. Mir, P.-H. Pugliesi-Conti, M. Renovell, F. Soulier, E. Simeu, and H.-G. Stratigopoulos, "Solutions for the self-adaptation of communicating systems

in operation," *IEEE International On-Line Testing Symposium*, Platja d'Aro, Spain, July 2014

34. M. Andraud, H.-G. Stratigopoulos, and E. Simeu, "One-Shot Calibration of RF Circuits Based on Non-Intrusive Sensors," *Design Automation Conference*, San Francisco, CA, USA, June 2014
35. H.-G. Stratigopoulos and S. Sunter, "Efficient Monte Carlo-Based Analog Parametric Fault Modelling," *IEEE VLSI Test Symposium*, Napa, CA, USA, April 2014
36. L. Abdallah, H.-G. Stratigopoulos, and S. Mir, "True Non-Intrusive Sensors for RF Built-In Test," *IEEE International Test Conference*, Anaheim, CA, USA, September 2013, Paper PTF2
37. K. Huang, H.-G. Stratigopoulos, and S. Mir, "Fault Modeling and Diagnosis for Nanometric Analog Circuits," *IEEE International Test Conference*, Anaheim, CA, USA, September 2013, Paper PTF3
38. H.-G. Stratigopoulos, P. Faubet, Y. Courant, and F. Mohamed, "Multidimensional Analog Test Metrics Estimation Using Extreme Value theory and Statistical Blockade," *Design Automation Conference*, Austin, TX, USA, June 2013
39. L. Abdallah, H.-G. Stratigopoulos, S. Mir, and J. Altet, "Defect-Oriented Non Intrusive RF Test Using On-Chip Temperature Sensors," *IEEE VLSI Test Symposium*, Berkeley, CA, USA, April-May 2013
40. A. Laraba, H.-G. Stratigopoulos, S. Mir, H. Naudet, and G. Bret, "Reduced-Code Linearity Testing of ADCs in the Presence of Noise," *IEEE VLSI Test Symposium*, Berkeley, CA, USA, April-May 2013
41. K. Huang, H.-G. Stratigopoulos, L. Abdallah, S. Mir, and A. Bounceur, "Multivariate Statistical Techniques for Analog Parametric Test Metrics Estimation," *Design & Technology of Integrated Systems in Nanoscale Era*, Abu Dhabi, UAE, March 2013, pp. 6-11
42. L. Abdallah, H.-G. Stratigopoulos, S. Mir, and C. Kelma, "Experiences With Non-Intrusive Sensors for RF Built-In Test," *IEEE International Test Conference*, Anaheim, CA, USA, November 2012, Paper 17.1
43. A. Laraba, H.-G. Stratigopoulos, S. Mir, H. Naudet, and C. Forel, "Enhanced Reduced Code Linearity Test Technique for Multi-bit/Stage Pipeline ADCs," *IEEE European Test Symposium*, Annecy, France, May 2012, pp. 50-55
44. L. Abdallah, H.-G. Stratigopoulos, S. Mir, and J. Altet, "Testing RF Circuits with True Non-Intrusive Built-In Sensors," *Design, Automation and Test in Europe Conference*, Dresden, Germany, March 2012, pp. 1090-1095
45. D. De Jonghe, E. Maricau, G. Gielen, T. McConaghy, B. Tasic, and H.-G. Stratigopoulos, "Advances in Variation-Aware Modeling, Verification, and Testing of Analog ICs," *Design, Automation and Test in Europe Conference*, Dresden, Germany, March 2012, pp. 1615-1620
46. A. Spyronasios, L. Abdallah, H.-G. Stratigopoulos, and S. Mir, "On Replacing an RF Test with an Alternative Measurement: Theory and a Case Study," *IEEE Asian Test Symposium*, New Delhi, India, November 2011, pp. 365-370
47. N. Kupp, H.-G. Stratigopoulos, P. Drineas, and Y. Makris, "On Proving the Efficiency of Alternative RF Tests," *IEEE/ACM International Conference on Computer-Aided Design*, San Jose, CA, USA, November 2011, pp. 762-767
48. K. Huang, H.-G. Stratigopoulos, and S. Mir, "Bayesian Fault Diagnosis of RF Circuits Using Nonparametric Density Estimation," *IEEE Asian Test Symposium*, Shanghai, China, December 2010, pp. 295-298
49. H.-G. Stratigopoulos, S. Mir, "Analog Test Metrics Estimates with PPM Accuracy," *IEEE/ACM International Conference on Computer-Aided Design*, San Jose, CA, USA, November 2010, pp. 241-247

50. D. Maliuk, H.-G. Stratigopoulos, H. Huang, and Y. Makris, “Analog Neural Network Design for RF Built-In Self-Test,” *IEEE International Test Conference*, Austin, TX, USA, November 2010, Paper 23.2
51. D. Maliuk, H.-G. Stratigopoulos, and Y. Makris, ”An Analog VLSI Multilayer Perceptron and its Application Towards Built-In Self-Test in Analog Circuits,” *IEEE International On-Line Testing Symposium*, Corfu, Greece, July 2010, 71-76
52. L. Abdallah, H.-G. Stratigopoulos, C. Kelma, and S. Mir, “Sensors for Built-In Alternate RF Test,” *IEEE European Test Symposium*, Prague, Czech Republic, May 2010, pp. 49-54
53. K. Huang, H.-G. Stratigopoulos, and S. Mir, “Fault Diagnosis of Analog Circuits Based on Machine Learning,” *Design, Automation and Test in Europe Conference*, Dresden, Germany, March 2010, pp. 1761-1766
54. M. Dubois, H.-G. Stratigopoulos, and S. Mir, “Hierarchical Parametric Test Metrics Estimation: A $\Sigma\Delta$ Converter BIST Case-Study,” *IEEE International Conference on Computer Design*, Lake Tahoe, California, USA, October 2009, pp. 78-83
55. H.-G. Stratigopoulos, S. Mir, E. Acar, and S. Ozev, “Defect Filter for Alternate RF Test,” *IEEE European Test Symposium*, Sevilla, Spain, May 2009, pp. 101-106
56. H.-G. Stratigopoulos, S. Mir, and Y. Makris, “Enrichment of Limited Training Sets in Machine-Learning-Based Analog/RF Testing,” *Design, Automation and Test in Europe Conference*, Nice, France, April 2009, pp. 1668-1673
57. L. Kupka, E. Simeu, H.-G. Stratigopoulos, L. Rufer, S. Mir, and O. Tumova, “Signature analysis for MEMS pseudorandom testing using neural networks,” *12th IMEKO Joint Symposium on Man Science and Measurement*, Annecy, France, September 2008, pp. 321-325
58. J. Dardig, H.-G. Stratigopoulos, E. Stern, M. Reed, and Y. Makris, “A Statistical Approach to Characterizing and Testing Functionalized Nanowires,” *IEEE VLSI Test Symposium*, San Diego, California, USA, April-May 2008, pp. 267-274
59. H.-G. Stratigopoulos, J. Tongbong, and S. Mir, “A General Method to Evaluate RF BIST Techniques Based on Non-parametric Density Estimation,” *Design, Automation and Test in Europe Conference*, Munich, Germany, March 2008, pp. 68-73
60. H.-G. Stratigopoulos, P. Drineas, M. Slamani, and Y. Makris, “Non-RF To RF Test Correlation Using Learning Machines: A Case Study,” *IEEE VLSI Test Symposium*, Berkeley, California, USA, May 2007, pp. 9-14
61. H.-G. Stratigopoulos, Y. Makris, “Bridging the Accuracy of Functional and Machine-Learning-Based Mixed-Signal Testing,” *IEEE VLSI Test Symposium*, Berkeley, California, USA, April-May 2006, pp. 406-411
62. H.-G. Stratigopoulos, Y. Makris, “Constructive Derivation of Analog Specification Test Criteria,” *IEEE VLSI Test Symposium*, Palm Springs, California, USA, May 2005, pp. 395-400
63. H.-G. Stratigopoulos, Y. Makris, ”Generating Decision Regions in Analog Measurement Spaces,” *ACM Great Lakes Symposium in VLSI*, Chicago, Illinois, USA, April 2005, pp. 88-91
64. H.-G. Stratigopoulos, Y. Makris, “Concurrent Error Detection in Linear Analog Circuits Using State Estimation,” *IEEE International Test Conference*, Charlotte, North Carolina, USA, September-October 2003, pp. 1164-1173
65. H.-G. Stratigopoulos, Y. Makris, “An Analog Checker with Input-Relative Tolerance for Duplicate Signals,” *IEEE International On-Line Testing Symposium*, Kos Island, Greece, July 2003, pp. 54-58
66. H.-G. Stratigopoulos, Y. Makris, “An Analog Checker with Dynamically Adjustable Error Threshold for Fully Differential Circuits,” *IEEE VLSI Test Symposium*, Napa Valley, California, USA, April-May 2003, pp. 209-214

Peer-Reviewed Workshop Papers:

67. D. Genius, M.-M. Louërat, F. Pêcheux, L. Apvrille, and H.-G. Stratigopoulos, "Modeling Heterogeneous Embedded Systems with TTool," *5th Workshop on Design Automation for Understanding Hardware Designs*, Dresden, Germany, March 2018
68. A. Dimakos, H.-G. Stratigopoulos, A. Siligaris, S. Mir, and E. De Foucault, "Non-Intrusive Built-In Test for 65nm RF LNA," *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop*, Porto Alegre, Brazil, September 2014
69. H.-G. Stratigopoulos and S. Sunter, "Fast Monte Carlo-Based Estimation of Analog Parametric Test Metrics," *Workshop on Statistical Test Methods*, Paderborn, Germany, May 2014
70. M. Dubois, H.-G. Stratigopoulos, and S. Mir, "Ternary Stimulus for Fully Digital Dynamic Testing of SC $\Sigma\Delta$ ADCs," *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop*, Taipei, Taiwan, May 2012
71. N. Kupp, H.-G. Stratigopoulos, P. Drineas, and Y. Makris, "PPM-Accuracy Error Estimates for Low-Cost Analog Test: A Case Study," *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop*, Santa Barbara, California, USA, May 2011
72. J. Tongbong, L. Abdallah, S. Mir, and H.-G. Stratigopoulos, "Evaluation of Built-In Sensors for RF LNA Response Measurement," *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop*, La Grande Motte - Montpellier, France, June 2010
73. H.-G. Stratigopoulos, S. Mir, "A Versatile Technique for Evaluating Test Measurements at the Design Stage," *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop*, Scottsdale, Arizona, USA, June 2009

Book Chapters

74. H.-G. Stratigopoulos and B. Kaminska, "Analog and Mixed-Signal Test", in *Electronic Design Automation for Integrated Circuits Handbook*, Edited by G. Martin, L. Lavagno, and I. Markov, CRC Press, 2016
75. D. Maliuk, H.-G. Stratigopoulos, and Y. Makris, "Machine Learning-Based BIST in Analog/RF ICs", in *Mixed-Signal Circuits*, Edited by M. Soma and T. Noulis, CRC Press, 2015
76. M. Dubois, H.-G. Stratigopoulos, S. Mir, and M. J. Barragan, "Statistical evaluation of digital techniques for $\Sigma\Delta$ ADC BIST?, *VLSI-SoC: Internet of Things Foundations*, Edited by L. Claesen, M.-T. Sanz-Pascual, R. Reis, and A. Sarmiento-Reye, Springer, pp. 129-148, 2015
77. H.-G. Stratigopoulos and Y. Makris, "Checkers for On-line Self-Testing of Analog Circuits," in *Advanced Circuits for Emerging Technologies*, Edited by K. Iniewski, John Wiley & Sons, Inc., 2012

Invited Talks and Tutorials in Conferences

78. H.-G. Stratigopoulos and Y. Makris, "From Data to Actions: Applications of Data Analytics in Semiconductor Manufacturing & Test," *IEEE International Test Conference*, Half-day Tutorial, Fort Worth, TX, USA, October 2017
79. H.-G. Stratigopoulos, "Adapting the Test Process for Mixed-Signal ICs: Algorithm, Metrics, and Demonstration," *IEEE International Mixed-Signals Test Workshop*, Embedded Tutorial, Thessaloniki, Greece, July 2017
80. H.-G. Stratigopoulos and Y. Makris, "From Data to Actions: Applications of Data Analytics in Semiconductor Manufacturing & Test," *Design, Automation and Test in Europe Conference*, Half-day Tutorial, Lausanne, Switzerland, March 2017

81. H.-G. Stratigopoulos and Y. Makris, “From Data to Actions: Applications of Data Analytics in Semiconductor Manufacturing & Test,” *IEEE International Test Conference*, Half-day Tutorial, Fort Worth, TX, USA, November 2016
82. M. Andraud, H.-G. Stratigopoulos, and E. Simeu, “One-Shot Non-Intrusive Calibration Against Process Variations for Analog/RF Circuits,” *International Workshop on Design Automation for Analog and Mixed-Signal Circuits*, Austin, TX, USA, November 2016
83. M. Andraud, H.-G. Stratigopoulos, and E. Simeu, “Post-manufacturing “One-Shot” Calibration of Analog/RF Circuits Based on Non-intrusive Sensors,” *IEEE International Mixed-Signals Test Workshop*, Sant Feliu de Guíxols, Spain, July 2016
84. H.-G. Stratigopoulos and Y. Makris, “From Data to Actions: Applications of Data Analytics in Semiconductor Manufacturing & Test,” *IEEE International Test Conference*, Half-day Tutorial, Anaheim, CA, USA, October 2015
85. A. Dimakos, M. Andraud, L. Abdallah, H.-G. Stratigopoulos, E. Simeu, and S. Mir, “Test and calibration of RF circuits using built-in non-intrusive sensors ,” *IEEE Computer Society Annual Symposium on VLSI*, Invited Talk in Special Session, Montpellier, France, July 2015
86. M. Andraud, H.-G. Stratigopoulos, and E. Simeu, “Self-healing of RF circuits using built-in non-intrusive sensors,” *13th IEEE International New Circuits and Systems Conference*, Invited Talk in Special Session, Grenoble, France, June 2015
87. H.-G. Stratigopoulos and Y. Makris, “From Data to Actions: Applications of Data Analytics in Semiconductor Manufacturing & Test,” *IEEE International Symposium on Circuits and Systems*, Full-day Tutorial, Lisbon, Portugal, May 2015
88. H.-G. Stratigopoulos and Y. Makris, “From Data to Actions: Applications of Data Analytics in Semiconductor Manufacturing & Test,” *Design, Automation and Test in Europe Conference*, Half-day Tutorial, Grenoble, France, March 2015
89. H.-G. Stratigopoulos, “RF Built-In Test with Non-Intrusive Sensors,” *IEEE VLSI Test Symposium*, Elevator Talk, Napa, CA, USA, April 2014
90. L. Abdallah, H.-G. Stratigopoulos, S. Mir, “Implicit Test of High-Speed Analog Circuits Using Non-Intrusive Sensors,” *IEEE European Conference on Circuit Theory and Design*, Invited Talk in Special Session, Linkping, Sweden, August 2011
91. H.-G. Stratigopoulos, “Statistical Learning for Analog Circuit Testing,” *Design & Technology of Integrated Circuits in Nanoscale Era*, Embedded Tutorial, Athens, Greece, April 2011
92. H.-G. Stratigopoulos, “Adaptive Analog Alternate Test,” *IEEE Latin-American Test Workshop*, Invited Talk in Special Session, Porto de Galinhas, Brazil, March 2011
93. S. Mir, H.-G. Stratigopoulos, M. Dubois, and A. Bounceur, “Evaluation of parametric test metrics for mixed-signal/RF DFT solutions using statistical techniques,” *Catrene European Nanoelectronics Design Technology Conference*, Grenoble, France, June 2010
94. S. Mir, H.-G. Stratigopoulos, and A. Bounceur, “Density Estimation for Analog/RF Test Problem Solving,” *IEEE VLSI Test Symposium*, Invited Talk in IP Session, Santa Cruz, California, USA, April 2010
95. H.-G. Stratigopoulos, Y. Makris, “Checkers for On-Line Monitoring of Analog Circuits,” *CMOS Emerging Technologies*, Invited Talk, Vancouver, Canada, September 2009

Patents

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96. S. Mir, H.-G. Stratigopoulos, M. Dubois, "$\Sigma\Delta$ ADC with test circuitry", US Patent 8,830,098, 2014

Teaching Responsibilities

Design-for-test of analog, mixed-signal, and RF circuits and systems, MSc course, Wireless Integrated Circuits and Systems (WICS), Université Grenoble Alpes, Grenoble, France

Design-for-test of analog, mixed-signal, and RF circuits and systems, MSc course, Systèmes Electroniques & Systèmes Informatiques (SESI), Université Pierre et Marie Curie, Paris, France

Artificial intelligence on silicon and brain-inspired computing, MSc course, Systèmes Electroniques & Systèmes Informatiques (SESI), Université Pierre et Marie Curie, Paris, France

Current Ph.D. Student Advisees

Mr. Julian Leonhard
Sorbonne Université, EDITE
Thesis Title: "Analog Hardware Security and Trust"
Start Date: 1/10/2017

Ms. Sarah Ali El-Sayed
Sorbonne Université, EDITE
Thesis Title: "Self-healing circuits for wireless communications"
Start Date: 15/12/2017

Mr. Antonios Pavlidis
Sorbonne Université, EDITE
Thesis Title: "Electrical fault diagnosis of analog and mixed-signal circuits"
Start Date: 15/01/2018

Mr. Mohamed Elshamy
Sorbonne Université, EDITE
Thesis Title: "Design-for-security of analog and mixed-signal circuits"
Start Date: 15/01/2018

Former Ph.D. Student Advisees

Dr. Martin Andraud
Université Grenoble Alpes, EEATS
Thesis Title: "Solutions for the Self-Adaptation of Wireless Systems"
Defense Date: 14/6/2016
Current Position: post-doc, Eindhoven University of Technology, The Netherlands

Dr. Athanassios Dimakos
Université Grenoble Alpes, EEATS
Thesis Title: "Built-In Test in Wireless Systems Using Non-Intrusive Sensors"
Defense Date: 19/3/2016
Current Position: post-doc, LaMIPS Laboratory, Caen, France

Dr. Asma Laraba
Université Grenoble Alpes, EEATS
Thesis Title: "Built-In Self-Test of Pipeline ADCs"
Defense Date: 20/9/2013
Current Position: XILINX, San Jose, CA, USA

Dr. Louay Abdallah
Université Grenoble Alpes, EEATS
Thesis Title: "Non-Intrusive Sensors for Built-in-Test of RF Circuits"
Defense Date: 22/10/2012
Current Position: Dolphin Integration, Grenoble, France

Dr. Ke Huang
Université Grenoble Alpes, EEATS
Thesis Title: "Fault Modelling and Diagnosis for Nanometric Mixed-Signal/RF Circuits"
Defense Date: 16/11/2011
Current Position: Assistant Professor, San Diego State University, San Diego, CA, USA

Dr. Matthieu Dubois
Université Grenoble Alpes, EEATS
Thesis Title: "Methodology for Estimating Test Metrics Applied to a Novel Built-In Self-Test (BIST) Technique for ΣΔ Converters"
Defense Date: 23/6/2011
Current Position: Pyxalis, Moirans, France

Professional Service

Organizing Committee Member:

- Test Technology Technical Council (TTTC) Student Activities Group, E.J. McCluskey Best Doctoral Thesis Contest, *IEEE VLSI Test Symposium* (VTS '09 -'10)
- *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop* (IMS3TW '09 -'10) - Publications Chair
- *IEEE International Workshop on Test and Validation of High Speed Analog Circuits* (TVHSAC '10, '13) - Program Chair
- *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop* (IMS3TW '11) - Program Chair
- *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop* (IMS3TW '12, '14) - Program Co-Chair
- *Design, Automation and Test in Europe Conference* (DATE '14) - Topic Chair
- *Design, Automation and Test in Europe Conference* (DATE '13, '15) - Topic Co-Chair
- *IEEE European Test Symposium* (ETS '14, '16, '18) - Program Co-Chair
- *IEEE European Test Symposium* (ETS '15) - Topic Chair
- *IEEE International Mixed-Signals Test Workshop* (IMSTW '15) - General Chair
- *IEEE European Test Symposium* (ETS '17) - Program Chair
- *IEEE VLSI Test Symposium* (VTS '18) - Special Sessions Co-Chair

Technical Program Committee Member:

- *IEEE International On-Line Testing Symposium* (IOLTS '08 -'17)
- *Design, Automation and Test in Europe Conference* (DATE '11-'16)
- *IFIP/IEEE International Conference on Very Large Scale Integration* (VLSI-SoC '12-'14)
- *IEEE International Conference on Computer-Aided Design* (ICCAD '12-'14)
- *IEEE VLSI Test Symposium* (VTS '13-'18)
- *IEEE Great Lakes Symposium on VLSI* (GLSVLSI '13-'14)

- *European Workshop on CMOS Variability* (VARI '14-'16)
- *International Design & Test Symposium* (IDT '14-'15)
- *International Conference on Design & Technology of Integrated Systems in Nanoscale Era* (DTIS '14-'15)
- *IEEE International Test Conference* (ITC '15-'17)
- *Frontiers on Analog CAD* (FAC '15, '18)
- *IEEE International Workshop on Test and Validation of High Speed Analog Circuits* (TVHSAC '15)
- *IEEE Latin-American Test Symposium* (LATS '16-'18)
- *IEEE North Atlantic Test Workshop* (NATW '16-'17)
- *IEEE International Mixed-Signals Test Workshop* (IMSTW '16-'17)
- *International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design* (SMACD '17-'18)
- *IEEE International Symposium on Power and Timing Modeling, Optimization and Simulation* (PATMOS '17)

Editor:

- *Springer Journal of Electronic Testing: Theory & Applications* (JETTA)
  Guest Editor of Special Issue on "Analog, Mixed-Signal, RF, and MEMS Testing"
  Date of publication: February 2011
- *Springer Journal of Electronic Testing: Theory & Applications* (JETTA)
  Associate Editor since January 2012
- *IEEE Design & Test of Computers*
  Guest Editor of Special Issue on "Digitally Enhanced Wireless Transceivers"
  Date of publication: November/December 2012
- *IEEE Design & Test*
  Associate Editor since December 2011
- *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*
  Associate Editor since October 2012
- *IEEE Design & Test*
  Guest Editor of Special Section on "Top Papers from the 2015 International Test Conference"
  Date of publication: November/December 2016

Technical Referee in additional journals and conferences:

- *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* (TVLSI)
- *IEEE Transactions on Circuits and Systems I* (TCAS-I)
- *IEEE Transactions on Circuits and Systems II* (TCAS-II)
- *ASP Journal of Low Power Electronics* (JOLPE)
- *Wiley International Journal of Circuit Theory and Application*
- *Elsevier Integration, the VLSI Journal*
- *ACM Transactions on Design Automation of Electronic Systems (TODAES)*
- *IEEE Asian Test Symposium* (ATS)

Participation in Ph.D. Juries:

- Eduardo Aldrete, "Strategies for built-in performance monitoring of analog RF circuits with temperature measurements," Universitat Politècnica de Catalunya, Spain, September 2010
- Dídac Gómez Salinas, "Design of Reconfigurable RF circuits for Self-Compensation," Universitat Politècnica de Catalunya, Spain, January 2013
- Delaram Haghighitalab, "Highly digitized RF Receiver for Software Defined Radio," Université Pierre et Marie Curie, France, September 2015
- Syhem Larquech, "Test indirect des circuits analogiques et RF," Université Montpellier, France, December 2015
- Alhassan Sayed, "Récepteur RF front-end pour la radio cognitive basé sur un convertisseur analogique-numérique ΣΔ," Université Pierre et Marie Curie, France, July 2016
- Jury member of 2017 EDA Competition at the International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Italy, 2017
- Anthony Coyette, "Defect-oriented automatic test generation for analog and mixed-signal integrated circuits," KU Leuven, Belgium, December 2017

Panelist:

- *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop* (IMS3TW '09)
  Title: "AMS/RF/sensor testing: can alternate test or BIST replace functional test? Success stories and their limitations."
- *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop* (IMS3TW '12)
  Title: "How Best Can We Deploy Analog/Mixed-Signal DFT Solutions?"
- *IEEE VLSI Test Symposium* (VTS '15)
  Title: "Analog/RF BIST: Are we there yet?"
- *IEEE European Test Symposium* (ETS '15)
  Title: "Is adaptive testing the panacea for the future test problems?"

Panel/Special Session Organizer:

- *IEEE VLSI Test Symposium* (VTS '10)
  Title: "Adaptive Analog Test: Feasibility and Opportunities Ahead"
- *IEEE International On-Line Testing Symposium* (IOLTS '10)
  Title: "On-Line Monitoring for Analog and Sensor-Based Systems"
- *IEEE International On-Line Testing Symposium* (IOLTS '14)
  Title: "Solutions for the Self Adaptation of Communicating Systems in Operation"
- *IEEE Symposium on Circuits And Systems* (ISCAS '16)
  Title: "Data Analytics in Semiconductor Manufacturing and Test"

Session Chair:

- *IEEE VLSI Test Symposium* (VTS '08 - '09)
- *IEEE International On-Line Testing Symposium* (IOLTS '08 -'10,'13)
- *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop* (IMS3TW '09 -'10, '12, '14, '16)
- *Design, Automation and Test in Europe Conference* (DATE '11-'12)
- *IEEE European Test Symposium* (ETS '11,'13,'15-'16)
- *IEEE European Conference on Circuit Theory and Design* (ECCTD '11)

- *IEEE International Conference on Computer-Aided Design* (ICCAD ’11)
- *IEEE International Test Conference* (ITC ’15-’17)

Professional Associations

IEEE, Test Technology Technical Council, Technical Chamber of Greece