Haralampos-G. Stratigopoulos
Sorbonne Universités, UPMC Univ. Paris 6, CNRS, LIP6

LIST OF SCIENTIFIC PUBLICATIONS

1 – Peer reviewed journal articles

[1] H.-G. Stratigopoulos and C. Streitwieser, "Adaptive Test with Test Escape Estimation for Mixed-Signal ICs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2017 (to appear)

[2] A. Ahmadi, H.-G. Stratigopoulos, K. Huang, A. Nahar, B. Orr, M. Pas, J. M. Carulli Jr., and Y. Makris, "Yield Forecasting Across Semiconductor Fabrication Plants and Design Generations," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 36, no. 12, pp. 2120 – 2133, 2017

[3] M. Andraud, H.-G. Stratigopoulos, and E. Simeu, "One-Shot Non-Intrusive Calibration Against Process Variations for Analog/RF Circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 11, pp. 2022 – 2035, 2016

[4] M. Barragan, R. Alhakim, H.-G. Stratigopoulos, M. Dubois, S. Mir, H. Le Gall, N. Bhargava, and A. Bal, "A Fully-Digital BIST Wrapper Based on Ternary Test Stimuli for the Dynamic Test of a 40nm CMOS 18-bit Stereo Audio ΣΔ ADC," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 11, pp. 1876 – 1888, 2016

[5] M. Barragan, H.-G. Stratigopoulos, S. Mir, H. Le-Gall, N. Bhargava, and A. Bal, "Practical Simulation Flow for Evaluating Analog and Mixed-Signal Test Techniques," *IEEE Design & Test*, vol. 33, no. 6, pp. 46 – 54, 2016

[6] G. Renaud, M. Barragan, A. Laraba, H.-G. Stratigopoulos, S. Mir, H. Le-Gall, and H. Naudet, "A 65nm CMOS Ramp Generator Design and its Application Towards a BIST Implementation of the Reduced-code Static Linearity Test Technique for Pipeline ADCs," *Journal of Electronic Testing: Theory & Applications*, Springer, vol. 32, no. 4, pp. 407–421, 2016

[7] A. Laraba, H.-G. Stratigopoulos, S. Mir, and H. Naudet, "Exploiting Pipeline ADC Properties for a Reduced-Code Linearity Test Technique," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 10, pp. 2391-2400, 2015

[8] A. Dimakos, H.-G. Stratigopoulos, A. Siligaris, S. Mir and E. De Foucauld, "Parametric Built-In Test for 65nm RF LNA Using Non-Intrusive Variation-Aware

Sensors," *Journal of Electronic Testing: Theory & Applications*, Springer, vol. 31, no. 4, pp. 381-394, 2015

[9] H.-G. Stratigopoulos and S. Sunter, "Fast Monte Carlo-Based Estimation of Analog Parametric Test Metrics," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no. 12, pp. 1977-1990, 2014

[10] A. Laraba, H.-G. Stratigopoulos, S. Mir, H. Naudet, and G. Bret, "Reduced Code Testing of Pipeline ADCs," *IEEE Design & Test of Computers*, vol. 30, no. 6, pp. 80-88, 2013

[11] K. Huang, H.-G. Stratigopoulos, S. Mir, C. Hora, Y. Xing, and B. Kruseman, "Diagnosis of Local Spot Defects in Analog Circuits," *IEEE Transactions on Instrumentation and Measurement,* vol. 61, no. 10, pp. 2701-2712, 2012

[12] H.-G. Stratigopoulos, "Test Metrics Model for Analog Test Development," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 31, no. 7, pp. 1116-1128, 2012

[13] H.-G. Stratigopoulos and S. Mir, "Adaptive Alternate Analog Test," *IEEE Design & Test of Computers,* vol. 29, no. 4, pp. 71-79, 2012

[14] L. Abdallah, H.-G. Stratigopoulos, S. Mir, and C. Kelma, "RF Front-End Test Using Built-In Sensors," *IEEE Design & Test of Computers*, vol. 28, no. 6, pp. 76-84, 2011

[15] A. Bounceur, S. Mir, and H.-G. Stratigopoulos, "Estimation of Analog Parametric Test Metrics Using Copulas," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 30, no. 9, pp. 1400-1410, 2011

[16] H.-G. Stratigopoulos, P. Drineas, M. Slamani, and Y. Makris, "RF Specification Test Compaction Using Learning Machines," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 18, no. 6, pp. 998-1002, 2010

[17] H.-G. Stratigopoulos, S. Mir, and A. Bounceur, "Evaluation of Analog/RF Test Measurements at the Design Stage," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 28, no. 4, pp. 582-590, 2009

[18] H.-G. Stratigopoulos, Y. Makris, "Error Moderation in Low-Cost Machine Learning-Based Analog/RF Testing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 27, no. 2, pp. 339-351, 2008

[19] H.-G. Stratigopoulos, Y. Makris, "An Adaptive Checker for the Fully-Differential Analog Code," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 6, pp. 1421-1429, 2006

[20] H.-G. Stratigopoulos, Y. Makris, "Concurrent Detection of Erroneous Responses in Linear Analog Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 25, no. 5, pp. 878-891, 2006

[21] H.-G. Stratigopoulos, Y. Makris, "Non-Linear Decision Boundaries for Testing Analog Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, no. 11, pp. 1760-1773, 2005

[22] H.-G. Stratigopoulos, Y. Makris, "An Analog Checker with Input-Relative Tolerance for Duplicate Signals," *Journal of Electronic Testing: Theory & Applications*, Kluwer Academic Publishers (now Springer), vol. 20, no. 5, pp. 479-488, 2004

2 – Invited talks and tutorials in conferences

[23] H.-G. Stratigopoulos and Y. Makris, "From Data to Actions: Applications of Data Analytics in Semiconductor Manufacturing & Test," IEEE International Test Conference, Half-day Tutorial, Fort Worth, TX, USA, October 2017

[24] H.-G. Stratigopoulos, "Adapting the Test Process for Mixed-Signal ICs: Algorithm, Metrics, and Demonstration," *IEEE International Mixed-Signals Test Workshop*, Embedded Tutorial, Thessaloniki, Greece, July 2017

[25] H.-G. Stratigopoulos and Y. Makris, "From Data to Actions: Applications of Data Analytics in Semiconductor Manufacturing & Test," *Design, Automation and Test in Europe Conference*, Half-day Tutorial, Lausanne, Switzerland, March 2017

[26] H.-G. Stratigopoulos and Y. Makris, "From Data to Actions: Applications of Data Analytics in Semiconductor Manufacturing & Test," IEEE International Test Conference, Half-day Tutorial, Fort Worth, TX, USA, November 2016

[27] M. Andraud, H.-G. Stratigopoulos, and E. Simeu, "One-Shot Non-Intrusive Calibration Against Process Variations for Analog/RF Circuits," *International Workshop on Design Automation for Analog and Mixed-Signal Circuits*, Austin, TX, USA, November 2016

[28] M. Andraud, H.-G. Stratigopoulos, and E. Simeu, "Post-manufacturing "One-Shot'' Calibration of Analog/RF Circuits Based on Non-intrusive Sensors," *IEEE International Mixed-Signals Test Workshop*, Sant Feliu de Guixols, Spain, July 2016

[29] H.-G. Stratigopoulos and Y. Makris, "From Data to Actions: Applications of Data Analytics in Semiconductor Manufacturing & Test," IEEE International Test Conference, Half-day Tutorial, Anaheim, CA, USA, October 2015

[30] A. Dimakos, M. Andraud, L. Abdallah, H.-G. Stratigopoulos, E. Simeu, and S. Mir, "Test and calibration of RF circuits using built-in non-intrusive sensors ," *IEEE Computer Society Annual Symposium on VLSI*, Invited Talk in Special Session, Montpellier, France, July 2015

[31] M. Andraud, H.-G. Stratigopoulos, and E. Simeu, "Self-healing of RF circuits using built-in non-intrusive sensors," *13th IEEE International New Circuits and Systems Conference*, Invited Talk in Special Session, Grenoble, France, June 2015

[32] H.-G. Stratigopoulos and Y. Makris, "From Data to Actions: Applications of Data Analytics in Semiconductor Manufacturing & Test," *IEEE International*

Symposium on Circuits and Systems, Full-day Tutorial, Lisbon, Portugal, May 2015

[33] H.-G. Stratigopoulos and Y. Makris, “From Data to Actions: Applications of Data Analytics in Semiconductor Manufacturing & Test," *Design, Automation and Test in Europe Conference*, Half-day Tutorial, Grenoble, France, March 2015

[34] H.-G. Stratigopoulos, ``RF Built-In Test with Non-Intrusive Sensors," *IEEE VLSI Test Symposium*, Elevator Talk, Napa, CA, USA, April 2014

[35] L. Abdallah, H.-G. Stratigopoulos, S. Mir, and C. Kelma, "Implicit Test of High-Speed Analog Circuits Using Non-Intrusive Sensors," *IEEE European Conference on Circuit Theory and Design,* Invited Talk in Special Session, Linköping, Sweden, August 2011, p. 652

[36] H.-G. Stratigopoulos, "Statistical Learning for Analog Circuit Testing," *Design & Technology of Integrated Systems in Nanoscale Era*, Embedded Tutorial, Athens, Greece, April 2011

[37] H.-G. Stratigopoulos and S. Mir, "Adaptive Alternate Analog Test," *IEEE Latin-American Test Workshop*, Invited Talk in Special Session, Porto de Galinhas, Brazil, April 2011

[38] S. Mir, H.-G. Stratigopoulos, M. Dubois, and A. Bounceur, "Evaluation of parametric test metrics for mixed-signal/RF DFT solutions using statistical techniques," *Catrene European Nanoelectronics Design Technology Conference*, Grenoble, France, June 2010

[39] S. Mir, H.-G. Stratigopoulos, and A. Bounceur, "Density Estimation for Analog/RF Test Problem Solving," *IEEE VLSI Test Symposium*, Invited Talk in IP Session, Santa Cruz, CA, USA, April 2010, p. 41

[40] H.-G. Stratigopoulos, "Checkers for On-Line Monitoring of Analog Circuits," *CMOS Emerging Technologies*, Invited Talk, Vancouver, Canada, September 2009

3 – Peer reviewed conference articles

[41] H.-G. Stratigopoulos and C. Streitwieser, “Adaptive test flow for mixed-signal ICs,” *IEEE VLSI Test Symposium*, Las Vegas, NV, USA, April 2017

[42] A. Ahmadi, H.-G. Stratigopoulos, A. Nahar, B. Orr, M. Pas, and Y. Makris, "Harnessing Fabrication Process Signature for Predicting Yield Across Designs," *IEEE International Symposium on Circuits and Systems*, Montreal, Canada, May 2016

[43] A. Dimakos, H.-G. Stratigopoulos, A. Siligaris, S. Mir, and E. De Foucauld, ``Built-in Test Paradigm for Millimeter-Wave Circuits Based on Non-Intrusive Sensors," *Design, Automation and Test in Europe Conference*, Dresden, Germany, March 2016

[44] A. Ahmadi, H.-G. Stratigopoulos, A. Nahar, B. Orr, M. Pas, and Y. Makris, ``Yield Forecasting in Fab-to-Fab Production Migration Based on Bayesian Model Fusion," *IEEE/ACM International Conference on Computer-Aided Design,* Austin, TX, USA, November 2015

[45] H.-G. Stratigopoulos, M. J. Barragan, S. Mir, H. Le Gall, N. Bhargava, and A. Bal, ``Evaluation of Low-Cost Mixed-Signal Test Techniques for Circuits with Long Simulation Times," *IEEE International Test Conference*, Anaheim, CA, USA, October 2015

[46] H. Le Gall, R. Alhakim, M. Valka, S. Mir, H.-G. Stratigopoulos, and E. Simeu, ``High Frequency Jitter Estimator for SoC," *IEEE European Test Symposium*, Cluj-Napoca, Romania, May 2015

[47] J. Liaperdos, H.-G. Stratigopoulos, L. Abdallah, Y. Tsiatouhas, A. Arapoyanni, and X. Li, ``Fast Deployment of Alternate Analog Test Using Bayesian Model Fusion," *Design, Automation and Test in Europe Conference*, Grenoble, France, March 2015

[48] A. Serhan, L. Abdallah, H.-G. Stratigopoulos, and S. Mir, ``Low-cost EVM built-in test of RF transceivers," *IEEE International Design & Test Symposium*, Algiers, Algeria, December 2014

[49] M. Dubois, H.-G. Stratigopoulos, S. Mir, and M. J. Barragan, ``Evaluation of Digital Ternary Stimuli for Dynamic Test of ΣΔ ADCs," *22nd IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Playa del Carmen, Mexico, October 2014

[50] J. Altet, E. Aldrete-Vidrio, F. Reverter, D. Gomez, J.-L. Gonzalez, M. Onabajo, J. Silva-Martinez, B. Martineau, X. Perpina, L. Abdallah, H.-G. Stratigopoulos, X. Aragones, X. Jorda, M. Vellvehi, S. Dilhaire, S. Mir, and D. Mateo, ``Review of temperature sensors as monitors for RF-MMW built-in testing and self-calibration schemes", *IEEE 57th International Midwest Symposium on Circuits and Systems*, College Station, TX, USA, August 2014

[51] M. Andraud, A. Deluthault, M. Dieng, F. Azais, S. Bernard, P. Cauvet, M. Comte, T. Kervaon, V. Kerzerho, S. Mir, P.-H. Pugliesi-Conti, M. Renovell, F. Soulier, E. Simeu, and H.-G. Stratigopoulos, ``Solutions for the self-adaptation of communicating systems in operation," *IEEE International On-Line Testing Symposium*, Platja d'Aro, Spain, July 2014

[52] M. Andraud, H.-G. Stratigopoulos, and E. Simeu, "One-Shot Calibration of RF Circuits Based on Non-Intrusive Sensors," Design Automation Conference, San Francisco, CA, USA, June 2014

[53] H.-G. Stratigopoulos and S. Sunter, "Efficient Monte Carlo-based Analog Parametric Fault Modelling," *IEEE VLSI Test Symposium*, Napa, CA, USA, April 2014

[54] L. Abdallah, H.-G. Stratigopoulos, and S. Mir, “True Non-Intrusive Sensors for RF Built-In Test,” *IEEE International Test Conference*, Anaheim, CA, USA, September 2013, Paper PTF2
[55] K. Huang, H.-G. Stratigopoulos, and S. Mir, “Fault Modeling and Diagnosis for Nanometric Analog Circuits,” *IEEE International Test Conference*, Anaheim, CA, USA, September 2013, Paper PTF3
[56] H.-G. Stratigopoulos, P. Faubet, Y. Courant, and F. Mohamed, ”Multidimensional Analog Test Metrics Estimation Using Extreme Value theory and Statistical Blockade”, *Design Automation Conference*, Austin, TX, USA, June 2013
[57] L. Abdallah, H.-G. Stratigopoulos, S. Mir, and J. Altet, “Defect-Oriented Non-Intrusive RF Test Using On-Chip Temperature Sensors,” *IEEE VLSI Test Symposium*, Berkeley, CA, USA, April-May 2013
[58] A. Laraba, H.-G. Stratigopoulos, S. Mir, H. Naudet, and G. Bret, "Reduced-Code Linearity Testing of ADCs in the Presence of Noise, ” *IEEE VLSI Test Symposium*, Berkeley, CA, USA, April-May 2013
[59] K. Huang, H.-G. Stratigopoulos, L. Abdallah, S. Mir, and A. Bounceur, “Multivariate Statistical Techniques for Analog Parametric Test Metrics Estimation,” *International Conference on Design & Technology of Integrated Systems in Nanoscale Era*, Abu Dhabi, UAE, March 2013, pp. 6-11
[60] L. Abdallah, H.-G. Stratigopoulos, S. Mir, and C. Kelma, “Experiences With Non-Intrusive Sensors for RF Built-In Test,” *IEEE International Test Conference*, Anaheim, CA, USA, November 2012, Paper 17.1
[61] A. Laraba, H.-G. Stratigopoulos, S. Mir, H. Naudet, and C. Forel, "Enhanced Reduced Code Linearity Test Technique for Multi-bit/Stage Pipeline ADCs," *IEEE European Test Symposium*, Annecy, France, May 2012, pp. 50-55
[62] L. Abdallah, H.-G. Stratigopoulos, S. Mir, and J. Altet, "Testing RF Circuits with True Non-Intrusive Built-In Sensors," *Design, Automation and Test in Europe Conference*, Dresden, Germany, March 2012, pp. 1090-1095
[63] D. De Jonghe, E. Maricau, G. Gielen, T. McConaghy, B. Tasic, and H.-G. Stratigopoulos, "Advances in Variation-Aware Modeling, Verification, and Testing of Analog ICs," *Design, Automation and Test in Europe Conference*, Dresden, Germany, March 2012, pp. 1615-1620
[64] A. Spyronasios, L. Abdallah, H.-G. Stratigopoulos, and S. Mir, "On Replacing an RF Test with an Alternative Measurement: Theory and a Case Study," *IEEE Asian Test Symposium,* New Delhi, India, November 2011, pp. 365-370
[65] N. Kupp, H.-G. Stratigopoulos, P. Drineas, and Y. Makris, "On Proving the Efficiency of Alternative RF Tests," *IEEE/ACM International Conference on Computer-Aided Design*, San Jose, CA, USA, November 2011, pp. 762-767

[66] K. Huang, H.-G. Stratigopoulos, and S. Mir, " Bayesian Fault Diagnosis of RF Circuits Using Nonparametric Density Estimation," *IEEE Asian Test Symposium*, Shanghai, China, December 2010, pp. 295-298
[67] H.-G. Stratigopoulos, S. Mir, "Analog Test Metrics Estimates with PPM Accuracy," *IEEE/ACM International Conference on Computer-Aided Design*, San Jose, CA, USA, November 2010, pp. 241-247
[68] D. Maliuk, H.-G. Stratigopoulos, H. Huang, and Y. Makris, "Analog Neural Network Design for RF Built-In Self-Test," *IEEE International Test Conference*, Austin, TX, USA, November 2010, Paper 23.2
[69] D. Maliuk, H.-G. Stratigopoulos, and Y. Makris, "An Analog VLSI Multilayer Perceptron and its Application Towards Built-In Self-Test in Analog Circuits," *IEEE International On-Line Testing Symposium*, Corfu, Greece, July 2010, 71-76
[70] L. Abdallah, H-G. Stratigopoulos, C. Kelma, and S. Mir, "Sensors for Built-In Alternate RF Test," *IEEE European Test Symposium*, Prague, Czech Republic, May 2010, pp. 49-54
[71] K. Huang, H.-G. Stratigopoulos, and S. Mir, "Fault Diagnosis of Analog Circuits Based on Machine Learning," *Design, Automation and Test in Europe Conference*, Dresden, Germany, March 2010, pp. 1761-1766
[72] M. Dubois, H.-G. Stratigopoulos, and S. Mir, "Hierarchical Parametric Test Metrics Estimation: A $\Sigma\Delta$ Converter BIST Case-Study," *IEEE International Conference on Computer Design,* Lake Tahoe, California, USA, October 2009, pp. 78-83
[73] H.-G. Stratigopoulos, S. Mir, E. Acar, and S. Ozev, "Defect Filter for Alternate RF Test," *IEEE European Test Symposium*, Sevilla, Spain, May 2009, pp. 101-106
[74] H.-G. Stratigopoulos, S. Mir, and Y. Makris, "Enrichment of Limited Training Sets in Machine-Learning-Based Analog/RF Testing," *Design, Automation and Test in Europe Conference*, Nice, France, April 2009, pp. 1668-1673
[75] L. Kupka, E. Simeu, H.-G. Stratigopoulos, L. Rufer, S. Mir, and O. Tumova, "Signature analysis for MEMS pseudorandom testing using neural networks," *12th IMEKO Joint Symposium on Man Science and Measurement*, Annecy, France, September 2008, pp. 321-325
[76] J. Dardig, H.-G. Stratigopoulos, E. Stern, M. Reed, and Y. Makris, "A Statistical Approach to Characterizing and Testing Functionalized Nanowires," *IEEE VLSI Test Symposium*, San Diego, California, USA, April-May 2008, pp. 267-274
[77] H.-G. Stratigopoulos, J. Tongbong, and S. Mir, "A General Method to Evaluate RF BIST Techniques Based on Non-parametric Density Estimation," *Design, Automation and Test in Europe Conference*, Munich, Germany, March 2008, pp. 68-73

[78] H.-G. Stratigopoulos, P. Drineas, M. Slamani, and Y. Makris, "Non-RF To RF Test Correlation Using Learning Machines: A Case Study," *IEEE VLSI Test Symposium*, Berkeley, California, USA, May 2007, pp. 9-14
[79] H.-G. Stratigopoulos, Y. Makris, "Bridging the Accuracy of Functional and Machine-Learning-Based Mixed-Signal Testing," *IEEE VLSI Test Symposium*, Berkeley, California, USA, April-May 2006, pp. 406-411
[80] H.-G. Stratigopoulos, Y. Makris, "Constructive Derivation of Analog Specification Test Criteria," *IEEE VLSI Test Symposium*, Palm Springs, California, USA, May 2005, pp. 395-400
[81] H.-G. Stratigopoulos, Y. Makris, "Generating Decision Regions in Analog Measurement Spaces," *ACM Great Lakes Symposium in VLSI*, Chicago, Illinois, USA, April 2005, pp. 88-91
[82] H.-G. Stratigopoulos, Y. Makris, "Concurrent Error Detection in Linear Analog Circuits Using State Estimation," *IEEE International Test Conference*, Charlotte, North Carolina, USA, September-October 2003, pp. 1164-1173
[83] H.-G. Stratigopoulos, Y. Makris, "An Analog Checker with Input-Relative Tolerance for Duplicate Signals," IEEE International On-Line Testing Symposium, Kos Island, Greece, July 2003, pp. 54-58
[84] H.-G. Stratigopoulos, Y. Makris, "An Analog Checker with Dynamically Adjustable Error Threshold for Fully Differential Circuits," *IEEE VLSI Test Symposium*, Napa Valley, California, USA, April-May 2003, pp. 209-214

4 – Book Chapters

[85] H.-G. Stratigopoulos and B. Kaminska, “Analog and Mixed-Signal Test", in *Electronic Design Automation for Integrated Circuits Handbook*, Edited by Grant Martin, Luciano Lavagno, and Igor Markov, CRC Press, 2016
[86] D. Maliuk, H.-G. Stratigopoulos, and Y. Makris, “Machine Learning-Based BIST in Analog/RF ICs", in *Mixed-Signal Circuits*, Edited by M. Soma and T. Noulis, CRC Press, 2015
[87] M. Dubois, H.-G. Stratigopoulos, S. Mir, and M. J. Barragan, “Statistical evaluation of digital techniques for ΣΔ ADC BIST”, *VLSI-SoC: Internet of Things Foundations*, Edited by L. Claesen, M.-T. Sanz-Pascual, R. Reis, and A. Sarmiento-Reye, Springer, pp. 129-148, 2015
[88] H.-G. Stratigopoulos, Y. Makris, “Checkers for On-line Self-Testing of Analog Circuits,” in *Advanced Circuits for Emerging Technologies*, Edited by Kris Iniewski, John Wiley & Sons, Inc., 2012

5 – Workshop articles

[89] D. Genius, M.-M. Louërat, F. Pêcheux, L. Apvrille, and H.-G. Stratigopoulos, "Modeling Heterogeneous Embedded Systems with TTool," *5th Workshop on Design Automation for Understanding Hardware Designs*, Dresden, Germany, March 2018

[90] A. Dimakos, H.-G. Stratigopoulos, A. Siligaris, S. Mir, and E. De Foucault, "Non-Intrusive Built-In Test for 65nm RF LNA", *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop*, Porto Alegre, Brazil, September 2014

[91] H.-G. Stratigopoulos and S. Sunter, "Fast Monte Carlo-Based Estimation of Analog Parametric Test Metrics," *1st Workshop on Statistical Test Methods*, Paderborn, Germany, May 2014

[92] M. Dubois, H.-G. Stratigopoulos, and S. Mir, "Ternary Stimulus for Fully Digital Dynamic Testing of SC ΣΔ ADCs," *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop*, Taipei, Taiwan, May 2012

[93] N. Kupp, H.-G. Stratigopoulos, P. Drineas, and Y. Makris, "PPM-Accuracy Error Estimates for Low-Cost Analog Test: A Case Study," *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop*, Santa Barbara, California, USA, May 2011

[94] J. Tongbong, L. Abdallah, S. Mir, and H.-G. Stratigopoulos, "Evaluation of Built-In Sensors for RF LNA Response Measurement," *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop*, La Grande Motte – Montpellier, France, June 2010

[95] H.-G. Stratigopoulos, S. Mir, "A Versatile Technique for Evaluating Test Measurements at the Design Stage," *IEEE International Mixed-Signals, Sensors, and Systems Test Workshop*, Scottsdale, Arizona, USA, June 2009

6 – Patents

[96] S. Mir, H.-G. Stratigopoulos, M. Dubois, "ΣΔ ADC with test circuitry", US Patent 8,830,098, 2014