Researcher's/Engineer's Career Background

* One sheet for each researcher/engineer

1) Name

Naohiko Shimizu

2) Organization/Institution Tokai University

(Title, position) Full Professor

(Name) Naohiko Shimizu

(Country) Japan

(Website address: if not available, please attach a sheet describing the outline of the organization/institution in Annex 3.) http://www.u-tokai.ac.jp/international/index.html

3) Date of birth	**26 October 1960**	**4) Sex**	male

5) Education

(University/Institution) Sophia University, Japan

(Degree) Doctor of Engineering

(Date of acquisition) March 1994

(Major) Electrical and Electronics Engineering

6) Research career

1985 Enterprise Computer Division of Hitachi Ltd. (Designer/Engineer of Mainframe computer's hardware)
1995 Tokai University, Assistant Professor
1997 Tokai University, Associate Professor
2005 Tokai University, Full Professor

7) Papers related to the research theme

* You may attach other sheets if necessary

(Title) (see attached paper)

(Name of the journal)

(Date of publication)

(Co-author)

8) Books related to the research theme

* You may attach other sheets if necessary

(Title) (see attached paper)

(Date of publication)

(Co-author)

[Curriculum Vitae]

Naohiko SHIMIZU

1-8-17 Fujimigaoka, Ninomiya-cho, Naka-gun, Kanagawa, 259-0122, Japan
Tel(Office): +81-3-3441-1171 e-mail: nshimizu@ tokai.ac.jp

Doctorate Degree:

March 1994, Doctor of Engineering, Sophia University, Japan
Title of the paper: Parallel Circuit Simulation with Parallelized Sparse Matrix Calculation

Education:

April 1991 to March 1994 Doctor of Science and Engineering, Sophia University, Post Graduate School of Electrical and Electronics Engineering
April 1983 to March 1985 Master of Science and Engineering, Sophia University, Graduate School of Electrical and Electronics Engineering
April 1979 to March 1983 Bachelor of Science and Engineering, Sophia University, Electrical and Electronics Engineering

Work Experience and Position:

April 1995 to Present Tokai University
April 1995 Assistant Professor of Tokai University, Department of Telecommunication Engineering
April 1997 Associate Professor of Tokai University, Department of Telecommunication Engineering
April 2001 Associate Professor of Tokai University, Department of Embedded Technology
April 2005 Full Professor of Tokai University, Department of Embedded Technology
April 2009 Full Professor of Tokai University, Professional Graduate School of Embedded Technology
April 2012 to Present Full Professor of Tokai University, Department of Embedded Technology
March 2014 to September 2014, Sabbatical Leave to LIP6 Paris.
March 2015, invited professor at LIP6 Paris.
March 2016, invited professor at LIP6 Paris.
March 2017, invited professor at LIP6 Paris.
March 2018, invited professor at LIP6 Paris.
March 2019, invited professor at LIP6 Paris.
February 2020 invited professor at LIP6 Paris.

April 1985 - March 1995 Hitachi Ltd. Co. Enterprise Computer Division.
July 1985 Engineer: Mainframe M660, (Instruction control unit, micro programs, RASIS control system, Virtual Machine Assist firmware)
September 1987 Engineer: Database machines (Search engine, Sort engine, logic design, microprogram design)
April 1989 Unit leader of hardware design: Mainframe M860 (logic design, RASIS design, System controller)
April 1993 Performance design engineer: Parallel Super Computer SR2001
September 1993 Unit leader, Engineer, Performance Designer: Parallel Super Computer SR2201

November 2003 to Present CEO of IP ARCH, Inc. USA
January 2010 to Present CTO of Overtone Corp. Japan

Teaching Carrier:

Major Research Fields:

Computer Architecture and Design
Operating Systems
Application Specific Hardware/Software Co-Design
Embedded Systems
High Level Silicon Compiler
Executable Modeling Language and Method

Member of Academy

Institute of Electrical and Electronics Engineering(IEEE)
Association of Computing Machinery(ACM)
Institute of Electronics, Information and Communication Engineer(IEICE)
Information Processing Society of Japan(IPSJ)

Major Social Activity:

2004 - 2008 Committee member of The Information Technology Engineers Examination (ITEE), Ministry of Economy, Trade and Industry [METI]).
2004 - 2009 Committee member of INFORMATION-TECHNOLOGY PROMOTION AGENCY, JAPAN
2017 – current Committee member of The Institution of Professional Engineers, Japan.

Publication List:

See attached Publication List.

Date: 29 Nov. 2021 Signature: _____

Publication List of Naohiko Shimizu (1983.4-2013.12)

*: in Japanese

	Authors	Books, Papers, etc.	Publication Information	Date of Publication
	1 Books			
*	1)Nakazawa, et al.	Introduction to VLSI system design, Chapter 5	Maruzen	1995
*	2)N.Shimizu	Fundamentals of Computer Design	Kyoritsu	2003
	2 Papers			
	[A] Doctoral Thesis (Doctor of Engineering)			
*	1) N.Shimizu	Circuit Simulation with Parallel Sparse Matrix Solver	Sophia University	1994.3
	[B] Journal Papers			
*	1) Shimizu, Takana	Bit-Serial LU Decomposition Processor	IEICE transactions	vol.D 66(12), p1416-1423, 1983-12
*	2) Chigusa, Miki, Shimizu,Tanaka	Sequential Parallel Switched-Capacitor AD/DA Converters by Unity Gain Buffers and Their Applications	IEICE transactions	vol.C 68(3), p232-239, 1985-03
*	3) Mizutani, Shimizu, Tanaka	LISTAP: Symbolic Analysis of Transistor Networks Based on Switching Control	IEICE transactions	vol.A 73(3), p509-519, 1990-03
	4)Shimizu, et al.	Pipelining Gauss Seidel Method for Analysis of Discrete Time Cellular Neural Networks	IEICE transactions	vol.E77-A(8), 1396-1403, 1994-08-25
	5)Shimizu	High Performance Parallel FFT on Distributed Memory Parallel Computers	Lecture Notes in Computer Science	Vol.1336, pp.317-326, 1997
*	6)Shimizu	Parallel Pipelining SOR Method for an Iterative Linear Equation Solver on a Distributed Memory Parallel Processor	Proceeding of School of Engineering of Tokai University	vol.38(2), 53-59, 1998

*	7)Mitake Shimizu	Processor Architecture and Evaluation which Correspond to Deviation of Memory Latency	Proceeding of School of Engineering of Tokai University	vol.39(1), 43-48, 1999
*	8)Mitake Shimizu	Design of A Memory Latency Tolerant Processor (SCALT)	Proceeding of School of Engineering of Tokai University	vol.40(1), 19-24, 2000
*	9)Li Kouyama Shimizu	Fast MP3 Encoder	Proceeding of Computer System Symposium, IPSJ	Vol.2001, No.16, 137--143
*	10)Li Kouyama Shimizu	An Optimization of MP3 Encoder for Faster Execution	Journal of IPSJ	vol.43(6), 1760-1768, 2002-06-15
*	11)Hayasaka Shimizu	Implementation and Evaluation of Transparent Linux Super Page for IA32	Proceeding of Computer System Symposium, IPSJ	Vol.2002, No.18, pp. 29-35, Nov. 2002
*	12)Kouyama Shimizu	A Design and Evaluation of MP3 Encoder on the Basis of Statistics Data of Sounds	Proceeding of Computer System Symposium, IPSJ	Vol.2002, No.18, pp. 135-141, Nov. 2002
*	13)Hayasaka Shimizu	An Implementation and Evaluation of IA32 Linux Super Page	Journal of IPSJ	vol.44(SIG_10(ACS_2)), 28-35, 2003-07-15
	14)Shimizu	Design of sfl2vl: SFL to Verilog Converter Based on an LR-Parser	IEICE transactions on fundamentals of electronics, communications and computer sciences	vol.E86-A(12), 3225-3229, 2003-12-01
*	15)Iida	Education course with UNIX and PDP-11 Processor on FPGA	IPSJ Letters	vol.LB-005, Vol.2, 43--44, 2003
*	16)Hayasaka, Shimizu	Evaluation of Memory Performance by Linux Super Page and Page Coloring	Proceeding of Symposium on Advanced Computing Systems and Infrastructures	Vol.2003, No.8, pp.209-210, May. 2003
*	17)Shimizu	LSI Design Education on Tokai University	Proceeding of DA Symposium, IPSJ	Vol.2004, No. 8, pp.25-30, Jul.2004
*	18)Mori Futagami Iwasaki Shimizu	Experience and Knowledge of the Educative	Proceeding of Embedded Software	Vol.2004, No.10, pp.78-85, Oct. 2004

		Unmanned Aerial Prove "Hamana-1" Development	Symposium, IPSJ	
*	19)Mimura Khongsomboon Mansoku Shimizu	Development of A Small Data Logger For The Payload on A Model Rocket	Proceeding of Embedded Software Symposium, IPSJ	Vol.2005, No.12, pp.118-125, Oct. 2005
*	20)Kondo et al. Shimizu	The running strategy and the car device property analysis for embedded robot contest	Proceeding of Embedded Software Symposium, IPSJ	Vol.2006, No.9, pp.100-103, Oct. 2006
*	21)Fujita et al. Shimizu	The running strategy and the car device property analysis for embedded robot contest 2008	Proceeding of the School of Information and Telecommunication Engineering Tokai University	Vol.1 No.2, pp.15-22, 2009
*	22)Hiuchi Ogane Shimizu	Clock Tree Generator for Open Souce EDA (Alliance) and Making a Chip with Rohm 0.18um Process	Proceeding of DA Symposium, IPSJ	Vol.2010, No.7 pp.9-14, 2010
*	23)Hiuchi Ogane Shimizu	Building A Design Flow for ON-SEMI 1.2um Digital LSI with A Scalable Cell Library	Proceeding of the School of Information and Telecommunication Engineering Tokai University	vol.3, No.1, pp.25-30, 2010
*	24)Yamazaki et al. Shimizu	Effectiveness of PBL in ASIC 16bit CPU Development	Proceeding of the School of Information and Telecommunication Engineering Tokai University	vol.3, No.1, pp.19-24, 2010
*	25)Hosokawa Higuchi Imai Shimizu	Development of Clock Tree Generator for Open Source EDA Tool Set	Proceeding of DA Symposium, IPSJ	vol.2011, no.5, pp.39-44, 2011
*	26)Higuchi Hosokawa Imai Shimizu	The Implementation Trial and the TEG Chip Development of The Lambda Rule Scalable Cell Libraries to Rohm 0.18um Process	Proceeding of the School of Information and Telecommunication Engineering Tokai University	Vol.4, No1, pp.19-25, 2011
*	27)Hosokawa et al. Shimizu	The Operation and Valuation of Embedded System PBL in ET-robot Contest 2010	Proceeding of the School of Information and Telecommunication Engineering Tokai University	Vol.4, No1, pp.26-33, 2011
*	28)Kamikage Yamazaki Ozawa Shimizu	A UML STRUCTURAL AND BEHAVIORAL SYNTHESIZER FOR FPGA DESIGN	Proceeding of DA Symposium, IPSJ	Vol.2011, No.5, pp.9-14, 2011

*	29)Kano, Shimizu	Visual Method of Designing and Verification of Hardware Design with UML and SysML	Proceeding of the School of Information and Telecommunication Engineering Tokai University	Vol.6, No.1, pp15-21, 2013
*	30)Hosokawa, Shimizu	VLSI Layout Method for Rohm 0.18um Process Technology with Open Source EDA and Cell Library	Proceeding of the School of Information and Telecommunication Engineering Tokai University	Vol.6, No.1, pp23-30, 2013
*	31) Kawano, Saito, Shimizu	Printing and Scanning Systems for Mobile Device	Proceeding of the School of Information and Telecommunication Engineering Tokai University	Vol.7, No.1, pp.9-16, 2014
*	32) Tamaki, Shimizu	Implementation of Multi Game AI system of Blokus Duo on FPGA with NSL	Proceeding of the School of Information and Telecommunication Engineering Tokai University	Vol.7, No.2, pp.9-16, 2015
*	33) Ohtsuka, Shimizu, Shimizu	Systematic Education for Development of Embedded Hardware Design Engineer using FPGA	Proceeding of the School of Information and Telecommunication Engineering Tokai University	Vol.7, No.2, pp.1-8, 2015
	34) Shimizu, Ohtsuka, Okuyama, Shimizu	FPGA and System on Chip Education for Embedded Engineer	International Journal of E-Learning and Educational Technologies in the Digital Media (IJEETDM)	Vol.1, No.2 pp.68-80, 2014
*	35) Furukawa, Shimizu	Enhancing Motivation in Learning of Embedded System with Game Development	Proceeding of the School of Information and Telecommunication Engineering Tokai University	Vol.8, No.2, pp.21-29, 2016
	36) Shimizu	Development of NDA Free VLSI Design Flow for 0.6μm Commercial Fabrication	ICIC Express Letters	Vol.12, No.3,pp.213-220, 2018
	[C] Papers in Proceedings of International Conferences			
	1)Shimizu, Tanaka	Pipelining Gauss-Seidel Method for a	APCCAS92	Sidney, 1992

		Systolic Array		
	2)Naohiko Shimizu, Gui-Xin Cheng and Mamoru Tanaka	Pipelining method without global communications for relaxation-based processor	IEEE International Symposium on Circuits and Systems(ISCAS'92)	San Diego, U.S.A., May 1992.
	3)Tei, Shimizu, Tanaka	Structural compression and reconstruction of static image by ideal diode retina network	ISCAS93	Chicago USA, 1993
	4)Shimizu, Tanaka	A Network-based Parallel Matrix Solver with Pipelining Gauss-Seidel Method	ECCTD93	Swiss, 1993
	5)Tanaka, Shimizu	Pipelining System of Discrete Time Cellular Neural Networks for Information Coding and Decoding	ECCTD93	Swiss, 1993
	6)Shimizu, Tanaka	Some notes on a Relaxation Method for Circuit Simulations	NOLTA93	Hawaii, 1993
	7)Shimizu	NAS Parallel Benchmarks with Segmented / Switched Ethernet Connected Workstations	CTC-CSCC96	Korea, 1996
	8)Shimizu, Watanabe	High Performance Parallel FFT on Distributed Memory Parallel Computers	ISHPC'97	Fukuoka, Japan, Nov., 1997
	9)Shimizu	Parallel Pipelining SOR Method for a Iterative Linear Equation Solver on a Distributed Memory Parallel Processor	11th Annual Symposium on High Performance Computer Systems	Manitoba, Canada, Jul., 1997

	10)Shimizu	Processor Architecture and Evaluation for the Long Deviated Memory Latency	APPT99	Changsha, China, 1999
	11)Shimizu, Mitake	Scalable Latency Tolerant Architecture(SCALT) and Its Evaluation	The First IEEE Asia Pacific Conference on ASICs	Seoul, Korea 1999
	12)Shimizu, Naito	Design of JAVA processor -- TRAJA project	The First IEEE Asia Pacific Conference on ASICs	Seoul, Korea 1999
	13)Shimizu	Multi-Granularity Page Size Support for Linux and the Performance Evaluation	International Software Engineering Symposium (ISES01),	Wuhan University Journal of Natural Sciences, Vol.6 No.1-2, 347--350, 2001
	14)Shimizu	Design of A Memory Latency Tolerant Processor(SCALT),	MEDEA2001	2001, Barcelona, Spain
	15)Shimizu, Takatori	Linux Super Page Kernel for Alpha, Sparc64 and IA32 -- Reducing TLB misses of Applications	MEDEA-2002	2002, Charlottesville, Virginia, USA
	16)Hayasaka, Shimizu	Design of a PCI Bus Interface	ASP-DAC 2003	Yokohama Japan 2003
	17)Kouyama, Nano, Kon, Shimizu	Design of a USB Device Controller IYOYOYO	ASP-DAC 2003	Yokohama Japan 2003
	18)Kon, Shimizu	Design of an i8080A Instruction Compatible Processor with Extended Memory Address	ASP-DAC 2003	Yokohama Japan 2003
	19)Shimizu	The Design of sfl2vl: SFL to Verilog Convertor Based on a LR-parser	SASIMI 2003	Hiroshima Japan 2003

	20)Iida, Shmizu	A PDP-11 Compatible 16-bit Embedded Processor Core For Programmable Chip	COOL Chips VI	Yokohama Japan 2003
	21)Shimizu, Kon	Java Object Look Aside Buffer for Embedded Applications	MEDEA2003	2003, New Orleans, Louisiana, USA
	22)Iida, Shimizu	Design of POP-11(PDP-11 on Programmable Chip)	Proceedings of Asia and South Pacific Design Automation Conference 2004	Yokohama, Jan., 2004
	23)Shimizu	SFL Centric HDL Based Design System and EDA Linux LiveCD	COOL Chips VII	Yokohama Japan 2004
	24)M.Ohyama, N.Shimizu	Development of i8086 Compatible Processor for VLSI Design Education and System on Chip	COOL Chips VII	Yokohama Japan 2004
	25)Khamphong Khongsomboon, Nobuyuki Kondoh, N.Shimizu	Microprocessor Development using SFL for Educational Purposes	2005 6th International Conference On ASIC Proceedings	Shanghai China 2005
	26)K.Khongsomboon, N.Kondoh, M.Ohyama, N.Shimizu	Design and Implementation of a Co-Emulation Environment with High Portability and Usability	SASIMI 2006	Nagoya Japan 2006
	27)Takahito Nakajima, Shigeru Namiki, Shuhei Kinoshita, N.Shimizu	A Portable Co-Verification System Which Generates Testbench Automatically	Proceeding of International Conference on Field-Programmable Technology (ICFPT) 2007	Fukuoka Japan 2007
	28)Sorawat Chivapreecha, N.Shimziu, Kobchai Dejhan	A New Multiplierless Sobel Edge Detection Filter Structure	International Workshop on Nonlinear Circuits and Signal Processing	Hawaii USA 2009

	29)Takahito Nakajima, N.Shimziu	"Design of Co-Emulation System with SCE-MI API	International Workshop on Nonlinear Circuits and Signal Processing	Hawaii USA 2009
	30)Hiroyuki Ohtsuki, N.Shimizu	Synthesize SFL from UML Class Diagram	International Workshop on Nonlinear Circuits and Signal Processing	Hawaii USA 2009
	31) Shimizu et al	A New Logic Circuit Design Methodology with UML	ITC-CSCC 2009	Korea 2009
	33)Shimizu	Reincarnate Historic Systems On FPGA with Novel Design Methodology	XXVII INTERNATIONAL CONFERENCE ON COMPUTER DESIGN 2009	USA 2009
	34)Akiko Yoshizaki, Takafumi Suzuki, Naohiko Shimizu	Computer Design Education with NSL	International Conference on Computer, Communication and Electrical Technology. ICCCET 2011	India 2011
	35)Jun'ichiro Ogane, Takuya Higuchi, Naohiko Shimizu	Develop A Design Flow for Deep Sub-micron Process(0.18um) with A Scalable Cell Library- A Solution Methodology of Clock Skew with Mesh style Clock	ITC-CSCC2010	Thailand 2010
	36)Takuya Higuchi, Jun'ichiro Ogane, Naohiko Shimizu	Develop A Design Flow for Deep Sub-micron Process(0.18um) with A Scalable Cell Library- Adjustment for Deep Sub-micron Process	ITC-CSCC2010	Thailand 2010
	37)Tatsuya Hosokawa, Hiroshi Imai, Takuya Higuchi,	The Application Scalable Cell Libraries to SCMOS with ROHM0.18um	ITC-CSCC2011	Korea 2011

	Naohiko Shimizu	Process and The Learning Method		
	38)Daiki KANO, Ryota YAMAZAKI, Naohiko SHIMIZU	THE METHOD FOR HARDWARE DESIGN TO GENERATE NSL FROM UML DIAGRAM AND THE EXPERIMENTS WITH FPGA	ICCEETS2012	India 2012
	39) Kajihara, Shimizu	New PBL Method for Embedded Technology	ICEAST2012	Thailand pp.406-411, 2012
	40) Shimizu	RTOS Over POSIX for Embedded Application Development and Migration	ICEAST2013	Thailand pp.45-50, 2013
	41)Kajihara, Shimizu	High Speed WEBM Encoder with GPU	ICEAST2013	Thailand pp.177-180, 2013
	42)Shimizu	OSEK/VDX over Linux	LinuxCon Japan 2013	Tokyo, Japan, 2013
	43)Kajihara, Shimizu	Hardware Design Education for Short Term with High Abstraction Level of the Behavior Description Language	IEEE TALE2013	Indonesia pp.705-710, 2013
	44) Kajihara, Shimizu	PROJECT-BASED LEARNING APPROACH APPIED TO EMBEDDED SOFTWARE DEVELOPMENT	Proceedings of the MJIIT-JUC Joint International Symposium	Kanagawa Japan IT-2-4, 2013
	45) Okuyama, Chan, Shimizu	Educational Program for Systems on Chip Design Using Minimal Set of Standalone Computer	ITC-CSCC2014	pp.627-630, 2014
	46) Tamaki, Shimizu	Implementation of BlokusDuo? Hardware with high level behavioral language NSL	ITC-CSCC2014	pp.602-605, 2014
	47) Tamaki,	Implementation of Game Tree Search	Proceedings of the International	pp.99-104, 2014, Kuala Lumpur,

	Shimizu	Method by using NSL	Conference on Computer Science, Computer Engineering, and Education Technologies 2014	Malaysia
	48) Ohtsuka, Shimizu, Okuyama, Shimizu	Rapid Method for Embedded Systems Hardware and Software Education	Proceedings of the International Conference on Computer Science, Computer Engineering, and Education Technologies 2014	pp.90-98, 2014, Kuala Lumpur, Malaysia
	50) Kawano, Shimizu	Development of A Programming Environment on LEGO MindstomsTM with nxtOSEK	ITC-CSCC2015	pp. 362-365, 2015, Seul, Korea
	51) Furukawa, Shimizu	Development of a Game console with High Level Hardware Description Language NSL	ITC-CSCC2015	pp. 728-731, 2015, Seul, Korea
	52) Kawano, Shimizu	Development of a Sugoroku Based Visual Programming Language SUGOPRO for Children	ACEAIT2016	pp.227-337, 2016, Kyoto, Japan
	53) Shimizu, Furukawa	Development of VLSI Design Flow with FOSS EDA and NDA Free Design Rules	5th Asia Symposium on Engineering and Information 2017	pp.39-51, 2017, Hanoi, Vietnam
	54) Shimizu, Kawano	Development of A Visual Programming Language SUGOPRO	5th Asia Symposium on Engineering and Information 2017	pp. 52-62, 2017, Hanoi, Vietnam
	55) Shimizu, Chaput, Louerat	Development of a NDA Free Cell Library for 180nm CMOS Technology with FOSS EDA Tools	5th Asia Symposium on Engineering and Information 2017	pp. 63-71, 2017, Hanoi, Vietnam
	56) Shimizu	Development of NDA Free VLSI Design Flow for 0.6μm Commercial Fabrication	The Twelfth International Conference on Innovative Computing, Information and Control (ICICIC2017)	2017, Kurume, Japan

	57) Shimizu, Akita, Louert, Chaput, Galayko	Open Source Hardware and EDA Tools for Analog/Mixed-Signal Design and Prototyping	International Symposium on Circuits and Systems (ISCAS)2018	pp. 1-5, 2018, Italy
	58) Koyama, Shimizu	Design of an original architecture CPU sun32	14th International Conference on Innovative Computing, Information and Control (ICICIC2019), 2019	2019, Seoul, Korea
	59) Azuma, Morikawa,, Shimizu	Research on the usefulness of winding switching during driving of a brushless DC motor	14th International Conference on Innovative Computing, Information and Control (ICICIC2019), 2019	2019, Seoul, Korea
	60) Sasaishi, Azuma, Koyama, Shimizu	Multi-platform developent of visual programming language SUGOPRO using Node-RED and Cost reduction of programming education equipment by self-made robot	14th International Conference on Innovative Computing, Information and Control (ICICIC2019), 2019	2019, Seoul, Korea
	61) Koyama, Shimizu	Design of an original architecture CPU sun32	ICIC Express Letters,	Vol.14, No.7, pp. 669-678, 2020
	62) Azuma, Morikawa,, Shimizu	Research on the usefulness of winding switching during driving of a brushless DC motor	ICIC Express Letters, Part B: Applications,	Vol.11, No.11, pp.1045-1052, 2020
	63) Sasaishi, Azuma, Koyama, Shimizu	Multi-platform developent of visual programming language SUGOPRO using Node-RED and Cost reduction of programming education equipment by self-made robot	ICIC Express Letters, Part B: Applications,	Vol.11, No.12, pp.1165-1172, 2020
	64) Inoue, Shimizu	Maze search relaxation method hardware high-	ITC-CSCC2021	pp.55-58, 2021, Seul, Korea

		level synthesis language on FPGA by NSL		
	65) Iwaki, Shimizu	Effectiveness of using Model-based development in hardware development	ITC-CSCC2021	pp.59-62, 2021, Seul, Korea
	3 Oral Presentation in Domestic Convention Meeting etc.			
	Over 100 papers			
	4 Miscellaneous			