Internship proposal Bac + 5

AUTOMATIC DESIGN OF CONFIGURABLE OSCILLATORS

Laboratory: LIP6, Pierre et Marie Curie campus (Jussieu), Paris, France

Duration: 6 months

Background: In Systems On Chip (SoC), the Digital Oscillator Controlled (DCO) is a key element for creating clock or synchronization signals. In synchronous SoCs, it is even one of the most critical block, since it sets the timing performances of the whole system.

Among the existing controlled oscillator architectures, the DCO with 3-state inverter [1] is one of the most interesting structures, particularly because of its great regularity and symmetry. This architecture makes layout simpler than for other structures, but still very tedious. Indeed, at present, the design of this type of circuit is mainly handcrafted. This approach is, therefore, sub-optimal and non-reusable. In addition, the oscillator operation is difficult to achieve precisely because the oscillation frequency can vary depending on the technological process parameters and the temperature. This is why it is important to be able to precisely characterize and analyze the performances of such a component in simulation, before its realization (virtual prototyping).

At LIP6 we have developed:

- a method of systematic sizing analogue components [2], based on the control of the operating point (DC analysis) and the small signals (AC analysis),
- a design methodology for this type of DCO [3].
- a method for layout automation [4, 5].

Now, we want to use these 3 methods and extend them, in order to realize the (semi-) automatic synthesis of this family of DCO, based on a set of specifications as small as possible.

Objectives of the internship: During this internship, the design methodology of this family of DCO will be improved from the existing one and implemented to interact with the Coriolis tool of LIP6. For a given technology (65 nm CMOS, typically), this will provide a schematic (with a number of cells, transistors and the sizes of the transistors). Based on this netlist, the call of an electric simulator, configured to realize several different simulations (eg, DC, transient, harmonic analyzes), will provide the main performances of the circuit (e.g., oscillation frequency, power consumption and phase noise). They can then be compared automatically to a set of specifications set by the designer. Once the sizing is frozen, the automated and optimized generation of the layout will be done and the extraction of the associated parasitic elements will be performed. It will ultimately lead us to the evaluation of electrical simulation performances, which will be compared again to the initial specifications.

Tasks to be carried out during the whole internship:

- Understanding the oscillator under study: 2 days;
- Understanding the existing work (sizing and layout): 2 weeks;
- Simulation and analyses with an electric simulator of a simple cell and a DCO, taking into account static properties and large signal behavior: 1 week;
- Specifying the free parameters and the static and dynamic performances to take into account an inverting cell and the oscillator (matrix): 2 days;
- Proposing improvements in the oscillator sizing algorithm, implementing the associated codes and test/analyzes the simulation results: 4 weeks;
- Adapting the layout automation (Python coding) to the oscillator architecture and performing the semi-automatic layout: 12 weeks;

- Layout of inverting and controlled inverting cells. For standard logic, the existing cells will be used directly.
- Using the Placement and Routing Coriolis tool, to get the most compact layout.

- Testing and analyses of the results after extraction of parasitic elements: 2 weeks;
- Writing the internship report: 2 weeks.

Profile: Engineering school student or master 2 in the field of computer science and the Electronics.

Desired skills: Autonomous,
Rigorous,
Critical sense,
Communication skills (speaking and writing)
C ++ and Python programming skills,
Bases in transistor design / simulation,
Interest for mixed signals (analog and digital).

Continuation of the work of internship in doctoral dissertation possible.

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Gratuity: 555 €/month (+ 35 €/month for participation in the public transport costs).

Bibliography:

[1] E. Zianbetov, F. Anceau, M. Javidan, D. Galayko, E. Colinet, J. Juillard, A Digitally Controlled Oscillator in a 65-nm CMOS process for SoC clock generation, IEEE International Symposium on Circuits and Systems (ISCAS), 2011.
[2] https://www-soc.lip6.fr/equipe-cian/logiciels/coriolis/
[3] M. Terosiet, S. Feruglio, D. Galayko, P. Garda, An Analytical Model Of The Oscillation Period For Tri-State Inverter Based DCO, IEEE International Conference on Microelectronics (ICM), 2011.
[4] E. Lao, M. M. Louërat, J. P. Chaput, Highly configurable place and route for analog and mixed-signal circuits, PhD Forum at Design, Automation and Test in Europe Conference (DATE), 2017.
[5] E. Lao, M.M. Louërat, J. P. Chaput, Semi-Automated Analog Placement based on Margin Tolerances, The 20th Workshop on Synthesis And System Integration of Mixed Information Technologies (SASIMI), 2016.