Open Position for Free and Open Source Software Engineer for Open Hardware

Position : Software Engineer (Free and Open Source Software)
Duration : 3 years
Starting date : as soon as possible
Location :
Sorbonne Université, Campus Pierre et Marie Curie, 4 Place Jussieu, 75005 Paris
https://www.sorbonne-universite.fr/en

Team :
CIAN team within LIP6 lab
https://www.lip6.fr/?LANG=en
https://www-soc.lip6.fr/en/team-cian/

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Context: In the framework of the European project **Go IT!** (2022-2025), the Sorbonne Université/LIP6 partner has **an open position for an Engineer interested in Free and Open Source Software (FOSS) development and integration for Open Hardware**.

Go IT! Project moto: Europe's IT hardware development is constantly challenged by outrageously expensive development tools, legal constraints like NDAs or patents, lock-in threats, dependency from external vendors or supply chains and foreign political events. Europe's digital infrastructure (from consumer to critical appliances) is heavily relying on foreign closed-source chips which are literally black-boxes which may (and have been proven to) contain malicious features. This situation makes the hardware development expensive and inefficient, and undermines the very principle of sovereignty, resilience and re-usability. Open-source silicon chips, which are open in their entirety, i.e. down to the physical layout, carry the potential of catapulting Europe into a renaissance of digital technology. Several challenges are on the way, many of which will require the participation of the stakeholders (from the fertile ground made of "nerdy" hobbyists and makers who are the early protagonists of the scene, all the way up to large enterprises), as well as the participation of policymakers and regulatory bodies. The road ahead is steep, but rich of rewards. Therefore we loudly say: Go IT!

The engineer will work at Sorbonne Université, in the LIP6 laboratory.
The technical missions are the following:

Objective 1: Building FOSS design flows for Open Hardware, based on existing FOSS Electronic Design Automation (EDA) software. The result will be a hub of FOSS-EDA software and hardware libraries, from high-level design to layout (physical synthesis). Different tasks are identified:

- On-line Documentation: Creation of a map of the open-source EDA structured by following the main steps of the design.

- Description of alternative design flows, combining several open-source EDA from different repositories, such as :
  - the Placer and Router Coriolis developed in LIP6 http://coriolis.lip6.fr/ ,
  - the library Cell Generator PdkMaster https://chips4makers.io/blog/ ,
  - the Layout Editor Klayout https://klayout.de/ and
  - the logical synthesizer Yosys https://yosyshq.net/yosys/

- Tutorial examples installation using these design flows, purely digital or mixed signal ones.

- Packaging the interoperable tools in Debian Linux distribution.

Objective 2: Open-source Process Design Kit (PDK), PDK compatibility with open- source EDA tools, open-source standard-cell libraries documentation and integration. The work will be done in cooperation with other partners of the project, especially Fibra Servi https://chips4makers.io/blog/

- Perform a survey and prepare a cartography of existing open-source standard-cell libraries. Data will include the maintenance status, the supported platforms and the interoperability with open-source design tools.

- Help the library maintainers to deliver their standard-cell libraries in a format compatible with main open-source design tools, i.e. using a de-facto standard.

- Facilitate for all PDKs made available in this project, the (semi-)automatic creation of a corresponding standard-cell library and analog and mixed-signal blocks.

- Disseminate libraries on mainstream knowledgeable platforms like Wikipedia.

Required Skills:

- Basic knowledge on VLSI design
- Basic knowledge on EDA software
- C++ and Python
- Interest for Free and Open Source Software
- Interest for Open Hardware
- English and French