Subject : Virtual reconfigurable architectures and bitstream management

With the expansion of the capabilities of FPGAs appeared the heterogeneity of the reconfiguration grain within these circuits.
Each fabricant has integrated new computing and memorisation cell units. Inside of modern FPGA, we don't have only LUT's (Look-Up-Tabel) cells, but also distributed memory units, computing operators at medium grain level named DSPs (Digital Signal Processing), to arrive today at high grain level with the System-on-Chip where the reconfigurable architectures coexist, on silicon, with configurable hard processors (number of cores, system clock frequency, dedicated interfaces and system bus; i.e. Zynq chip by Xilinx).
The design and development of FPGA architectures is based on a complex digital CAD design flow that ends with the creation of a hardware configuration file (placement and routing of FPGA resources), called bitstream. This format is related to an FPGA (Intel or Xilinx) manufacturer and are encrypted. There are open source digital CAD tools that allow to define an FPGA architecture in a virtual way, in order to explore new hardware configurations. For example the VTR Framework.

This internship aims to realize an FPGA architecture model as close as possible to one of the last Xilinx circuits, in order to set up the generation of different bitstreams.

The study will take into account the different characteristics of the LUTs, DSP, BRAM memory and elements dedicated to their routing (SB: switch block, CB: connection block). Efforts will focus on getting started with the VTR framework and Xilinx architectures.

Reconfigurable digital architecture skills, VHDL, Verilog will be learned as part of this internship.

Location and Means :

The internship will take place at LIP6 at Sorbonne University, Paris. The tools used will be Linux PCs with Xilinx Vivado development tools, and gcc.

Contacts :

Andrea Pinna
Sorbonne Université
Laboratoire d'Informatique de Paris 6 – LIP6 UMR7606
Tour 25 - Couloir 25/24 – 5éme Étage
Bureau 510
4, Place Jussieu

75252 Paris Cedex 05
Téléphone : 01 44 27 96 35
Mél : andrea.pinna@sorbonne-universite.fr

Sébastien Pillement
IETR UMR 6164 - Syscom
ECOLE POLYTECHNIQUE DE L'UNIVERSITE DE NANTES

Rue Christian Pauc - La Chantrerie CS 50609
44309 NANTES Cedex 3
Bâtiment Ireste, Bureau C116
Téléphone : 02 40 68 30 64
Mél : Sebastien.Pillement@univ-nantes.fr

LIP 6 - CNRS UMR 7606
Équipe SYEL
B.C. 167 - 4, Place Jussieu
75252 Paris Cedex 05
FRANCE
tel. +33 1 44 27 96 35 - fax. +33 1 44 27 96 36