A THIRD-ORDER CURRENT-MODE CONTINUOUS-TIME ΣΔ MODULATOR

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Abstract—

In this paper, the design procedure for a third-order continuous-time ΣΔ modulator with RZ feedback is described. The circuit is realized using continuous-time current-mode integrators and DACs with switched-current sources. A design method to find the minimum biasing current required to achieve the desired dynamic range is presented. With a sampling frequency of 25.6MHz, the circuit is expected to achieve 84dB of dynamic range for a 100kHz bandwidth input signal. The circuit operates from a power supply of 1.7V and consumes 7.4mW in a 0.35μm CMOS process.

I. Introduction

Continuous-time ΣΔ modulators are receiving an increasing attention in low power [1] and high speed [2] applications. In this paper, we present a low power third order continuous-time ΣΔ modulator suitable for base-band telecommunication applications. In section II, a systematic method is used to derive integrators gains and feedback coefficients of a third-order continuous-time modulator, starting from a third-order discrete-time modulator. In section III, the circuits used to realize the integrators, the digital-to-analog converters and the comparator are presented. A design method to find the minimum biasing current of the integrators is also presented in section III. Circuit characteristics and simulation results are discussed in sections IV and V. The conclusion is given in section VI.

II. System Design

A general design method for continuous-time ΣΔ modulators, starting from the conventional discrete-time ΣΔ modulators was described in [3]. Only the special case of a third order system will be detailed in this paper. A third-order discrete-time ΣΔ modulator is shown in Fig.1. We would like to obtain the coefficients a_1, a_2 and a_3 of the continuous-time modulator, shown in Fig. 2, in function of the discrete-time modulator coefficients b_1, b_2 and b_3. The feedback digital-to-analog converter is assumed to have an output signal as shown in Fig.3.

It has been demonstrated in [3] that the $\mathcal{Z}$ transform of the continuous-time loop gain can be found

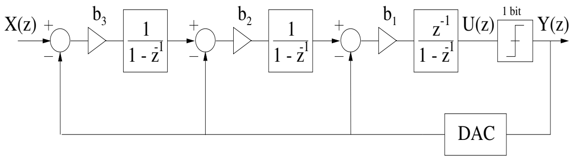

Fig. 1. *A Third Order Discrete-Time ΣΔ Modulator.*

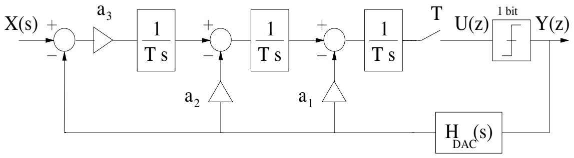

Fig. 2. *A Third Order Continuous-Time ΣΔ Modulator.*

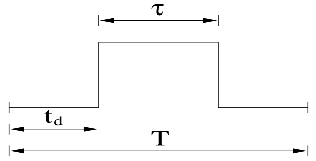

Fig. 3. *The rectangular feedback DAC pulse $H_{DAC}(s)$, (T = Sampling Period, t_d = Pulse Delay and τ = Pulse Width).*

using the modified $\mathcal{Z}$ transform technique [4]:

$$\mathcal{Z}(LG_c) = \frac{U(z)}{Y(z)} = \mathcal{Z}_{m_1}(\frac{K(s)}{s}) - \mathcal{Z}_{m_2}(\frac{K(s)}{s}) \quad (1)$$

where $K(s)$ is the loop filter, $m_1 = 1 - \frac{t_d}{T}$ and $m_2 = 1 - \frac{t_d}{T} - \frac{\tau}{T}$. For the continuous-time third-order ΣΔ modulator, shown in Fig.2, we have

$$\begin{aligned} \mathcal{Z}(LG_c) &= \mathcal{Z}_{m_1}(\frac{-a_1}{Ts^2} + \frac{-a_2}{T^2s^3} + \frac{-a_3}{T^3s^4}) \\ &- \mathcal{Z}_{m_2}(\frac{-a_1}{Ts^2} + \frac{-a_2}{T^2s^3} + \frac{-a_3}{T^3s^4}). \quad (2) \end{aligned}$$

The loop gain of the discrete-time ΣΔ modulator, shown in Fig.1, can directly be found to be

$$\begin{aligned} \mathcal{Z}(LG_d) &= \frac{(-b_1b_2b_3 - b_1b_2 - b_1)z^{-1}}{(1-z^{-1})^3} \\ &+ \frac{(b_1b_2 + 2b_1)z^{-2} - b_1z^{-3}}{(1-z^{-1})^3}. \quad (3) \end{aligned}$$

By equating Eqn.(2) and Eqn.(3), and by taking $t_d = \frac{1}{4}T$ and $\tau = \frac{3}{4}T$, the coefficients a_3, a_2 and a_1 are found to be

$$\begin{aligned} a_3 &= 1.333 b_1 b_2 b_3 \\ a_2 &= 1.5 b_1 b_2 b_3 + 1.333 b_1 b_2 \\ a_1 &= 0.646 b_1 b_2 b_3 + 0.833 b_1 b_2 + 1.333 b_1. \end{aligned} \quad (4)$$

The discrete-time coefficients were chosen from [5]: $b_3 = 0.2$ and $b_2 = b_1 = 0.5$. Substituting in Eqn.(4), yields $a_3 = 0.0667$, $a_2 = 0.4083$ and $a_1 = 0.9073$.

III. Circuit Design

Fig.4 shows one integrator-DAC pair used in the realization of the third order current mode $\Sigma\Delta$ modulator. The current-mode integrator [6], is composed of six branches, each branch having a biasing current of I. The DAC consumes $\frac{I}{2} *$ *feedback coefficient*. Except for the first integrator, whose biasing current is determined by the dynamic range requirements, the biasing currents of the second and third integrator are determined only by their corresponding gain factor. This means that any reduction in the integrators gain or the feedback coefficient will significantly reduce power consumption. One way, to achieve this, is to introduce a gain factor of 1/4 in the last integrator. This gain should not modify the behavior of the $\Sigma\Delta$ modulator, since it is followed by a comparator with a very large gain. By rearranging this gain over the other integrators and feedback coefficients, the second integrator would have a gain factor of 1/2 and the modified coefficients would be

$$\begin{aligned} a_{3m} &= \frac{a_3}{2} = 0.0333 \\ a_{2m} &= \frac{a_2}{2} = 0.2042 \\ a_{1m} &= \frac{a_1}{4} = 0.2268. \end{aligned} \quad (5)$$

This modified architecture for reduced power consumption is shown in Fig.5. Due to the additional 1/2 gain in the first integrator, the second integrator can now be biased with $I/2$. Similarly, with the 1/2 gain in the second integrator, the third integrator is now biased with $I/4$. This method has roughly halved power consumption.

A. The Integrator

The integrator circuit is depicted in Fig.4. Neglecting output conductances and parasitic capacitances, and assuming identical transistors, small-signal analysis of this circuit yields the following input-output relation:

$$i_{op} - i_{on} = \frac{g_m}{sC}(i_{ip} - i_{in}). \quad (6)$$

From the above expression, and from the modified coefficients given in Eqn.(5) and shown in Fig.5, we can see that, for proper operation of the modulator,

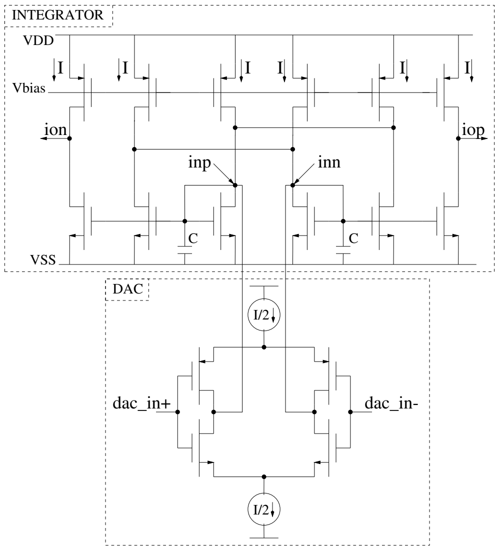

Fig. 4. *The Fully-Balanced Current-Mode Integrator and The Feedback DAC. (All integrator's transistors are cascoded, but not shown here for simplicity).*

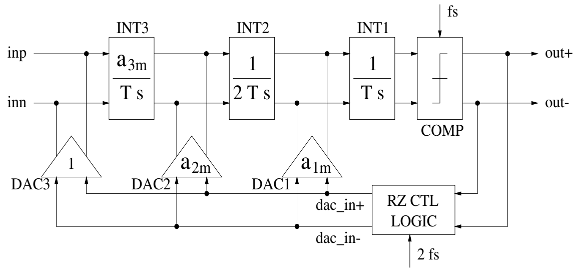

Fig. 5. *The Differential Third-Order $\Sigma\Delta$ Modulator.*

the following conditions must be satisfied:

$$\begin{aligned} \text{For INT3:} \quad \frac{g_m}{C} &= \frac{a_{3m}}{T} \\ \text{For INT2:} \quad \frac{g_m}{C} &= \frac{1}{2T} \\ \text{For INT1:} \quad \frac{g_m}{C} &= \frac{1}{T}. \end{aligned} \quad (7)$$

In a low power design, we would like the transconductance g_m to be as small as possible, in order to have a low biasing current I. From the above relations, we see that a small g_m will necessarily mean a small integrating capacitance C. On the other hand, the value of C of the first integrator INT3 must be chosen carefully to satisfy the dynamic range requirements.

In the following section, we will present a design procedure used to find the minimum integrating capacitance C required to achieve a given dynamic range. Starting from this capacitance C we can find the transconductance g_m for each integrator and the corresponding biasing current I.

B. Thermal Noise

Assuming that cascode transistors in the integrator and the current sources in the DAC have negligible effect on input reffered thermal noise, the power spectral density of thermal noise at the integrator input can be expressed by

$$S_i = \frac{\overline{i_{in}^2}}{\Delta f} = \frac{2}{3}[6(g_{mn} + g_{mp})_{int}]4KT + \frac{2}{3}[2(g_{mn} + g_{mp})_{dac}]4KT. \quad (8)$$

In the derivation of the input reffered thermal noise we will make use of the following approximations:

$$g_{mn_{int}} = g_{mp_{int}} = g_{m_{int}}$$
$$g_{mn_{dac}} = g_{mp_{dac}} = g_{m_{dac}}.$$

In the return-to-zero phase, we have $I_{int} = 4 * I_{dac_{pair}}$, and by taking $(V_{gs} - V_t)_{int} = 2*(V_{gs} - V_t)_{dac}$ Then we can say that: $g_m = g_{m_{int}} \approx 2 * g_{m_{dac}}$. By subtitution in Eqn.(8), we get

$$S_i = \frac{\overline{i_{in}^2}}{\Delta f} = \frac{28}{3} * g_m * 4KT. \quad (9)$$

The input referred noise power is given by

$$\overline{i_{in}^2} = S_i * \text{Signal Bandwidth} = S_i * \frac{f_s}{2OSR}. \quad (10)$$

Substituting in the above relation, S_i by Eqn.(9) and since $f_s = \frac{1}{T} = \frac{1}{a_{int}}\frac{g_m}{C}$ where a_{int} is the gain of the first integrator, then we can express the input reffered noise power by

$$\overline{i_{in}^2} = \frac{14}{3}\left(\frac{1}{a_{int}}\frac{g_m^2}{C}\right)\frac{4KT}{OSR}. \quad (11)$$

The dynamic range is expressed by

$$DR = \frac{m^2 I^2/2}{\overline{i_{in}^2}} \quad (12)$$

where m is the modulation index. By substituting Eqn.(11) into Eqn.(12) and since $I = \frac{g_m}{2}(V_{gs} - V_t)_{int}$, we get

$$DR = \frac{a_{int} m^2 C (V_{gs} - V_t)^2 OSR}{\frac{112}{3} * 4KT}. \quad (13)$$

In Eqn.(13) we can see the different design parameters that can be used to obtain the required dynamic range. The oversampling ratio OSR is determined by system requirements to reduce in-band quantization noise. The effective gate-source voltage $(V_{gs} - V_t)_{int}$ is optimized for the cascode structure to maximize the modulation index m of the integrator. The coefficient a_{int} is derived from the discrete-time modulator coefficients as seen in section II, for the third order system described in this paper $a_{int} = a_{m3} = 0.0333$. It is obvious that the small value of a_{int} has drastically reduced the dynamic range. This important reduction will have to be compensated by increasing the value of the integrating capacitor C.

C. The Return-to-Zero DAC

In Fig.4, we can also see the feedback DAC which is composed of two equal switched current sources. One PMOS current source switched using a PMOS differential pair and the other is an NMOS current source switched using an NMOS differential pair. The advantage of this structure is that the switching occurs smoothly and with minimum glitches because the current sources are always drawing current, either to the positive branch, the negative branch or to both branches during the return-to-zero phase. The disadvantage of this structure is the mismatch between the NMOS and PMOS current sources, but in single bit $\Sigma\Delta$ modulators, this mismatch should not influence the linearity of the modulator. During the return-to-zero phase, a return-to-zero control logic connects the positive and negative inputs of the DAC to the same potential, otherwise DAC inputs are connected to $+V_{ref}$ or $-V_{ref}$, depending on the modulator's digital output. For high speed operation, $\pm V_{ref}$ is chosen to be of small amplitude around zero, so that the DAC does not leave the linear region of operation.

D. The Comparator

The comparator circuit used, shown in Fig.6, is close to the comparator presented in [7]. Transistors $M1 - M4$ form a traditional CMOS cross coupled latch. In order to obtain a faster response time, this structure is different from [7] in that NMOS and PMOS transistors are interchanged. The reason behind this is to be able to connect bulk to source in M1 and M2 and then have lower threshold voltage than NMOS transistors with bulk connected to Vss. $M5$ and $M6$ are operating in the linear region.

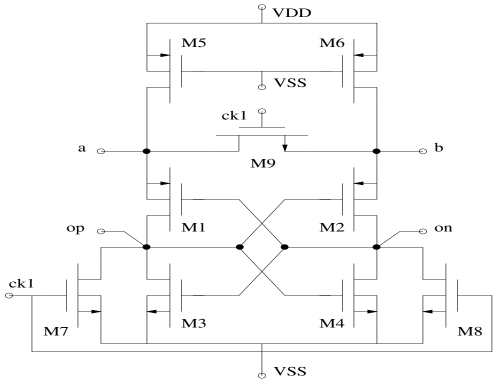

Fig. 6. *The Differential Current-Mode Comparator.*

They bias the input nodes a and b to the same potential as the output nodes of the integrator. During the reset phase, $M9$ forces the comparator's input nodes a and b to equal potentials. $M7$ and $M8$ are used to reset the ouput nodes o_p and o_n respectively.

IV. Circuit Implementation

A third order continuous-time $\Sigma\Delta$ modulator, with an oversampling ratio of 128 is implemented using the integrator shown in Fig.4. A cascode configuration is used to obtain the required high DC-gain and to reduce harmonic distortion due to output conductance error. Maximum modulation index is obtained for $V_{gs} - V_t = 0.28$. Behavioral simulation of the modulator has shown that maximum signal to noise ratio is obtained for an input signal of $I/2$. The required dynamic range, over a frequency band of 100kHz, is 84dB. Using Eqn.(13), the integrating capacitance that achieves this dynamic range is 2200pF (external capacitor). The required sampling frequency is 25.6MHz, by substituting in Eq.(7), we can deduce the transconductance $g_m = 0.002$. To obtain this transconductance, the biasing current of the first integrator should be equal to $285\mu A$.

Care must be taken in the realization of the clock signal. A previous study [8], has shown that in order to obtain 84dB of SNR a clock signal with less than 0.02% jitter has to be used.

V. Simulation Results

To study the influence of the integrator's circuit on the system performance, the third order $\Sigma\Delta$ modulator, shown in Fig.5, was simulated using ideal models for all elements except the integrators. The power spectral density of the resulting output is shown in Fig.7. The signal-to-noise ratio is 89dB, which means the SNR will be limited by thermal noise. As expected in a differential structure, we can see from Fig.7, that even harmonics are attenuated and a third harmonic distortion is dominant with an amplitude of -90dB. It should be noted that mismatch between current mirrors of the integrators has not been taken into consideration in this simulation.

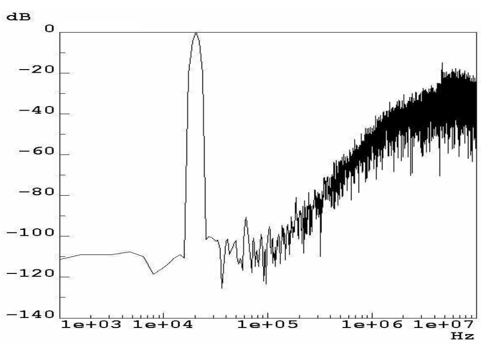

Fig. 7. *The Power Spectral Density of The Third Order $\Sigma\Delta$ Modulator with Ideal Models for all Elements Except The Integrators (Input Signal = $I/2$, 16384 pts FFT).*

TABLE I

Circuit Characteristics

Supply Voltage	1.7 V
Sampling Frequency	25.6 MHz
Signal Bandwidth	100 kHz
Expected SNR	84 dB
Power Consumption	7.4 mW
Technology	0.35μm CMOS

The characteristics and expected performances of the realized third-order continuous-time $\Sigma\Delta$ modulator are summarized in Table I.

VI. Conclusion

A systematic method has been used to derive integrators gain and feedback coefficients for a third order continuous-time $\Sigma\Delta$ modulator with delayed return-to-zero feedback. A design method for a current-mode continuous-time integrator has been detailed to find the minimum biasing current required in the integrators to achieve the desired dynamic range. Using these methods, a third order continuous-time $\Sigma\Delta$ modulator has been designed in a 0.35μm CMOS technology. Although the integrating capacitance had to be very large to satisfy dynamic range requirements, the low power consumption of the modulator still makes the proposed circuit interesting.

References

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