A CURRENT-MODE CONTINUOUS-TIME ΣΔ MODULATOR WITH DELAYED RETURN-TO-ZERO FEEDBACK

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Abstract—

In this paper, a design method for continuous-time ΣΔ modulators with RZ feedback pulse is proposed. This method is used to design a second-order continuous-time ΣΔ modulator. The circuit is realized using continuous-time current-mode integrators and switched-current sources DAC. The effect of the integrator thermal noise and non-ideal RZ feedback pulse on the system performance is studied. An analog layout language was used to generate the complete layout of the modulator in a 0.6μm CMOS process. With a sampling frequency of 26MHz, the circuit is expected to achieve 80 dB of Dynamic Range for a 200kHz bandwidth input signal. The circuit operates from a power supply of ±1.65V with a power consumption of 9.1mW and occupies an area of 0.348mm^2.

I. Introduction

Currently, the popularity of continuous-time ΣΔ modulators is increasing due to some important advantages they have over the well-known discrete-time ΣΔ modulators. Recently, continuous-time modulators with higher sampling rate [1], lower power consumption [2], and lower thermal noise [3] than their discrete-time counterparts, have been reported. Additional advantages of continuous-time ΣΔ modulators are inherent anti-aliasing filtering [2], reduced sampling errors, and the fact that they are well suited for realization in other technologies (such as bipolar or GaAs).

However, continuous-time ΣΔ modulators with non-return-to-zero (NRZ) feedback signal suffer from harmonic distortion due to the asymmetry in the waveform of the DAC output signal [4]. At high sampling frequencies, signal dependent quantizer delay increases the noise floor in the band of interest [1] and excess loop delay causes Signal-to-Noise Ratio (SNR) degradation [5].

Digital-to-Analog converters with return-to-zero (RZ) eliminate the correlation between the input signal and the amount of current fed back. This correlation is the main source of harmonic distortion in NRZ DACs with asymmetric waveforms. If the DAC output is set to zero at the beginning of each cycle, the quantizer will have enough time to settle and the loop delay will be absorbed.

In Section II of this paper, a design method for continuous-time ΣΔ modulators is proposed. The circuit design of the several building blocks and the effects of both thermal noise and non-ideal RZ feedback pulse on the system performance are described in Section III. Section IV presents simulation results of the implemented circuit and discusses clock jitter and layout. The conclusion is given in section V.

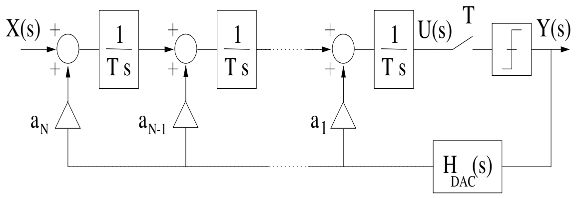

Fig. 1. *A general structure of an Nth order single-bit continuous-time ΣΔ modulator.*

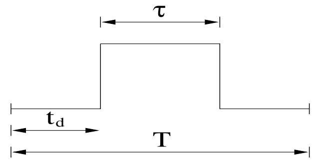

Fig. 2. *The rectangular feedback DAC pulse $H_{DAC}(s)$.*

II. System Design

A general low-pass continuous-time ΣΔ modulator is shown in Fig.1. It is formed by a cascade of integrators whose transfer function is $\frac{1}{Ts}$, where T is the sampling period. The digital-to-analog converter output signal is supposed to be rectangular with a pulse-width τ and delayed by t_d with respect to the sampling instant, Fig.2. In order to obtain the coefficients $a_1, a_2, ..., a_N$, we first find the $\mathcal{Z}$ transform of the continuous-time ΣΔ loop gain and then equate it to the loop gain of the equivalent discrete-time ΣΔ modulator. The $\mathcal{Z}$ transform of the continuous-time loop-gain is given by

$$\mathcal{Z}(L.G) = \mathcal{Z}[K(s)H_{DAC}(s)] \tag{1}$$

where $K(s)$ and $H_{DAC}(s)$ are the loop filter and the DAC transfer functions respectively. The rectangular feedback DAC pulse, shown in Fig.2, can be described in the time domain by the following relationship :

$$h_{dac}(t) = u(t - t_d) - u(t - t_d - \tau) \tag{2}$$

By applying the Laplace transform to (2) we get

$$H_{DAC}(s) = \frac{e^{-t_d s} - e^{-(t_d+\tau)s}}{s} \tag{3}$$

Substituting (3) into (1), yields

$$\mathcal{Z}(L.G) = \mathcal{Z}[K(s)(\frac{e^{-t_d s} - e^{-(t_d+\tau)s}}{s})] \tag{4}$$

$\mathcal{Z}(L.G)$ can be found using the modified $\mathcal{Z}$ transform technique [6]

$$\mathcal{Z}(L.G) = \mathcal{Z}_{m_1}(\frac{K(s)}{s}) - \mathcal{Z}_{m_2}(\frac{K(s)}{s}) \tag{5}$$

where m_1 and m_2 are defined such that $t_d = (1-m_1)T$ and $t_d+\tau = (1-m_2)T$. For the general structure, shown in Fig.1, the loop filter transfer function can be defined by

$$K(s) = \frac{a_1}{Ts} + \frac{a_2}{T^2s^2} + ... + \frac{a_N}{T^N s^N} \tag{6}$$

In the special case of a second-order system, the loop filter is reduced to

$$K(s) = \frac{a_1}{Ts} + \frac{a_2}{T^2s^2} \tag{7}$$

Therefore, in a continuous-time second-order $\Sigma\Delta$ modulator, the $\mathcal{Z}$ transform of the loop gain is given by

$$\mathcal{Z}(L.G) = \mathcal{Z}_{m_1}(\frac{a_1}{Ts^2} + \frac{a_2}{T^2s^3}) - \mathcal{Z}_{m_2}(\frac{a_1}{Ts^2} + \frac{a_2}{T^2s^3}) \tag{8}$$

Using table II given in the appendix, and equating the above relation to the loop gain of a second-order discrete-time $\Sigma\Delta$ modulator, given by $(-2z^{-1}+z^{-2})/(1-z^{-1})^2$, the coefficients a_1 and a_2 are found to be

$$a_1 = -\frac{1}{2} - \frac{t_d}{\tau} - \frac{T}{\tau} \ , \ a_2 = -\frac{T}{\tau} \tag{9}$$

For the NRZ case ($\tau = T$ and $t_d = 0$), the above relations will give the same results as those obtained by Candy in [7] : $a_1 = -1.5$ and $a_2 = -1$. Eq. (9) gives the modulator coefficients for any desired value of τ and t_d. In our system, we have chosen $t_d = \frac{1}{4}T$ and $\tau = \frac{3}{4}T$, which can be realized by using a DAC clock frequency equal to twice the sampling frequency. The corresponding coefficients for these values of t_d and τ are $a_1 = -\frac{13}{6}$ and $a_2 = -\frac{4}{3}$.

III. Circuit Design

The differential structure for a second-order $\Sigma\Delta$, shown in Fig.3, has been implemented using two fully-balanced current-mode integrators, a differential current comparator and two switched-current sources RZ DACs. Current mirrors have been used to realize the feedback coefficients.

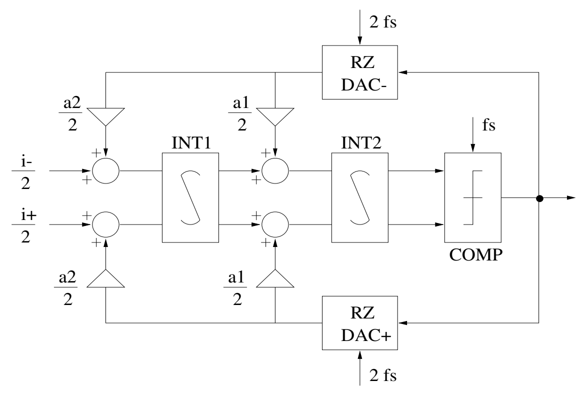

Fig. 3. *A Differential Second-Order $\Sigma\Delta$ Modulator.*

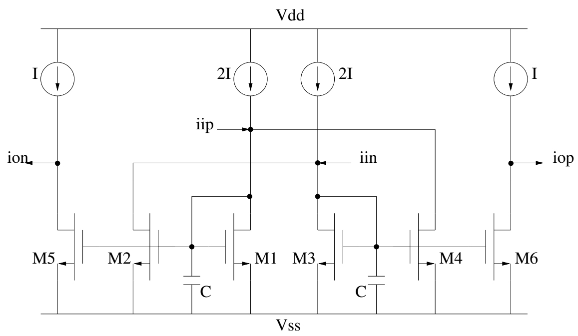

Fig. 4. *A Fully-Balanced Current-Mode Integrator.*

A. The Integrator

The integrator circuit is depicted in Fig.4 [8]. Neglecting output conductances and parasitic capacitances, and assuming identical transistors, small-signal analysis of this circuit yields the following input-output relation :

$$i_{op} - i_{on} = \frac{g_m}{sC}(i_{ip} - i_{in}) \tag{10}$$

From the above expression, we can see that, for proper operation of the modulator, the following condition has to be satisfied : $\frac{g_m}{C} = \frac{1}{T}$. Small signal analysis of Fig. 4 including g_{ds} and C_{gd} gives

$$i_{op} - i_{on} = A_0 \frac{(1 - \frac{s}{z_1})}{(1 + \frac{s}{p_1})}(i_{ip} - i_{in}) \tag{11}$$

where

$$z_1 = \frac{(g_m - g_{ds})}{2C_{gd}} \ , \ p_1 = \frac{2g_{ds}}{(C + 4C_{gd})} \ \ and \ \ A_0 = \frac{g_m - g_{ds}}{2g_{ds}}$$

As a rule of thumb, the DC-gain of the integrators in $\Sigma\Delta$ modulators needs to be greater than or approximately equal to the oversampling ratio ($A_0 \geq \frac{f_s}{2B_0}$). A cascode configuration was used to obtain the required DC-gain (A_0) and to reduce harmonic distortion due to output conductance error.

B. Thermal Noise

The first integrator in a $\Sigma\Delta$ modulator is the main source of thermal noise. Assuming that the transconductances g_{mn} and g_{mp} of the NMOS and PMOS transistors in the integrator are equal, the power spectral density of thermal noise at the integrator input can be expressed by

$$S_i = \frac{\overline{i_{in}^2}}{\Delta f} = \frac{2}{3}[6(g_{mn} + g_{mp})]4KT \tag{12}$$

The input referred noise power is given by

$$\overline{i_{in}^2} = S_i f_N \tag{13}$$

where f_N is the equivalent noise bandwidth. In continuous-time single pole circuits we have $f_N = \frac{\pi}{2}f_c$, where f_c is the cut-off frequency. In $\Sigma\Delta$ A/D converters, since all signal components beyond B_0 are attenuated by the digital decimation filter, f_N is usually taken equal to B_0 [9]. Nevertheless, it can be shown that for a continuous-time integrator with $A_0 \geq \frac{f_s}{2B_0}$ the following expression is always satisfied :

$$\frac{\pi}{2} f_c < B_0 \tag{14}$$

This implies that we should take $f_N = \frac{\pi}{2} f_c$. Since $p_1 = 2\pi f_c$, then input referred noise power can be expressed by :

$$\overline{i_{in}^2} = 16 g_m KT \frac{g_{ds_{cas}}}{C + 4C_{gd}} \tag{15}$$

where $g_{ds_{cas}}$ is the output conductance of the cascode configuration. Replacing $\frac{g_m}{C}$ by the sampling frequency f_s, and taking $g_{ds_{cas}} \approx 2\frac{g_{ds}^2}{g_m}$ we get

$$\overline{i_{in}^2} \approx 32KT f_s \frac{g_{ds}^2}{g_m} \tag{16}$$

An expression can be obtained for the Dynamic Range

$$DR = \frac{m^2 I^2/2}{\overline{i_{in}^2}} \approx \frac{m^2 I L^2 V_E^2}{32KT f_s (V_{gs} - V_t)} \tag{17}$$

where m is the modulation index, L is the transistor's length and V_E is the Early effect coefficient. Eq. 17 is an important design equation. Using this equation, we can determine the minimum biasing current, I, required to achieve the desired dynamic range and sampling frequency.

C. Return-To-Zero DAC

The return-to-zero DAC, shown in Fig.5, is composed of two switched current sources ($-I_{ref}$) and a continuous current source ($+I_{ref}$). By proper control of the gate voltage of MN2 and MN3 we can obtain at the output 2 levels, $+I_{ref}$ and $-I_{ref}$. The zero is obtained by activating only one negative source ($+I_{ref} - I_{ref} = 0$) [10]. Due to the mismatch between positive and negative current sources, the difference is not an exact zero and an offset is present during the return-to-zero interval. A single-ended second-order $\Sigma\Delta$ modulator using this DAC has been simulated and the power spectral density is shown in Fig.6(a). To observe the DAC circuit effect on the system linearity, independently from other sources of non-linearity, ideal blocks were used to model the integrators and the comparator. As we can see from Fig.6(b), the use of a differential structure has attenuated harmonic distortion compared to the single-ended structure.

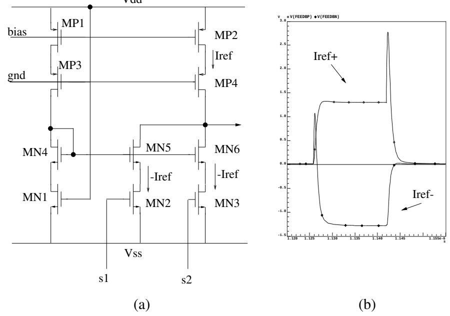

Fig. 5. *(a) Switched-Current Sources RZ DAC. (b) Simulated Output Signal Waveforms.*

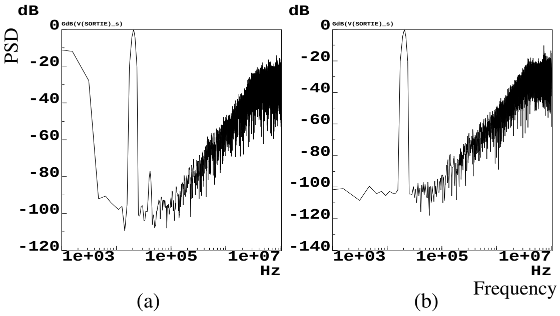

Fig. 6. *The power Spectral Density of a Second-Order $\Sigma\Delta$ Modulator with Ideal Models for all Elements Except the Feedback DACs. (a) Single Ended. (b) Differential.*

D. Comparator

The requirements on the comparator are relaxed due to the use of a delayed RZ DAC. The zero at the beginning of each period gives enough time for the quantizer to settle. The comparator circuit used [11], achieves settling-time of less than 2ns.

IV. Circuit Implementation

For a biasing current of $I = 100\mu$A in the integrators, the maximum input level is limited to $\frac{i}{2} = 13\mu$A (see Fig.3). The current mirrors in the feedback provide $\frac{a_1}{2} = 30\mu$A and $\frac{a_2}{2} = 20\mu$A. To obtain the required integrator constant, the value of the capacitance should be set to $C = 26$pF in each integrator. Table I summarizes the characteristics and the expected performances of the second-order continuous-time $\Sigma\Delta$ modulator.

TABLE I
Circuit Characteristics

Supply Voltage	3.3V
Sampling Frequency	26MHz
Signal Bandwidth ($2B_0$)	200kHz
OSR	128
Integrator DC gain	58dB
Signal-to-Quantization Noise Ratio	82dB
Signal-to-Thermal Noise Ratio (DR)	84dB
Power Consumption	9.1mW
Technology	0.6μm
Area	0.348mm^2

A. Clock Jitter

Care must be taken in the realization of the clock signal ; a previous study, concerning clock-jitter effects on continuous-time $\Sigma\Delta$ modulators [12], has shown that the Signal to Jitter-Noise Ratio (SNR_J) in a continuous-time $\Sigma\Delta$ modulator can described by the following relation :

$$SNR_J = 10 \log \frac{\alpha^2/2}{\delta\tau^2/\tau^2} OSR \tag{18}$$

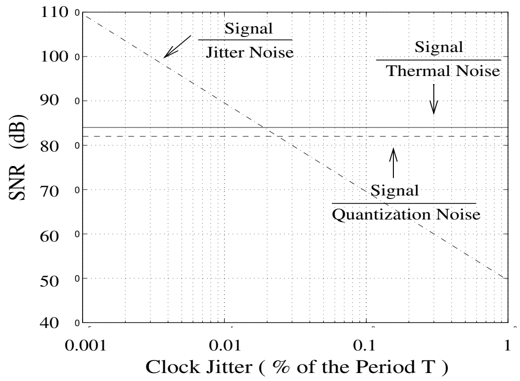

Fig. 7. *SNR_Q, SNR_{Th} and SNR_J against pulse-width clock jitter.*

where α is the amplitude of the input signal and $\overline{\delta\tau^2}$ is the DAC's pulse-width jitter. Eq. 18 is plotted in Fig. 7, along with the Signal to Quantization-Noise Ratio (SNR_Q) and the Signal to Thermal-Noise Ratio (SNR_{Th}) of a second-order modulator with the characteristics shown in table I. Fig. 7 shows that, in order to obtain a total signal to noise ratio (SNR) higher than 82 dB, a clock with less than 0.02% jitter has to be used.

B. Layout

The complete layout of the modulator in a 0.6 μm technology is shown in Fig.8. It has been automatically generated using the analog layout language CAIRO [13]. The language contains a parametrized device library that relies on the symbolic layout approach. This approach is used in the ALLIANCE VLSI CAD system to achieve technology independence. The user code describes the relative device and sub-circuit placement in horizontal and vertical slices, as well as the required routing in a completely hierarchical structure. Layout is generated by using as inputs : the user's code, the circuit netlist, the shape parameter and process technology information. Little effort is then required to generate new layouts for different technologies or new modulators with modified specifications. The layout produced is completely symmetric as shown in Fig.8.

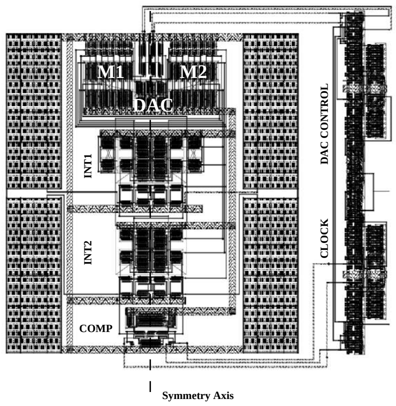

Fig. 8. *The Layout Generated using CAIRO.*

V. Conclusion

A simple design method, based on the modified $\mathcal{Z}$ transform technique, can be used to calculate the feedback coefficients for RZ continuous-time $\Sigma\Delta$ modulators. A second-order continuous-time $\Sigma\Delta$ modulator with RZ feedback has been implemented in a 0.6μm technology. The modulator is expected to achieve 12 bits of resolution for a signal bandwidth of 200kHz and a sampling frequency of 26MHz.

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Appendix

TABLE II

Modified $\mathcal{Z}$ transform

$\mathcal{Z}_m(\frac{1}{s^2})$	$\frac{mTz^{-1}}{1-z^{-1}} + \frac{Tz^{-2}}{(1-z^{-1})^2}$
$\mathcal{Z}_m(\frac{1}{s^3})$	$\frac{T^2}{2}[\frac{m^2z^{-1}}{1-z^{-1}} + \frac{(2m+1)z^{-2}}{(1-z^{-1})^2} + \frac{2z^{-3}}{(1-z^{-1})^3}]$

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