RAIL-TO-RAIL OPERATION OF VERY LOW VOLTAGE CMOS SWITCHED-CAPACITOR CIRCUITS

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ABSTRACT

A circuit that allows switch operation down to very low voltages in standard CMOS technologies is proposed. The circuit is an extension of the gate-source bootstrapping technique such that rail-to-rail operation of a single *n*-switch becomes possible. Architecture modifications introduced in a standard switched-capacitor circuit reduce the number of critical switches to only one switch per opamp plus one at the circuit input. Simulations show the usefulness of the proposed configuration down to 0.9 V.

1. INTRODUCTION

In any switched-capacitor circuit, the input switch, as well as switches at all opamp outputs, are required to switch the whole signal range. At very low supply voltages, complementary CMOS switches are not suitable any more for switching rail-to-rail analog signals. This is due to a gap which appears in the middle of the input voltage range, where both transistors enter weak-inversion as shown in Fig. (1). This results in very high switch on-resistance and makes switched-capacitor circuits unpractical. In order to avoid the use of expensive multithreshold processes, one technique to overcome this problem is supply or clock-voltage multiplication [1]. This however is not power efficient and not compatible with very advanced low-voltage CMOS processes where gate oxide breakdown becomes an issue. Alternatively, the switched-opamp technique [2] has been proposed to get around this problem. However, the switch connected to the input of the circuit remains, and it restricts severely the maximum allowable amplitude of the input signal. The switching of the opamp may also affect the speed of the circuit. This results in relatively poor performance of the switched-opamp circuits. This paper proposes a rearrangement of the bias levels in switched-capacitor circuits similar to [3] reducing the number of critical switches alongside with the application of a gate-voltage boosting scheme [4] to the few remaining ones. The gate-voltage boosting scheme is fully compatible with low-voltage CMOS processes and allows the signal to swing from rail-to-rail while requiring minimal extra hardware. The extra power consumption due to added circuitry is negligible. The proposed technique is readily applicable to switched-capacitor circuits as illustrated with a second order low-pass filter.

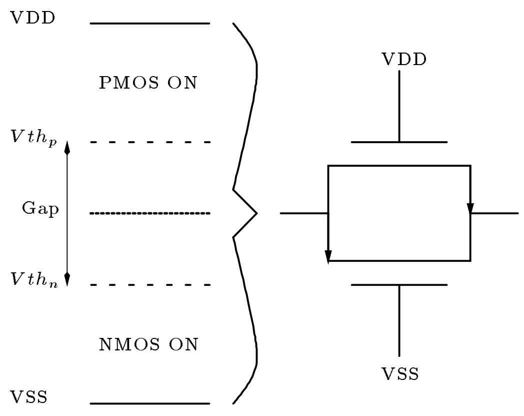

Figure 1. CMOS switch operating at rail-to-rail.

2. PROPOSED VGS BOOSTING CIRCUIT

Fig. (2) shows the well known gate-source bootstrapping technique [5]. It shows the signal switch MNSW together with five additional switches (S1-S5) and an additional capacitor C_{offset}. Switches S3 and S4 charge the capacitor during ϕ_2 to VDD. During ϕ_1 switches S1 and S2 add the pre-charged capacitor in series with the input voltage v_{in} such that the gate-source voltage of transistor MNSW is equal to the voltage V_C ($\approx VDD$) across the capacitor. This guarantees maximum switch conductance independently of v_{in}. Switch S5 fixes the gate voltage of MNSW to VSS during ϕ_2 to make sure that the transistor is in the OFF state.

The transistor level implementation is shown in Fig. (3). Transistors MN1, MP2, MN3, MP4 and MN5 correspond to

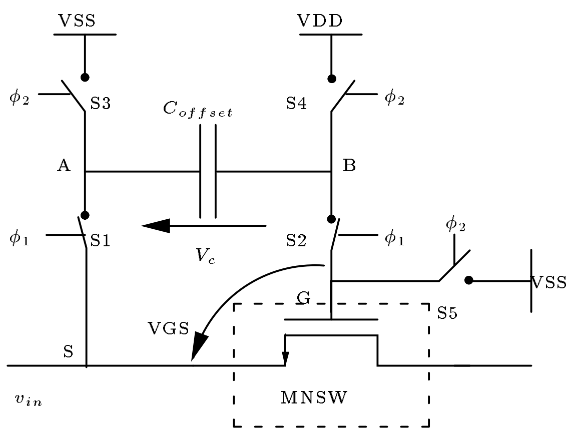

Figure 2. Basic circuit.

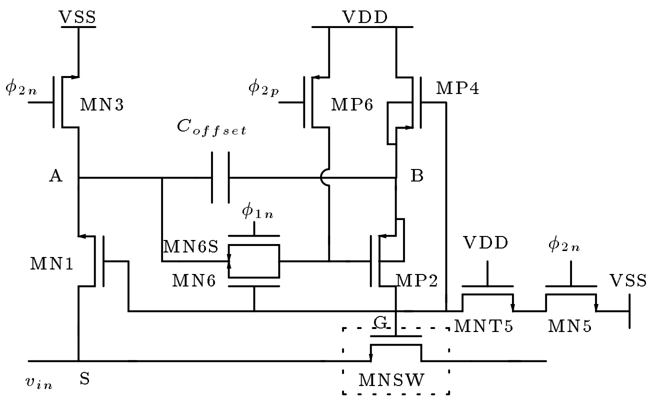

Figure 3. Proposed implementation.

the five ideal switches S1-S5 shown in Fig. (2) respectively. Additional transistors and modified connectivity shown in Fig. (3) were introduced to extend all switch operation from rail to rail while limiting all gate-source voltages to VDD [4]. It is evident that the worst case input signal (with respect to switch operation) is that of $v_{in} = VDD$, which is the value attributed to v_{in} in the discussion hereafter.

An apparent problem is that of the n-transistor MN1 which has to switch VDD. This is the same problem as that of MNSW. The gate of MN1 is tied to that of MNSW where a gate-source potential of VDD assures its high conductivity during ϕ_1. The gate potential then drops to zero during ϕ_2 to cutoff both transistors.

Additional critical problems arise on nodes B and G as their voltages reach $2VDD$: First of all, transistor MP4 must remain OFF during ϕ_1 in order not to loose the charge stored on C_{offset} during ϕ_2. If the clock is used to drive it as shown in Fig. (2), its gate-source voltage would be $-VDD$ and the transistor can't be turned OFF. That's why its gate is connected to node G which provides a voltage of $2VDD$ during ϕ_1 cutting-off the transistor, and a voltage of VSS during ϕ_2 which ensures its high conductivity.

Secondly, transistor MP2 has a technological problem. Using the clock to drive it as shown in Fig. (2), its gate-source voltage would be $-2VDD$ during ϕ_1. In Fig. (3) a solution to this problem is proposed; Transistor MN6 is used to connect the gate of MP2 to node A thus keeping its gate-source voltage equal to $-VDD$ (the voltage across C_{offset}) during ϕ_1. During ϕ_2 transistor MP6 connects it to VDD turning it OFF.

The gate of the n-transistor MN6 is tied to node G to keep it conducting as the voltage on node A rises to VDD during ϕ_1. There is thus a dependency loop inhere; In to turn on MN6, it must have a sufficient gate-source voltage i.e. MP2 must then be conducting!. Transistor MN6S is then necessary as a startup to force transistor MP2 to conduct. The clock is used to drive MN6S as it is assumed to conduct only when the voltage of node A is close to zero (which is the case at the beginning of ϕ_1). When MP2 conducts, the voltage on node G rises to $2VDD$ while that on node A rises to VDD; thus MN6S turns OFF while MN6 remains ON.

Lastly, transistor MNT5 has been added in series with MN5 in order to prevent the gate-drain voltage of the latter from reaching $2VDD$ during ϕ_1. The bulk of MNT5 is however tied to VSS. During ϕ_1 when it is OFF, its drain-bulk diode junction voltage reaches a reverse bias voltage of $2VDD$. This must be compatible with the technology limits.

It should be noted that for an NWELL process, the bulk of transistors MP2 and MP4 must be tied to the highest potential i.e. node B, and not to VDD.

3. MODIFIED SWITCHED-CAPACITOR CIRCUIT ARCHITECTURE

Fig. (4) shows a low-pass biquad that uses the circuit described in the previous section to drive the input switch MNS11 as well as the switches MNS21 and MNS31 at the opamp outputs. The bootstrap circuit is always connected between the gate and the terminal of the transistor having the lower voltage, such that when the gate voltage is raised by VDD with respect to this terminal, the voltage between the gate and the other terminal remains below VDD. In addition to enabling those transistors to pass rail-to-rail signals, the bootstrap circuit maximizes the gate-source voltage and keeps it constant during the ON-phase, thus eliminating completely signal dependent nonlinearity due to variable switch resistance.

The opamp input common mode is held at zero while the output common mode is set to $VDD/2$. The voltage difference between the input and output is compensated by injecting a fixed amount of charge at the opamp input at each clock cycle. Thus all switches other than MNS11, MNS21 and MNS31 are connected either to ground (and realized with NMOS) or to VDD (and realized with PMOS) [3]. This allows the simultaneous optimization of switch operation and output swing.

Capacitor C_{CM1} has then been added together with switches MNS17 and MPS17 in order to reduce the charge injected at the opamp input virtual ground to zero in steady state. This charge is equal to

$$\begin{aligned} Q_{inj} &= C_{14}VDD/2 - C_{12}VDD/2 \\ &\quad -C_{10}VDD/2 + C_{CM1}VDD \end{aligned} \tag{1}$$

then by choosing

$$C_{CM1} = 0.5(C_{12} + C_{10} - C_{14}) \tag{2}$$

Q_{inj} reduces to zero.

For the second opamp, $C_{CM2} = C_{24}/2$ has been used together with switches MNS27 and MPS27 in order to reduce the charge injected at the second opamp input to zero in steady state.

Four clock phases are used: ϕ_1 and ϕ_2 as well as their delayed versions ϕ_{1d} and ϕ_{2d}. The first two phases are used to drive the transistors at the opamp inputs while the other two are used to drive the rest of the transistors. This is done to minimize the signal dependent charge injection by insuring that no charge passes to the integrating capacitors $C1$ and $C2$ during the turn OFF transient of the signal transistors.

A disadvantage of this charge compensation scheme by using extra capacitors switched between VDD and VSS is the increase of the white noise level. Another problem related to the use of VSS as a reference voltage is the negative transient spikes which might cause bulk leakage. This can take place at nodes $I1$ and $I2$. Switch sizes are adjusted in order to minimize this effect [3].

The circuit shown in Fig. (4) is simulated using an advanced transistor model (MOS Bsim3V3) and model parameters of a 0.5μ technology having a typical n- and p-transistor threshold voltage of 0.6 V. The used VDD is 1 V.

The filter is designed to have a cutoff frequency of 8 kHz and a sampling frequency of 100 kHz. An input frequency of 980 Hz is chosen in order to be able to examine the output harmonics in the filter pass-band. Source and drain junction capacitances of switches are taken into account by calculating the corresponding junction areas.

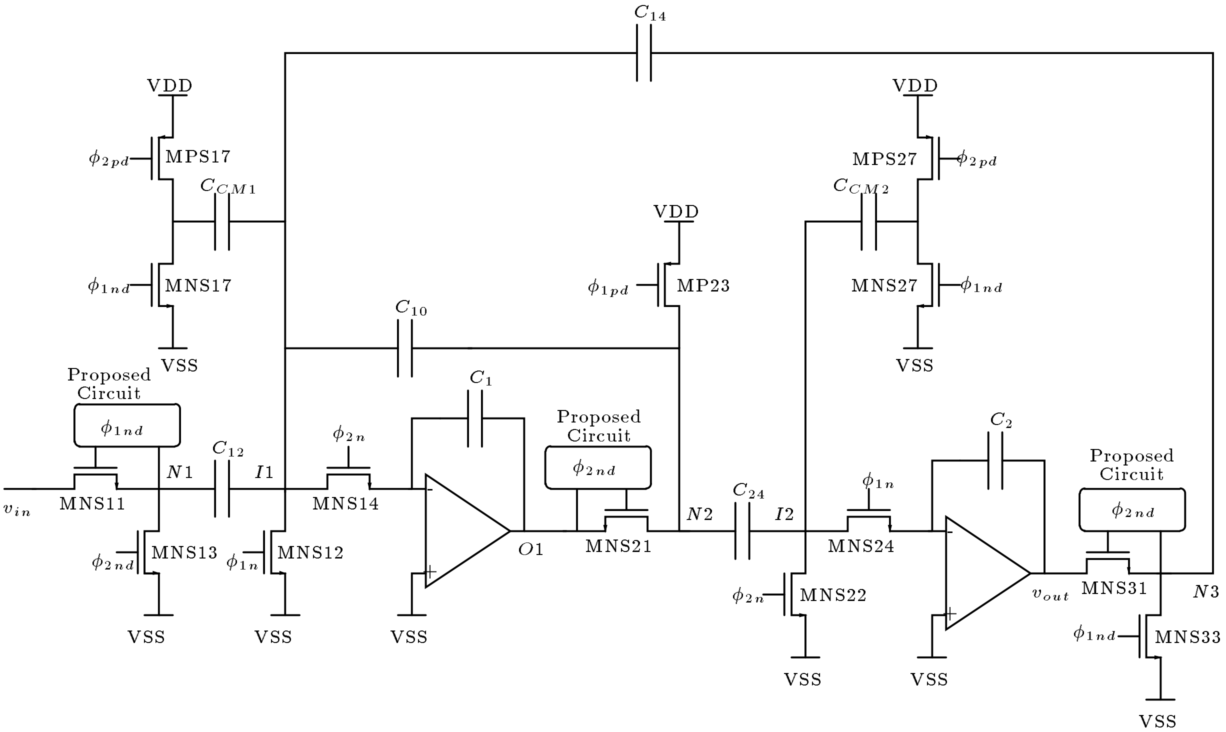

Figure 4. Modified switched-capacitor low-pass biquad.

Input (p/p)	Slow models	Typical models
1.0	-93.62	-106.60
0.5	-96.46	-102.56
0.1	-89.23	-91.41

Table 1. *Simulated results for the Total Harmonic Distortion.*

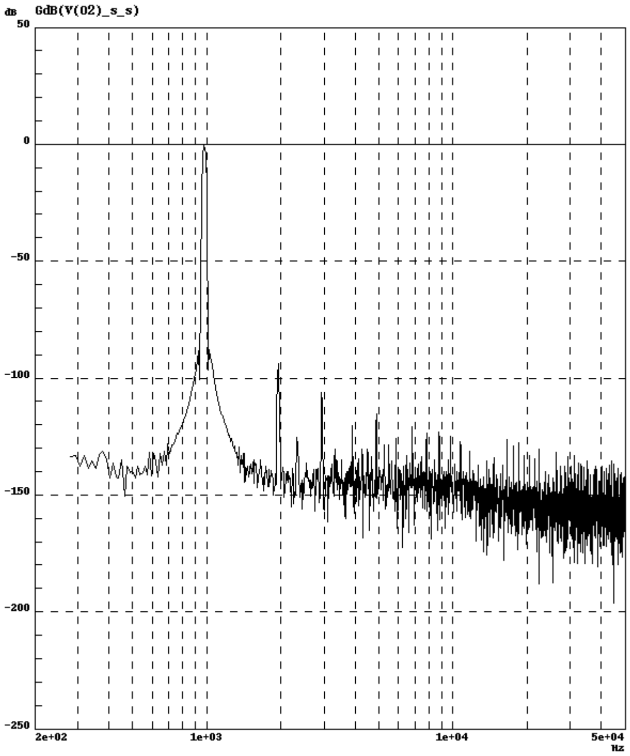

Figure 5. *Simulated output spectrum for a rail-to-rail input signal using the slow transistor parameter set.*

A one-pole opamp macro-model with a gain-bandwidth product of 1 MHz and dc gain of 100 dB is used in order to distinguish the proposed architecture influence on the filter linearity.

Table (1) shows the obtained total harmonic distortion for three different input amplitudes, as well as the same simulation repeated using the supplied process slow transistor parameter set. Fig. (5) shows the output spectrum for a rail-to-rail (1 V p/p) input signal using the slow transistor parameter set. As can be seen, the worst case distortion due to non-linear switches and charge injection is better than 90 dB for full-scale signals. This good results were to be expected as the proposed bootstrap circuit helps to maintain the switch drive at VDD, thus eliminating to a large extent the nonlinear distortion attributed to the signal dependence of the switch ON resistance.

4. CONCLUSIONS

The modified switch driver as well as the modified switched-capacitor structure allow rail-to-rail operation for very low-voltage switched-capacitor circuits. This increases the available signal-to-noise ratio and helps in reducing the power consumption. Key advantages of the proposed circuit is its simplicity, a significant increase in signal-to-noise ratio and linearity while the extra power and area requirements are very modest. It is fully compatible with advanced low-voltage CMOS as all gate-source and gate-drain voltages are limited to VDD. Simulations show robustness with respect to process parameter variations.

5. REFERENCES

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