Optimized Statistical Analog Fault Simulation

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Abstract

A new statistical method for analog fault simulation is presented. The method takes into account process parameter variations and aims to reduce the number of the computational expensive Monte Carlo simulations often required during analog fault simulation. The technique is illustrated by means of a fifth-order low-pass switched-capacitor filter.

1. Introduction

Due to the continuous expansion of the market of telecomunications, multimedia, portable systems and systems on-chip which all needs an analog interface, mixed-signal and analog integrated circuit design becomes more and more demanding. During the production phase, test is an important factor contributing significantly to the manufacturing cost [5]. Analog integrated circuit testing and diagnosis is a very challenging problem. The inaccuracy of measurements, the infinite domain of possible values and the process parameter deviations are among the major difficulties. Tools for optimizing production tests aim to reduce the test time that a given circuit spends on the expensive ATE (Automatic Test Equipement).

Before optimizing the set of production tests we have to run several fault simulations using a spice-like simulator in order to obtain the possible faults which can be detected by each test. The fault simulator runs multiple simulations to determine the set $\{Vg_i/i \in [1..n]\}$ of simulation results of the fault-free circuit and the set $\{Vf_{ij}/i \in [1..n], j \in [1..m]\}$ of simulation results of all possible faulty circuits. However, a direct use of the simulation results prove to be practically inadequate. This is mainly due to :

- Measurements are generally inaccurate because of the continuous nature of analog signals.
- Inaccurate transistor models used in the simulator.
- Analog circuit parameters are usually considered with a certain tolerance range.

For example, in figure (1) V_g and V_f represent the simulated values of the output of the fault-free and the faulty circuits respectively, D_g and D_f are their corresponding probability density function. If we compare only the simulated values we can conclude that in case (a) the fault is detected because V_g is far from V_f, while in case (b) the fault is not detected. But, if we now compare the probability density of the output values the conclusion is completely different, in case (a) the fault is not detected and in case (b) the fault is detected. This example shows that we need to compute the distribution for each faulty circuit if we want to get accurate results, this means that *statistical simulation* should be used.

Fault simulation for analog circuit have been lately considered for linear analog circuits [10] and [6], for mixed-signal circuits [2] and [7], using DC and transient analysis [14] and [15], or supply current monitoring [16]. Some trials as in [13] present a fault simulation method for analog circuits subject to process variation. To speed up the simulations, we can use concurrent analog fault simulation [16], VHDL-A language [11] and [9] or macromodels [8] and [3]. To take into account parameter deviations due to process variations, we can use either Monte Carlo simulations as in [12] and [1] or interval analysis [13]. To have a high accuracy and an accurate fault coverage in the optimization phase, we need to use Monte Carlo simulations for each faulty circuit in the fault simulation module. In this paper we propose a new technique to reduce the number of Monte Carlo simulations without degrading the accuracy of the results.

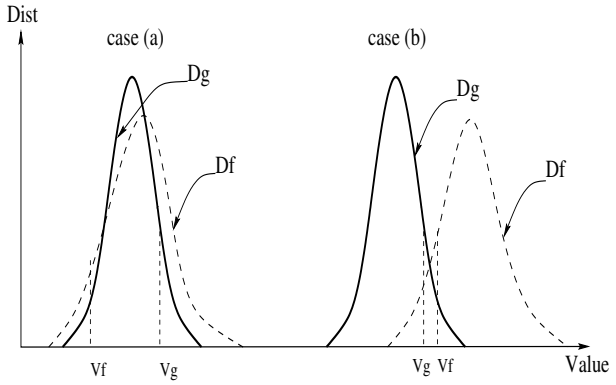

Figure 1. Comparison of simulated values of good and faulty circuits.

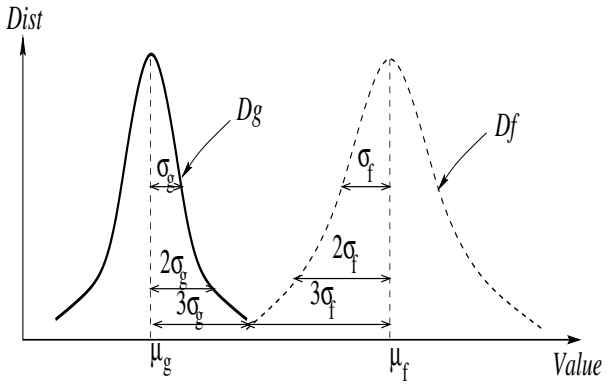

Figure 2. Probability density functions of the output of a good and a faulty circuits.

2. Fault simulation under parameter variation

2.1. Formulation

For fault simulation we need to introduce the following definitions :

- A set of tests : for test optimization we need to define a set $\mathbf{T} = \{T_1, T_2, ...T_n\}$ of n possible tests. Each test T_i is defined by an input value and a measured output. The test T_i detects a fault if and only if the measured output is different for the fault-free and the faulty circuits.

- A set of faults : we also need to define a set $\mathbf{F} = \{F_1, F_2, ...F_m\}$ of m possible faults to be detected. The set of possible faults can be extracted from the circuit layout using IFA (Inductive Fault Analysis) methods.

- For each test $T_i \in \mathbf{T}$, Vg_i is the simulated value of the output of the fault-free circuit.

- For each test $T_i \in \mathbf{T}$ and each fault $F_j \in \mathbf{F}$, Vf_{ij} is the simulated value of the output of the faulty circuit having the fault F_j.

2.2. New approach

The aim of our approach is to compute a large number of simulations only when it is really necessary (i.e. when the simulation results of the fault-free and the faulty circuits are close). For many faults, especially the catastrophic ones we don't need to make such a large number of Monte Carlo simulations to get an accurate result.

Let Dg and Df be the probability density of a given output of the fault-free and faulty circuits respectively (see figure (2)). Each distribution is defined by its mean value μ and its standard deviation σ. Depending on the required accuracy, we can define a threshold S such that :

$$(|\mu_g - \mu_f| > S) \Longrightarrow Fault\ is\ detectable \qquad (1)$$

$$\text{with } S = k * (\sigma_g + \sigma_f)\ , k \in [1, 3]$$

The factor k determines the efficiency of the fault simulation results. If k is low the probability that a good circuit will fail undergoing the test would be high and the probability that a bad circuit will pass the test would be low and vice-versa. For the normal distribution, the probability that a continuous random variable x has a value within a certain interval is given by the area under the corresponding distribution curve between the two limits of the interval. For the interval $[\mu - k\sigma, \mu + k\sigma]$ with different values of k, the probability is shown in the following table:

k	probability
1	68.26 %
2	95.44 %
3	99,74 %

We can see that for k within one, two and three standard deviations of the mean, the probability is more than 68%, 95% and 99.5% respectively. In this paper we choose $k = 2$ and $S = 2(\sigma_g + \sigma_f)$, such that according to (1) we have :

$$(|\mu_g - \mu_f| > 2(\sigma_g + \sigma_f)) \Longrightarrow Fault\ is\ detectable \quad (2)$$

and if we suppose that $(\sigma_g = \sigma_f)$ the assumption (2) becomes :

$$(|\mu_g - \mu_f| > 4\sigma_g) \Longrightarrow Fault\ is\ detectable \quad (3)$$

Let's consider that $V_f \in [\mu - 2\sigma_f, \mu + 2\sigma_f]$ is one of the simulated values of the faulty circuit, so according to assumption (2) we deduce that :

$$(|(\mu_g - V_f)| > 2\sigma_g + 4\sigma_f) \Longrightarrow Fault\ is\ detectable \quad (4)$$

and if we suppose that $(\sigma_g = \sigma_f)$ the assumption (4) becomes :

$$\boxed{(|\mu_g - V_f| > 6\sigma_g) \Longrightarrow Fault\ is\ detectable} \quad (5)$$

Assumption (5) shows that if the simulated value V_f of the faulty circuit satisfies the condition $(|\mu_g - V_f| > 6\sigma_g)$, we can deduce without computing the distribution of the faulty value and without using Monte Carlo simulation that the fault is detectable by the corresponding test.

2.3. Fault simulation algorithm

(01) **for** *each test* $T_i,\ i \in [1..n]$ **do**
(02) *compute* μ_g *et* σ_g *for the fault-free circuit*
(03) **for** *each fault* $F_j,\ j \in [1..m]$ **do**
(04) *Nstat = 0 ;*
(05) *StopSim = 0 ;*
(06) DD_{ij} *= 0 ;* *// initialize fault not detected*
(07) **while** *((StopSim == 0) and (Nstat <* $MAXstat$*))* **do**
(08) *make new simulation ;*
(09) *compute the value* Vf_{ij} *of faulty circuit ;*
(10) **if** $(|\mu_g - Vf_{ij}| > 6\sigma_g)$ **then**
(11) DD_{ij} *= 1 ;* *// the fault is detected*
(12) *StopSim = 1 ;*
(13) **else**
(14) *Nstat ++*
(15) *save* Vf_{ij} *// needed to compute* μ_f *et* σ_f
(16) **end if**
(17) **end while**
(18) **if** $(DD_{ij} == 0)$ **then** *// if fault not detected*
(19) *compute* μ_f *et* σ_f *of faulty circuit ;*
(20) $I_g = [\mu_g - 2\sigma_g\ ,\ \mu_g + 2\sigma_g]$ *;*
(21) $I_f = [\mu_f - 2\sigma_f\ ,\ \mu_f + 2\sigma_f]$ *;*
(22) $DD_{ij} = \frac{(I_f - I_g)}{(I_f \cap I_g) + (I_f - I_g)}$ *;*
(23) **end if**
(24) **end for**
(25) **end for**

This algorithm is based on assumption (5). For each test T_i, we compute the mean and the standard deviation μ_g *and* σ_g of the fault-free circuit, and for each fault F_j we make the first simulation to evaluate Vf_{ij}. If Vf_{ij} satisfies assumption (5), then the fault is detected (DD_{ij} = 1) and we proceed to the next fault, else we save the value and we choose another simulation and repeat the same process. If after $MAXstat$ simulations ($MAXstat \in [5 \cdots 30]$), assumption (5) is not reached, then we compute the mean μ_f and the standard deviation σ_f of the distribution of the MAXstat simulated values of the faulty circuit. At the end, we compare the two distributions with the following feasibility function :

$$\boxed{DD(I_g, I_f) = \frac{(I_f - I_g)}{(I_f \cap I_g) + (I_f - I_g)}} \quad (6)$$

With $I_g = [\mu_g - 2\sigma_g\ ,\ \mu_g + 2\sigma_g]$ and
$I_f = [\mu_f - 2\sigma_f\ ,\ \mu_f + 2\sigma_f]$

The function $DD(I_g, I_f)$ allows us to quantify by a number $\in [0\ ,\ 1]$ how much the distribution of the faulty circuit, represented by the interval I_f, is close to the distribution of the fault-free circuit, represented by the interval I_g. The coefficient DD_{ij} defines the detectability degree of the fault F_j by the test T_i, it can be considered as the probability that a test T_i detects the fault F_j. When we have $D_f \approx D_g$ (the symbol $\approx$ means close to), that means $I_f \approx I_g$, $(I_f - I_g) \approx 0$ and $DD_{ij} \approx 0$. In the opposite case, if $D_f \not\approx D_g$ then $(I_f - I_g) \approx 1$, $(I_f \cap I_g) \approx 0$ and $DD_{ij} \approx 1$. So, when the coefficient DD_{ij} is close to 1, it means that the probability to detect the fault is high ($(DD_{ij} = 1) \Longrightarrow$ the fault is detected), and when DD_{ij} is close to 0 the probability to detect the fault is low ($(DD_{ij} = 0) \Longrightarrow$ the fault is not detected).

At the end of all simulations, we obtain a matrix of detectability degrees DD_{ij}, in which columns $T_1 \cdots T_n$ of the matrix represent the n tests and the rows $F_1 \cdots F_m$ represent the m faults, refere to table 2.

frequency	mean	std. dev.
5.0W+02	0.05	0.03
1.5E+03	0.02	0.05
2.5E+03	0.12	0.30
3.5E+03	-0.61	0.78
4.5E+03	-23.77	3.78
5.5E+03	-47.65	7.70
6.5E+03	-45.22	2.19
7.5E+03	-60.49	6.94
8.5E+03	-51.52	2.25
9.5E+03	-45.98	1.11
1.0E+04	-44.70	0.93

Table 1. The mean and standard deviation of the fault free circuit

3. Simulation results

The fifth-order low-pass switched-capacitor filter shown in figure (3) is used as the test device. The magnitude of the filter transfer function is used as the output parameter to be analyzed. Due to the switched nature of the considered circuit, an AC analysis could not be used to develop the filter transfer function. Instead, transient analysis is used with a narrow input pulse representing a dirac-delta function. The fourier transform of the output impulse response then represents the filter transfer function in the frequency domain. In this example, emphasis is made on the effect of capacitor parametric faults, thus macromodels are used for the op-amps and the switches.

For the fault free and all faulty circuits, we assume that all capacitor values are within $\pm 5\%$ due to process statistical variations. The fault free filter response for a thirty Monte Carlo runs is shown in figure (4). As an example of faulty circuit simulations, the Monte Carlo runs with the value of capacitor C054 changed by -50% is also shown in figure (6). We can see from the two responses that the standard deviation of the circuit output is frequency dependant. Table 1 shows the mean and the standard deviation of the fault free circuit calculated from 100 Monte Carlo runs. It can be seen from table 1 that in the frequency range $[3.5kHz, 8.5kHz]$ we have a high standard deviation σ_g of the fault free circuit. Then the probability that a faulty value V_f satisfies the assumption (5) so that the fault could be detected is very small in that frequency range. Hence, in order to avoid excessive simulations, it would be better to apply the approach described in section (2.2) only to the frequency range $[0, 3.5kHz] \cup [9kHz, 10kHz]$.

In order to validate the assumption that the output probabilty distribution function (PDF) is close to a normal one, the histograms of the magnitude of the output of both the

cap. name	par. fault	frequency (kHz)				
		0.5	1.5	2.5	3.5	10
c010	-50%	1.00	1.00	1.00	0.39	0.27
c01	+100%	1.00	1.00	1.00	1.00	1.00
c025	-50%	0.20	0.24	0.28	1.00	0.17
c033	+100%	1.00	1.00	1.00	1.00	1.00
c041	-50%	1.00	1.00	1.00	1.00	1.00
c04	+100%	1.00	1.00	1.00	1.00	1.00
c054	-50%	1.00	1.00	1.00	1.00	1.00
c010	+100%	1.00	1.00	1.00	1.00	0.01
c021	-50%	1.00	1.00	1.00	1.00	1.00
c025	+100%	0.17	0.37	1.00	1.00	0.17
c034	-50%	1.00	1.00	1.00	1.00	1.00
c041	+100%	1.00	1.00	1.00	1.00	1.00
c050	-50%	1.00	1.00	1.00	1.00	0.30
c054	+100%	0.28	0.08	1.00	1.00	1.00
c012	-50%	1.00	1.00	1.00	1.00	1.00
c021	+100%	1.00	1.00	1.00	1.00	1.00
c02	-50%	1.00	1.00	1.00	1.00	0.50
c034	+100%	1.00	1.00	1.00	1.00	0.46
c044	-50%	1.00	1.00	1.00	0.67	0.07
c050	+100%	1.00	1.00	1.00	1.00	0.15
c05	-50%	1.00	1.00	1.00	0.10	1.00
c012	+100%	1.00	1.00	1.00	1.00	1.00
c024	-50%	1.00	1.00	1.00	1.00	0.00
c02	+100%	1.00	1.00	1.00	1.00	1.00
c03	-50%	1.00	1.00	1.00	1.00	1.00
c044	+100%	1.00	1.00	1.00	0.43	0.40
c053	-50%	0.51	1.00	1.00	0.18	1.00
c05	+100%	1.00	1.00	0.27	1.00	1.00
c01	-50%	1.00	1.00	1.00	1.00	1.00
c024	+100%	1.00	1.00	1.00	1.00	1.00
c033	-50%	1.00	1.00	1.00	1.00	1.00
c03	+100%	1.00	1.00	1.00	1.00	1.00
c04	-50%	0.29	0.07	1.00	1.00	1.00
c053	+100%	1.00	1.00	1.00	1.00	1.00

Table 2. Matrix DD_{ij} considering the magnitude of the filter response.

nb simulations	nb of faults
1	9
2	2
3	1
5	22

Table 3. Global number of simulations of all 34 faults.

fault free and the faulty circuits at multiple frequencies are investigated. As an example, those histograms are shown in figures (5) and (7) at four different frequencies. From these histograms, we have found that for low (below 3.5 kHz) and high (above 8.0 kHz) frequencies, the ouptut PDF is close to a normal one. From table 1, we notice that for the same frequence range $[0, 3.5kHz] \cup [9.0kHz, 10kHz]$, we have a low standard deviation. Otherwise, for mid-frequencies, the output PDF is close to a χ^2 distribution. Consequently, the approach described in section (2.2) can be successfully applied in the frequency range $[0, 3.5kHz] \cup [9kHz, 10kHz]$.

During analog fault simulation, we have considered two parametric faults for each capacitor (17 capacitors), with -50% and +100% changes. Simulations are performed at five different frequencies in the above frequency range. Simulation results are shown in table 2 which shows the computed matrix of the detectability degree (see section (2.3)) considering the magnitude of the filter response. It can be seen that all faults are detected at least at one test frequency. Only the -50% deviation fault of the C025 capacitor is detected at only one test ($frequency = 3.5kHz$). For production test optimization [4], it can also be noticed that all faults are detected at only two frequencies, namely $1.5kHz$ and $3.5kHz$.

In table 3 the number of simulations performed for all faults is shown with the maximun number of simulations MAXstat set to 5. The global number of simulations performed after optimization is $(1 * 9) + (2 * 2) + (3 * 1) + (5 * 22) = 126$, with about $18s$ CPU time for each simulation. The global CPU time used is $37mn$ and $48s$ on an UltraSparc IIi-333MHz. With just Monte Carlo simulation, the number of simulations needed is $34 * 5 = 170$ and the CPU times is $51mn$. Thus the speed-up of the presented approach is about 35% with no loss of accuracy.

4. Conclusions

We have presented a new methodology for fast and accurate fault simulation of analog circuits under parameter variations. We have introduced our approach using the statistical theory, and demonstrated the new technique with a fifth-order low-pass switched-capacitor filter. In the shown example, we have computed the probability of each frequency to detect each fault according to the magnitude of the filter response, thus reducing the number of the required Monte Carlo simulations.

This method is currently studied to implement an (ATSO) Automatic Test Stimulis Optimisation for analog circuits subject to process variations.

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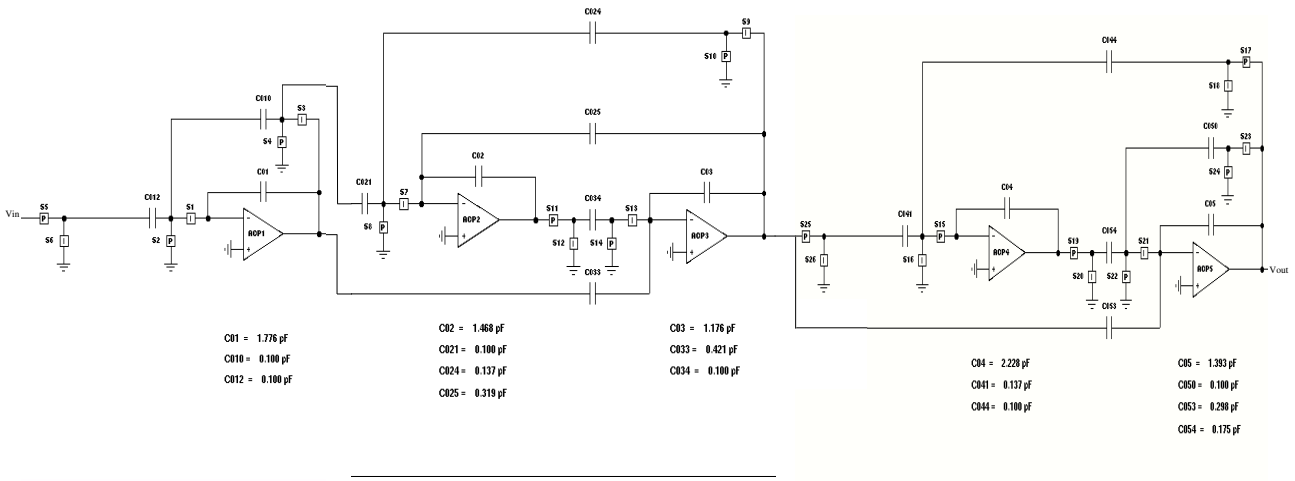

Figure 3. 5th switched-capacitor filter.

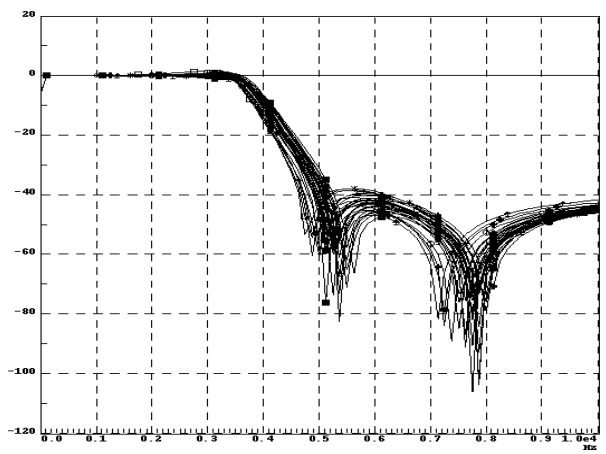

Figure 4. Simulated transfer function of the fault free circuit in dB.

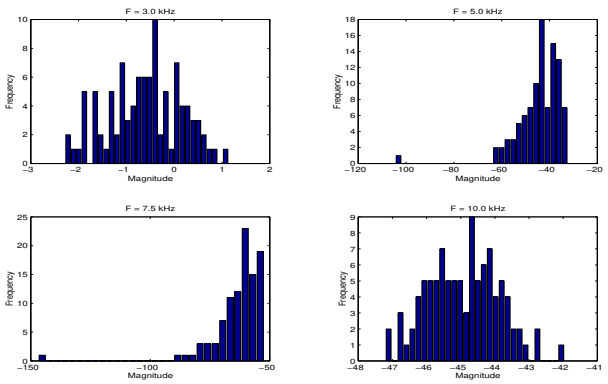

Figure 5. Histograms of the magnitude of the fault free circuit at four frequencies.

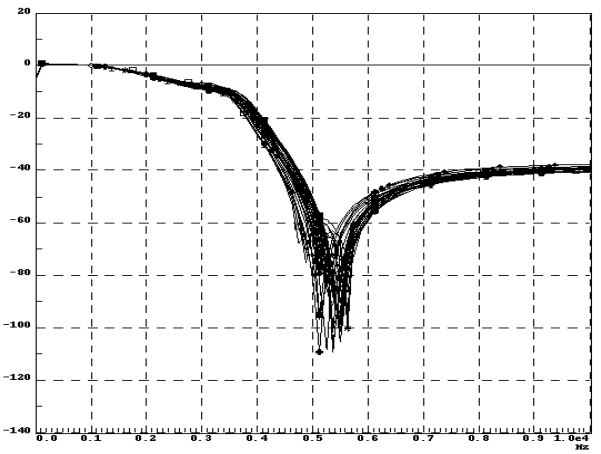

Figure 6. Simulated transfer function of the faulty circuit in dB.

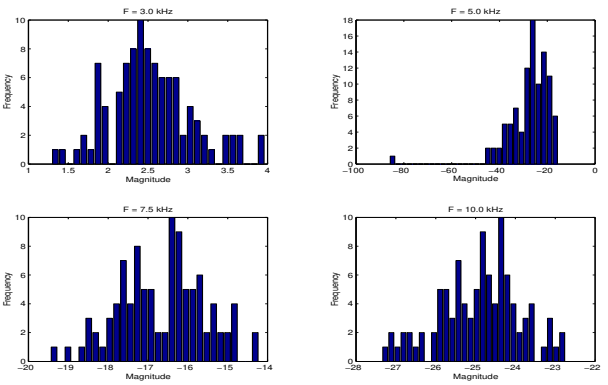

Figure 7. Histograms of the magnitude of the faulty circuit at four frequencies.