EFFICIENT POLYPHASE DECOMPOSITION OF COMB DECIMATION FILTERS IN $\Sigma\Delta$ ANALOG-TO-DIGITAL CONVERTERS.

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***Abstract*—A** power efficient multi-rate multi-stage Comb decimation filter for mono-bit and multi-bit $\Sigma\Delta$ A/D converters is presented. Polyphase decomposition in all stages, with high decimation factor in the first stage, is used to significantly reduce the sampling frequency of the Comb filter. Several implementations indicate that proper choice of the first stage decimation factor can considerably improve power consumption, area and maximum sampling frequency. In multibit $\Sigma\Delta$ A/Ds, this optimum first stage decimation factor is function of the input wordlength.

I. INTRODUCTION

Nowadays, power consumption of decimation filters in $\Sigma\Delta$ A/D converters is receiving an increasing attention [1][2][3]. Comb filters, shown in Fig.1(a), are widely used in the decimation filter of $\Sigma\Delta$ A/D converters. These filters operate at maximum sampling frequency before any decimation takes place. The power consumption of Comb filters is then very high. The transfer function $H(z)$ of a Comb filter of order k and for a decimation ratio M is defined by

$$H(z) = \left(\frac{1 - z^{-M}}{1 - z^{-1}}\right)^k . \qquad (1)$$

These filters were usually implemented using the IIR-FIR technique [4], Fig.1(b). Recently lower power consumption has been achieved using the FIR2 [3], and the POLY-FIR2 [5], implementations, shown in Fig.1(c) and Fig.1(d) respectively.

In this paper, we present a different representation of the Comb filter. This representation allows us to exploit the Polyphase decomposition in order to perform higher decimation factors at the input of the first stage. Although coefficients, resulting from this decomposition, require expensive multiplication operations and larger wordlength, the overall power consumption is lower. This is due to the significant reduction of the operating frequency. We show that, an optimum decimation factor exists that compromises the added complexicity of the Polyphase decomposition with the reduction of the operating frequency. This optimum decimation factor depends on the output wordlength of the $\Sigma\Delta$ modulator.

II. PREVIOUS WORK COMPARISON

In the IIR-FIR structure, shown in Fig.1(b), the FIR filter, $(1 - z^{-1})^k$, operates at a sampling frequency M times lower

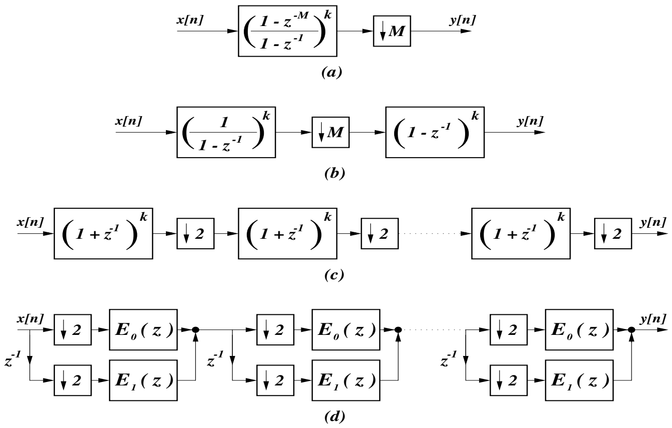

Fig. 1. (a) Comb filter. (b) IIR-FIR implementation. (c) FIR2: cascade of FIR filters each decimating by 2. (d) POLY-FIR2: Polyphase decomposition applied to FIR2.

than the IIR filter, $(\frac{1}{1-z^{-1}})^k$. In order to ensure stability of the IIR filter, the wordlength of the IIR filter has to be equal to $(W_0 + k\ log_2 M)$ bits [4], where W_0 is the number of bits at the filter input. The major drawback of this architecture is that the IIR filter is operating at maximum sampling frequency and with a very large wordlength.

Equation (1) can be written in the following form:

$$H(z) = \prod_{i=0}^{(log_2 M)-1} \left(1 + z^{-2^i}\right)^k . \qquad (2)$$

Applying the commutative rule [6], we get the FIR2 structure shown in Fig.1(c). In this structure, the Comb filter is realized by cascading $log_2 M$ identical FIR filters, $(1 + z^{-1})^k$, each decimating by 2. The POLY-FIR2 structure [5], illustrated in Fig.1(d), is obtained by applying Polyphase decomposition [7], to the FIR2 structure. In this case, the decimation occurs at the input of each filter, thus reducing by 2 the sampling frequency of each stage. The FIR2 and the POLY-FIR2 structures have the advantage of not having any stability problems and the wordlength of each stage i is limited to $(W_0 + k\ i)$ bits.

The average power consumption of a digital signal processing system is proportional to: the number of operations performed per sample, the wordlength and the sampling frequency. In Comb filters, we will assume that the number of operations is equal to the number of partial products to be added.

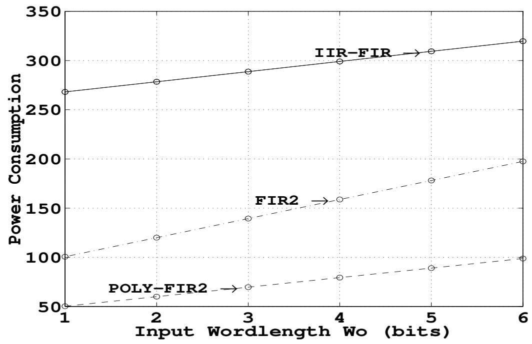

Fig. 2. Estimation of power consumption for different implementations of a 5^{th} order Comb filter with a decimation factor of 32 ($k = 5$ and $M = 32$).

The power consumption, P, can then be defined by the following relation:

$$P = \sum_{i=1}^{l} \frac{NP_i * W_i}{\prod_{j=1}^{i} M_j} \tag{3}$$

where NP_i is the number of partial products to be added in stage i, W_i the input wordlength of stage i, M_j the decimation factor in stage j and l the total number of decimation stages.
Equation (3) is used to compare the power consumption for different implementations of a 5^{th} order Comb filter, with a decimation factor of 32. Fig.2 shows that power consumption of POLY-FIR2 is significantly lower than the two other techniques. All three implementations have the same number of partial product per stage ($NP_i = 10$). The very large wordlength, in the first stage of the IIR-FIR technique ($W_i = W_0 + 25$), is the reason behind its considerably higher power consumption. POLY-FIR2 requires exactly the same hardware as FIR2, but operates at half the sampling frequency.

In the next section, we will introduce a different architecture that reduces even more power consumption, especially for low input wordlength.

III. Proposed Comb Filter Architecture

As shown in Fig.3(a), we propose to decompose the Comb decimation filter into a first stage FIR filter $H_1(z)$ with a decimation factor M_1, followed by a cascade of FIR $(1 + z^{-1})^k$ filters with a decimation factor 2. The reason behind choosing this representation is that we would like to decimate as much as possible in the first stage. The following stages are kept with the minimum decimation ratio 2 because, when the wordlength of the input signal is high, reducing the sampling frequency does not compensate for the added complexity of the Polyphase decomposition. In the following, we will explain how Polyphase decompostion is applied to Comb decimation filters. Equation (1) can be written in the following form:

$$H(z) = H_1(z) \;\; H_2(z) \tag{4}$$

where,

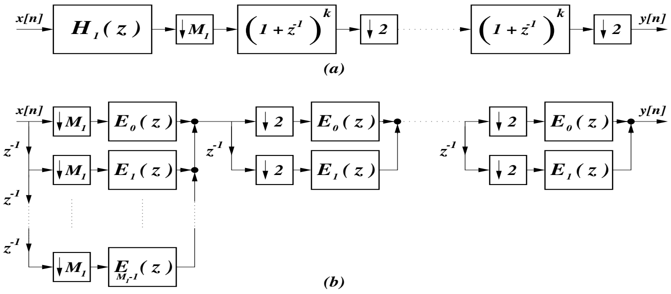

Fig. 3. (a) Cascade of FIR with high decimation factor M_1 in the 1st stage. (b) Polyphase decomposition of the 1st stage filter $H_1(z)$ decimating by M_1 and the subsequent filters decimating by 2.

$$H_1(z) \;=\; \left(\sum_{i=0}^{M_1-1} z^{-i} \right)^k \tag{5}$$

$$H_2(z) \;=\; \prod_{i=0}^{(log_2 \frac{M}{M_1})-1} \left(1 + z^{-2^i}\right)^k. \tag{6}$$

The expansion of $H_1(z)$ results in an FIR filter of order $k(M_1 - 1)$

$$H_1(z) = \sum_{n=0}^{k(M_1-1)} h(n) z^{-n}. \tag{7}$$

The coefficients of this filter are integers and symmetrical $h(n) = h(N - 1 - n)$, where $N = k(M_1 - 1)$. Applying Polyphase decomposition on the filter of equation (7), we get

$$\begin{aligned} H_1(z) &= \sum_{n=0}^{k(M_1-1)} h(nM_1) z^{-nM_1} \\ &= z^{-1} \sum_{n=0}^{k(M_1-1)} h(nM_1+1) z^{-nM_1} \\ &\;\vdots \\ &= z^{-(M_1-1)} \sum_{n=0}^{k(M_1-1)} h(nM_1+M_1-1) z^{-nM_1}. \end{aligned} \tag{8}$$

Efficient Polyphase implementation of $H_1(z)$ is shown in Fig.3(b). As we can see, decimation takes place before filtering, so multiplications and additions are performed at a sampling frequency M_1 times lower than the frequency of the input signal. The subsequent filters decimating by 2 are nothing but a special case of the general case described above.
Higher values of M_1 will significantly reduce the sampling frequency of the first stage which can be interesting for power consumption. On the other hand, we can see, from equation (5), that higher values of M_1 will increase the order of the filter $H_1(z)$, which implies more complex coefficients and a higher number of partial products. Note also that the wordlength of the polyphase filter will increase since it is equal to $(W_0 + k \; log_2 M_1)$ bits.

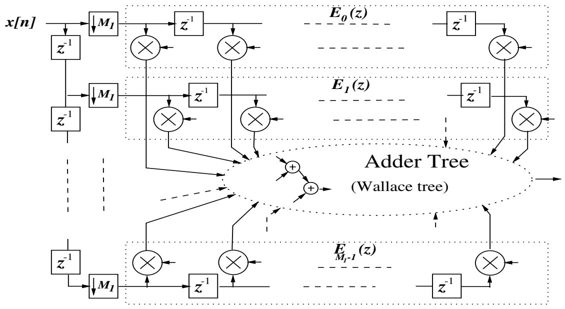

Fig. 4. Direct-form implementation of one stage of the Comb filter using one adder-tree.

In order to find the decimation factor M_1 that achieves minimum power consumption, several implementations with different values for M_1 have been implemented and are presented in the following section.

IV. Filter Implementation

The choice of the FIR architecture to implement the polyphase filters has an important impact on power consumption. FIR filters are implemented either in a transposed-form or a direct-form. Each of these two forms has one main drawback. The transposed-form requires larger wordlength for the intermediate registers, which can increase power consumption. The direct-form has a long critical path which limits the maximum sampling frequency of the filter. Since the use of Polyphase decomposition has highly reduced the operating frequency of the filter, the critical path is no longer a problem. Thus we have chosen the direct-form implementation.
Fig.4 shows the general architecture for one stage of the comb decimation filter. All the subfilters, E_0, E_1, ..., E_{M_1-1}, resulting from the polyphase decomposition are operating at the same sampling frequency. One way of reducing the required hardware is to gather all additions from the different subfilters into one adder tree. This adder tree is also used in the multipliers to sum all the partial products. In fact, partial products resulting from different multiplications is gathered with the addition operations in the same adder tree. The Wallace tree [8] is an efficient realization of the adder tree. This technique is usually used in the implementation of high speed multipliers [8][9]. Note that, we have only one Wallace tree for the complete polyphase filter. This has significantly reduced the overall power consumption.

V. Performances Evaluation

To study the effect of the decimation factor of the first stage M_1 on the overall performance of the circuit, several 5^{th} order Comb filters, with a total decimation factor M of 32 have been implemented. Each filter had: a different decimation factor in the first stage ($M_1 = 2, 4, 8, 16, 32$), and a different input wordlength ($W_0 = 1, 2, 3, 4, 5, 6$ bits). These filters have been realized using the proposed system architecture described in

TABLE I
NP_1 FOR ALL VALUES OF M_1 (5^{th} ORDER COMB).

M_1	2	4	8	16	32
NP_1	10	41	139	346	919

section III. and with the implementation described in section IV.. Table I lists the number of partial products NP_1 for all possible decimation factors M_1.

Three criteria have been chosen for evaluation: power consumption, area and maximum sampling frequency. Power consumption is estimated using equation (3). A similar equation can be deduced to estimate the area of the circuit. We assume, as in section II., that the hardware required to add the multiplication partial products is dominant. The area, A, can then be defined as

$$A = \sum_{i=1}^{l} NP_i * W_i. \tag{9}$$

The maximum operating frequency, F_{max}, can also be estimated by

$$F_{max} = 1/ \underset{i \in \{1,\dots,l\}}{Max} \left(\frac{log_2(NP_i * W_i)}{\prod_{j=1}^{i} M_j} \right) \tag{10}$$

where $log_2(NP_i * W_i)$ is the number of combinational logic layers necessary to sum the partial products of stage i.

The estimated circuit performances, based on equations (3), (9) and (10), are shown in Fig.5. The circuits have been implemented in a standard low-cost $0.35\mu m$ technology. Simulation results of the circuit performances are shown in Fig.6. Comparing Fig.5 and Fig.6, we see that equation-based estimations are very close to the simulations.

Analyzing these figures, we can see that, for mono-bit $\Sigma\Delta$, minimum power consumption and area are achieved for a decimation factor $M_1 = 16$. The worst performances are obtained when $M_1 = 2$, which is in fact nothing but the POLY-FIR2 structure. Comparing the two implementations for $M_1 = 16$ and $M_1 = 2$: the power consumption is reduced by 30%, the area is reduced by 20%, and the maximum sampling frequency is 5 times higher. In fact, the sampling frequency is limited by the intrinsic propagation delay of the D Flip-Flop.

For multi-bit (6-bit) $\Sigma\Delta$, minimum power consumption and area are achieved for a decimation factor $M_1 = 2$ and $M_1 = 4$. Since higher frequency of operation can be achieved with $M_1 = 4$, the implementation with $M_1 = 4$ is more interesting. In general, for multi-bit $\Sigma\Delta$, we can see that, as the number of bits at the input of the Comb filter decrease, the proposed architecture becomes more interesting. Although the main purpose from this architecture was to achieve low-power consumption, significant improvements regarding area and maximum sampling frequency have also been obtained.

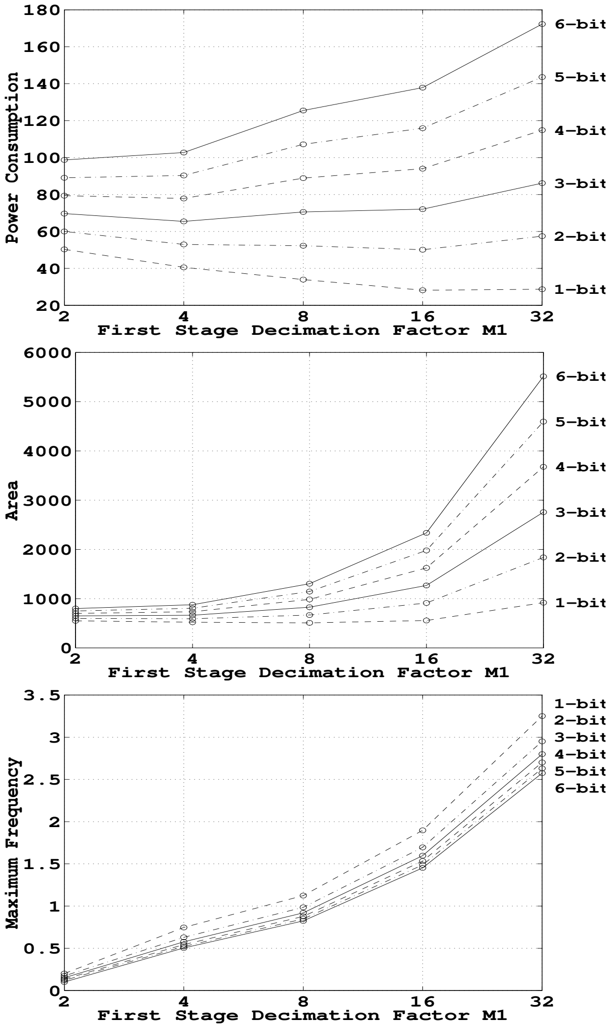

Fig. 5. Calculation of Polyphase Comb filters performances using equations (3), (9) and (10).

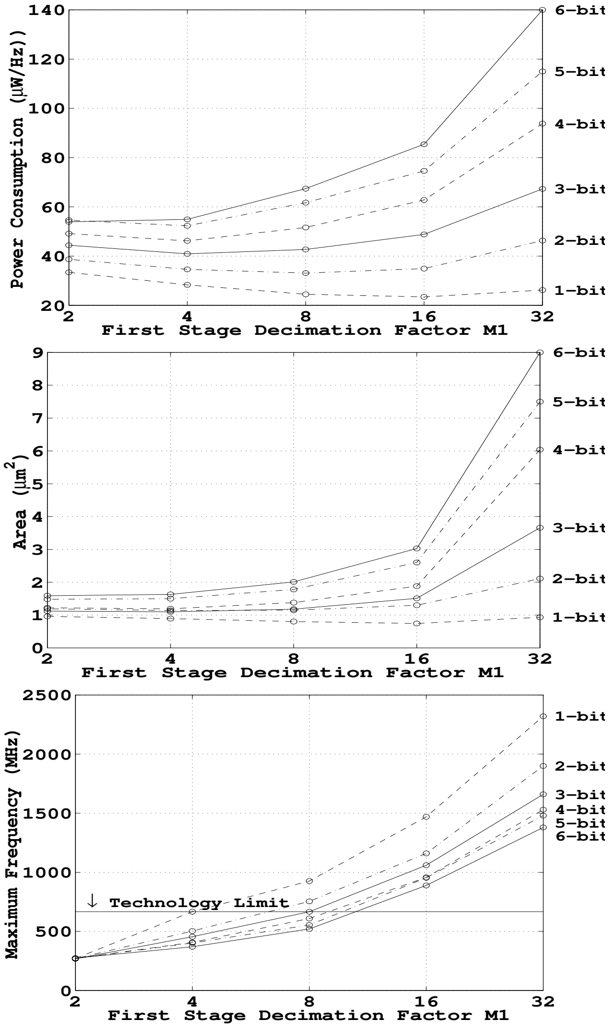

Fig. 6. Simulation results of the Polyphase Comb filters implemented in a $0.35\mu m$ technology.

VI. Conclusion

Low-power implementations of a Comb decimation filter for mono-bit and multi-bit $\Sigma\Delta$ A/D converters have been presented. A multi-stage polyphase structure with maximum decimation factor in the first stage has been used. The proper choice of this first stage decimation factor can significantly improve power consumption, area and maximum sampling frequency. In order to find this optimum first stage decimation factor, simple equations have been developed to estimate circuit performances of the proposed architecture. Gathering all the partial products additions into one adder tree has also considerably reduced the required hardware for the circuit.

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