A 1V 1mW Digital-Audio $\Delta\Sigma$ Modulator with 88dB Dynamic Range using Local Switch Bootstrapping

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Abstract

A 1V, 1mW, 14 bit delta-sigma modulator in a standard CMOS 0.35-μm technology is presented.
A modified symmetrical bootstrapped switch is used in order to allow rail-to-rail signal switching.
A single-loop third-order topology with an oversampling ratio of 100 achieves a dynamic range of 88 dB, a peak SNR of 87 dB and a peak SNDR of 85 dB in a signal bandwidth of 25 kHz.

Introduction

The demand on low-voltage low-power mixed-signal circuits is signficantly increasing in order to cope with modern advances in portable and battery operated systems. Analog to digital converters are one of the performance limiting blocks. Special techniques such as $\Delta\Sigma$ modulation allow to build robust high resolution converters in modern IC technologies.
The major limitation to low-voltage operation is the switch resistance which increases considerabely as the driving clock voltage goes down. In order to avoid the use of expensive multithreshold processes, low-voltage $\Delta\Sigma$ modulators often use clock voltage multiplication (1). This however is not power efficient and not compatible with advanced low-voltage CMOS processes where gate oxide overstress becomes an issue. Alternatively, the switched-opamp technique has been used (2). However, the switch connected to the circuit input remains and it restricts severely the maximum allowable amplitude of the input signal. The switching of the opamp may also affect the speed of the circuit. In addition, serious non-linearity problems emerge which limit the peak SNDR (2). Recently, a new compact bootstrapped switch implementation (3) has been proposed in order to allow rail-to-rail signal switching. Oxide overstress is completely avoided which renders this implementation fully compatible with modern low-voltage CMOS processes.
This paper uses the switch bootstrapping technique to build a very low-voltage $\Delta\Sigma$ modulator. Modifications introduced to the bootstrap circuit as well as the opamp enhance the reliability of the circuit and reduce overall power consumption.

Modulator architecture

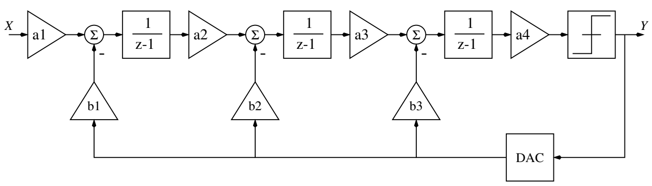

Fig. 1. Modulator topology

For low-voltage low-power applications, a single loop $\Delta\Sigma$ modulator topology is preferable over a cascaded one because it has more relaxed requirements on the amplifiers used except for the first stage. Therefore, integrators inside the feedback loop can be scaled down resulting in low power dissipation. However, in order to keep the oversampling ratio relatively low to reduce power consumption, the loop order must be increased. A third-order feedback topolgy based on delayed integrators is thus used. Fig. 1 shows the block diagram of the modulator. Modulator coefficients have been determined with the help of the *Delta-Sigma Toolbox* (4).
Fig. 2 shows the switched capacitor implementation of an integrator cell used in the modulator. Delayed clocks reduce charge injection. This integrator structure permits to set the input and output common-mode (CM) voltages independently. The output CM voltage V_{cm-out} is set to the mid-supply 0.5V, while the input CM voltage V_{cm-in} is set to zero. Bootstrapped switches are used to switch voltages around V_{cm-out} while simple n-switches are used to switch voltages at V_{cm-in}. CMOS switches are only used to switch the DAC levels, namely VSS and VDD.

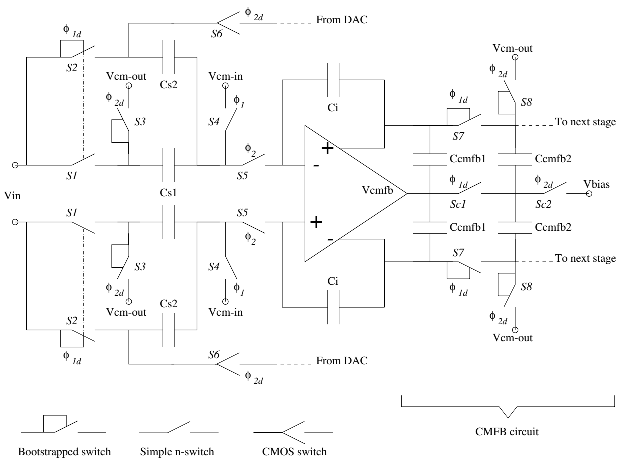

Fig. 2. Integrator using symmetrical bootstrapped switches

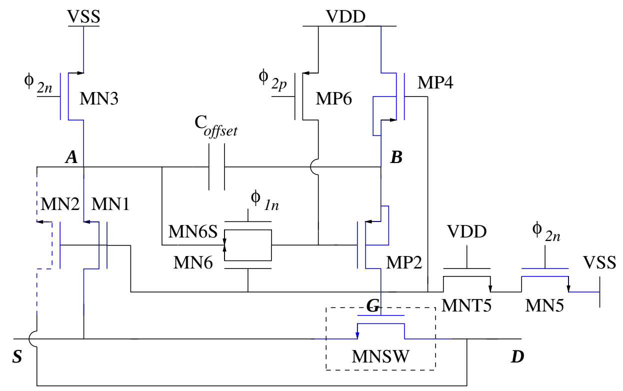

Fig. 3. Symmetrical n-switch with local bootstrapping

Low-voltage building blocks

A. Symmetrical bootstrapped switch

The gate-source bootstrapping technique (3) is used to allow low-voltage operation of simple n-switches. Fig. 3 shows the transistor implementation of the bootstrap circuit. Capacitor C_{offset} is charged to VDD during ϕ_2 through transistors $MN3$ and $MP4$ while the main switch $MNSW$ is cuttoff through transistor $MN5$. During ϕ_1, C_{offset} is placed around the gate-source terminals of $MNSW$ through transistors $MN1$ and $MP2$. Transistor $MN6S$ triggers $MP2$ ON at the beginning of ϕ_1 while transistor $MN6$ keeps it ON as the voltage on node A rises to the source voltage. The gate connection of $MP4$ prevents its overstress as the voltage on node B rises above VDD. Furthemore, transistor $MNT5$ has been added to prevent the gate-drain voltage of $MN5$ from exceeding VDD during ϕ_1 while it is OFF. This circuit allows switch operation (transistor $MNSW$) from rail-to-rail while limiting all gate-source voltages to VDD avoiding any oxide overstress. It also guarantees maximum switch conductance independently of the switched potential and enhances considerabely the switch linearity.
However, in the circuit presented in (3) the voltage at the drain side of the main switch $MNSW$ must be always higher than that at the source side at the switching moment to prevent the drain-gate voltage from exceeding VDD. In order to overcome this limitation, an additional transistor $MN2$ has been added on the drain side, shown dashed in Fig. 3, such that the switch $MNSW$ becomes completely symmetrical. The gate voltage is thus clamped at a voltage VDD higher than the terminal of the lowest voltage.
It is to be noted that another bootstrap switch implementation has also been proposed (5). However, the used bootstrap implementation has the merit of being much more simple.
Finally, it should be mentioned that the same bootstrap circuit can be used to drive parallel switches. This can be seen for switches $S1$ and $S2$ in Fig. 2.

B. Opamp

Fig. 4 shows the used opamp. It is based on a fully differential p-type two stage miller-compensated structure. The common-mode feedback (CMFB) circuit for the first stage has been replaced by the cross-coupled connection of transistors $M51$, $M52$, $M61$ and $M62$ similar to (6). The conductance gm_{51} seen at the gate of transistors M51 and M61 is canceled by the opposite action of the parallel transistors M52 and M62 respectively. This negative feedback connection causes the differential signal at the output of the first stage (nodes $n3$ and $n4$) to see a high load impedance. The output conductance is thus limited by gds_8.
On the other hand, for the common mode signal, the output conductance is limited by $gm_{51} + gm_{52}$. This is a low impedance and thus the first stage does not require an

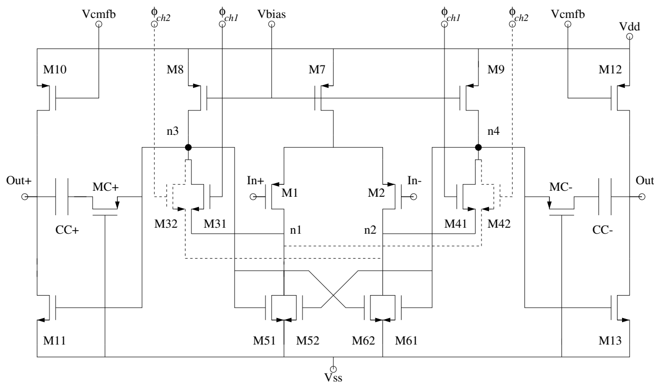

Fig. 4. Two-stage amplifier with first-stage inherent CMFB

additional CMFB circuit.

For the second stage a simple passive switched-capacitor CMFB circuit (shown in Fig. 2) is used. However, bootstrapped switches must be used in the CMFB circuit for those switches that have to switch the V_{cm-out} potential. Furthermore those bootstrapped switches can be shared with the sampling network connecting the integrator output to the subsequent stage as shown in Fig. 2.

While flicker noise can be reduced using larger areas for the transistors contributing to the flicker noise (namely M1, M2, M5, M6, M8 and M9), this causes higher parasitic capacitance on the internal nodes increasing the amplifier power consumption. To overcome this, chopper stabilization has been used. The output of the first stage is chopped as shown in Fig. 4 using only two additional cascode transistors M32 and M42 in parallel with the existing ones but with their sources connected to nodes $n2$ and $n1$ respectively. The gates of both cascodes are then driven by two *overlapping* chopper clocks (ϕ_{ch1} and ϕ_{ch2}) at half the sampling frequency. The two chopper clocks must overlap to avoid the simultaneous cutoff of both cascodes in parallel which would increase the settling time of the opamp. This arrangement reduces the $1/f$ noise for all transistors but M8 and M9 where a larger transistor length must be used. Choppper stabilization is used only for the first integrator stage. Noise of subsequent stages undergoes noise shaping by the loop filter.

Using the supply voltage as the gate bias of the cascode transistors eliminates the need of an additional biasing voltage and allows very low-voltage operation. On the other hand it limits the maximum allowable supply voltage to around 1.2V.

C. Comparater

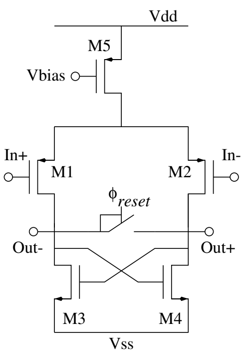

Fig. 5. Low voltage comparater

Since there is no critical design requirements on the comparators used in $\Delta\Sigma$ modulators, a simple low voltage comparater similar to that presented in (2) is used. Resetting the comparator to the metastable state is done using a bootstrapped switch as shown in Fig. 5. The input common mode of the comparator is at VSS, a simple switched capacitor circuit is used to shift the level of the last integrator output which is around $VDD/2$ to VSS.

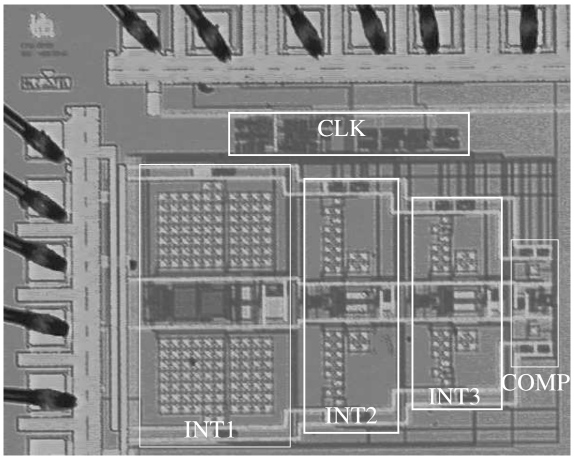

Fig. 6. Chip die photo

Experimental Results

The modulator has been implemented in a 0.35-μm standard CMOS process with double poly and triple metal. The threshold voltages for the n and p-transistors are 640 mV and 630 mV respectively. Fig. 6 shows the chip photograph. The core area excluding bonding pads is 0.9×0.7 mm^2.

A single clock at 5 MHz is used to drive the converter. The non-overlapping delayed clock phases as well as the overlapping clock phases at half the clock frequency needed for the chopping circuit are all generated on chip. On the test board, the input signal is converted from single-ended to a differential one using a transformer and shifted to a common-mode level equal to $VDD/2$. The digital output of the converter is captured with a data analyzer through opto-couplers to isolate ground noise of the digital measurement equipment. The data are then transferred to a PC, which performs FFT, windowing and graphical representation.

The modulator operates at a VDD of 1V and dissipates 950 μW. 60% of the total power is consumed by the first intgerator. The reference voltage is set to 1V and is brought on chip on a separate pad. With an oversampling ratio of 100, the signal bandwidth is 25 kHz. Fig. 7 shows the measured SNR and SNDR versus the relative input amplitude (V_{in}/V_{ref}). An input sinusoidal signal at 3.2 kHz was used to produce these plots. It is apparent that the modulator achieves a dynamic range of 88 dB, a peak SNR and a peak SNDR of 87 dB and 85 dB respectively. Based on the dynamic range, the figure of

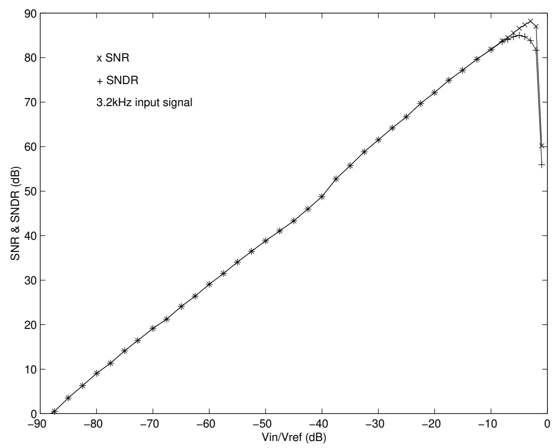

Fig. 7. Measured SNR & SNDR

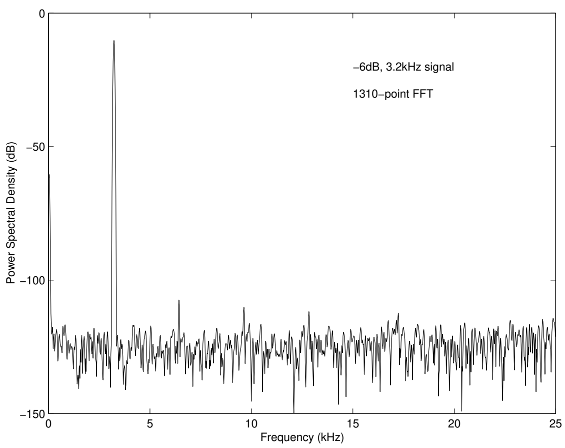

Fig. 8. Measured baseband output spectrum

merit is slightly less than that reported in (2), whereas the SNDR is around 25 dB higher. The measured performance is summarized in table I.

Fig. 8 shows the output spectrum for a 3.2 kHz input signal at -6 dB relative input level. The frequency independence of the noise floor indicates that the modulator's performance is thermal-noise limited rather than quantization-noise limited.

Contrary to clock boosting circuits, the bootstrap circuit could be used to the maximum supply voltage allowed by the technology. The circuit presented in this work is thus fully compatible with future low-voltage technologies.

TABLE I
Converter Performance Summary

Supply Voltage	1V
Reference Voltage	1V
DR	88dB
Peak SNR / SNDR	85dB / 87 dB
Oversampling Ratio	100
Sampling Rate	5MHz
Signal Bandwidth	25kHz
Power Consumption	950 μW
Figure of Merit $\times 10^6$	275
Die Area	0.9mm $\times$ 0.7mm
Technology	0.35-μm CMOS TMDP

Conclusion

A 1V $\Delta\Sigma$ modulator has been implemented using the bootstrapping technique. Rail-to-rail operation of bootstrapped switches allows very low-voltage robust switched-capacitor implementations in standard CMOS technologies while avoiding transistor gate oxide overstress. Futhermore, switch charge injection and linearity is improved due to the constant gate-source overdrive. An additional transistor renders the switch completely symmetrical and eliminates transient reliability problems.

Modifications introduced to the two-stage folded cascode opamp allow very low-voltage operation and permit the use of a passive CMFB switched capacitor circuit.

Obtained results show the feasibility of very low-voltage high performance circuits using standard switched-capacitor techniques.

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