SYSTEMATIC DESIGN OF HIGH-LINEARITY CURRENT-MODE INTEGRATORS FOR LOW-POWER CONTINUOUS-TIME $\Sigma\Delta$ MODULATORS.

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***Abstract*—In this paper, the main sources of non-linearity in current-mode continuous-time $\Sigma\Delta$ modulators are analyzed. The first integrator gain of the current-mode integrator is optimized to improve the linearity of the $\Sigma\Delta$ modulator. It is shown that by properly choosing the gain of the first integrator, harmonic distortion can be significantly reduced. A systematic design method for continuous-time $\Sigma\Delta$ modulators is presented. This method has been used to design two third order continuous-time $\Sigma\Delta$ modulators using $0.6\mu m$ and $0.18\mu m$ CMOS processes. Operating at a sampling frequency of 25.6MHz, these modulators achieve 80dB of SNDR for a 100kHz input signal bandwidth.

I. INTRODUCTION

Performances of discrete-time switched-capacitors $\Sigma\Delta$ modulators are limited by the increasing switch resistance due to low voltage supply of recent CMOS technologies. Performances of continuous-time $\Sigma\Delta$ modulators are not limited by the high switch resistance and are therefore more adapted to low voltage operation. Continous-time $\Sigma\Delta$ modulators are receiving an increasing attention in low power [1], and high speed [2] applications.

Continuous-Time $\Sigma\Delta$ modulators with non-return-to-zero (NRZ) feedback signal suffer from harmonic distortion due to the DAC output waveform asymmetry [3], and signal-to-noise ratio degradation due to excess loop delay [4]. Continuous-time $\Sigma\Delta$ modulators with return-to-zero (RZ) feedback, Fig.1, can then be used to avoid these problems.

Continuous-time current-mode circuits achieved interesting performances in high-speed low voltage applications [5]. However, current-mirror based circuits suffer from non-linearity and it is difficult to reduce harmonic distortion below -60dB [6].

In this paper, we analyse the main sources of harmonic distortion in current-mode continuous-time $\Sigma\Delta$ modulators. The effect of the first integrator gain and current mirror mismatch on the linearity of the $\Sigma\Delta$ modulator is studied. A systematic design method for high linearity and low-power current-mode $\Sigma\Delta$ modulator is described. This method is used to design two third order $\Sigma\Delta$ modulators with different technologies (0.6μm and 0.18μm CMOS processes).

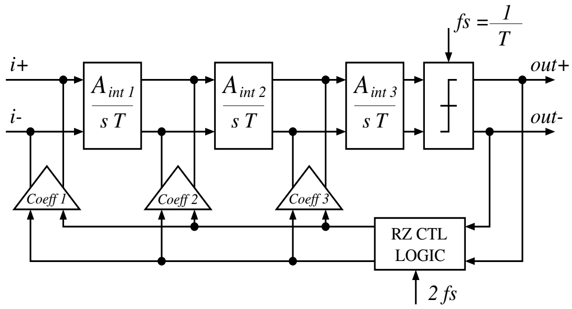

Fig. 1. Third order differential continuous-time $\Sigma\Delta$ modulator.

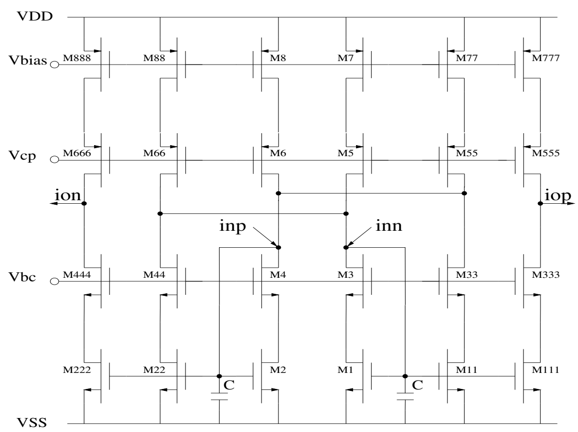

Fig. 2. Current-mode integrator $H(s) = \frac{g_m}{sC} = \frac{A_{int}}{sT}$

II. SOURCES OF HARMONIC DISTORTION

The integrator circuit depicted in Fig.2 has been presented in [5]. Neglecting output conductances and parasitic capacitances and assuming identical transistors, small-signal analysis of the integrator circuit yields the following transfer function:

$$H(s) = \frac{i_{out}(s)}{i_{in}(s)} = \frac{g_{m_{11}}}{s\ C} \tag{1}$$

A. Gm Variation

The main source of harmonic distortion in this current mode integrator is the variation of the transconductance $g_{m_{11}}$ with the input current.

In the following, we will study the impact of the value of the first integrator gain A_{int} on harmonic distortion.

Starting from the simple square model of a MOS tran-

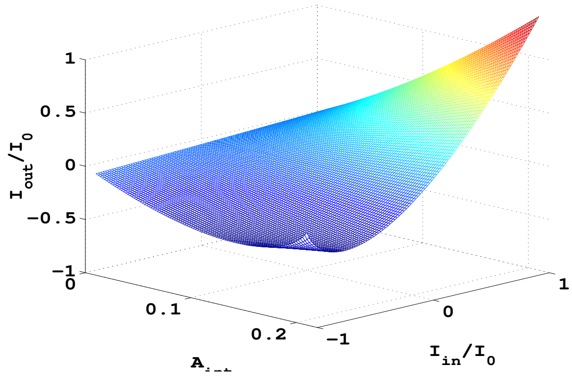

Fig. 3. The normalized output current, $\frac{i_{out}}{I_0}$, in function of the normalized input current $\frac{i_{in}}{I_0}$ and the integrator gain A_{int}, Eq.(6), ($\frac{f}{f_s} = 0.034$).

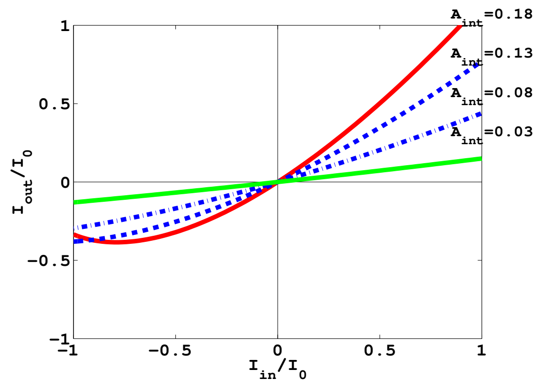

Fig. 4. The normalized output current, $\frac{i_{out}}{I_0}$, in function of the normalized input current $\frac{i_{in}}{I_0}$ for different values of the integrator gain A_{int}, Eq.(6), ($\frac{f}{f_s} = 0.034$).

sistor in the saturation region:

$$I = \frac{\beta}{2}(V_{GS} - V_{TH})^2.$$

The transconductance, $g_m = \beta(V_{GS} - V_{TH})$, can also be expressed in the following form:

$$g_m = \sqrt{2\,\beta\,I}. \qquad (2)$$

The current I_{11} flowing in transistor M_{11}, Fig.2, can be defined as:

$$I_{11} = I_0 + i_{out} \qquad (3)$$

where I_0 is the biasing current and i_{out} is the output current of the integrator. By substitution from equation (3) into equation (2), we find that:

$$g_{m_{11}} = \sqrt{2\beta I_0 (1 + \frac{i_{out}}{I_0})}$$

$$g_{m_{11}} = g_{m_0}\sqrt{(1 + \frac{i_{out}}{I_0})} \qquad (4)$$

where g_{m_0} is defined as the transistor transconductance for zero input signal. By substitution, from equation(1) into equation (4), we get:

$$i_{out}(s) = \frac{g_{m_0}}{s\,C}\, i_{in}(s)\, \sqrt{1 + \frac{g_{m_0}}{s\,C}\, \frac{i_{in}(s)}{I_0}}. \qquad (5)$$

In the $\Sigma\Delta$ integrators, we have $\frac{A_{int}}{T} = \frac{g_{m_0}}{C}$. By the substitution in equation (5), we get:

$$i_{out}(s) = \frac{A_{int}}{s\,T}\, i_{in}(s)\, \sqrt{1 + \frac{A_{int}}{s\,T}\, \frac{i_{in}(s)}{I_0}}. \qquad (6)$$

From equation(6), we can see that harmonic distortion can be reduced either by increasing the biasing current I_0 or by decreasing the integrator gain A_{int}. For a low power design, it is preferable to decrease the integrator gain A_{int}. Note that the main disadvantage of decreasing A_{int} is the corresponding increase in the integrating capacitance C.

Using equation(6), we show in Fig.3 the normalized output current $\frac{i_{out}}{I_0}$ in function of the normalized input current $\frac{i_{in}}{I_0}$ and the integrator gain A_{int}. In Fig.4, $\frac{i_{out}}{I_0}$ is plotted in function $\frac{i_{in}}{I_0}$ for different values of A_{int}. From these figures, it is obvious that very small values of A_{int} are required in order to have a reasonably linear input-output behavior.

The integrators gains and feedback DAC coefficients of two third order continuous-time $\Sigma\Delta$ modulators, $\Sigma\Delta_1$ and $\Sigma\Delta_2$, are listed in table I. These modulators result from a discrete-time to continuous-time transformation method described in [7]. Both modulators have the same noise transfer function: $\Sigma\Delta_1$ is scaled such that A_{int_1} is very small, and $\Sigma\Delta_2$ is scaled such that A_{int_1} is maximum. The circuits of the integrators have been designed and then used with ideal DACs and comparator models to simulate a complete $\Sigma\Delta$ modulator. The simulation results are shown in Fig.5, where we can see that the third harmonic of $\Sigma\Delta_1$ is significantly lower than that of $\Sigma\Delta_2$. Since the integrator structure is fully differential, even order harmonics are highly attenuated. Note that in this simulation, the transistors are perfectly matched.

B. Mismatch

In order to introduce mismatch, an ideal current source was added in parallel with transistor M_1, Fig.2. The value of this current source is 1% of the current flowing in M_1. In Fig.6, we show the difference between a perfectly matched circuit and a circuit with 1% mismatch. We can notice the slight rise of the second harmonic and the presence of an offset component.

TABLE I
Integrators gains and feedback DAC coefficients.

	A_{int_1}	A_{int_2}	A_{int_3}
$\Sigma\Delta_1$	0.03	0.50	2.00
$\Sigma\Delta_2$	0.18	0.38	2.00
	Coeff_1	Coeff_2	Coeff_3
$\Sigma\Delta_1$	0.50	0.10	0.11
$\Sigma\Delta_2$	0.50	0.54	0.45

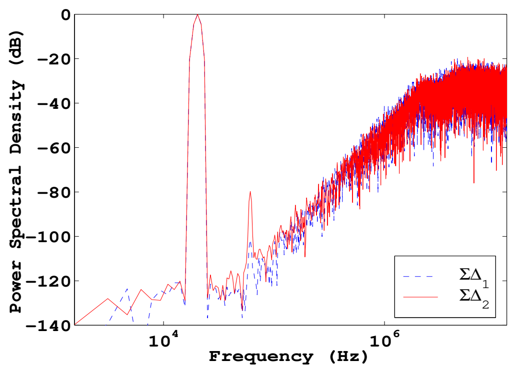

Fig. 5. The third harmonic of $\Sigma\Delta_1$ is 20dB lower than that of $\Sigma\Delta_2$, (input signal = -6 dB, 16384 pts FFT).

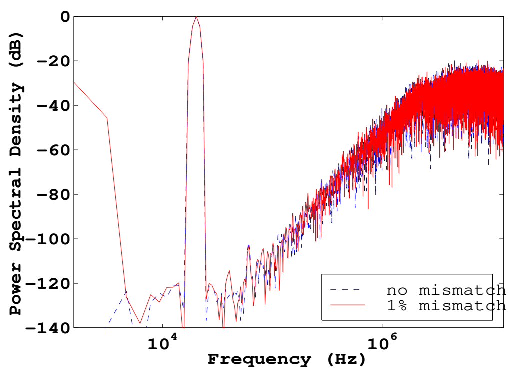

Fig. 6. Mismatch slightly increases the second harmonic and introduces an offset component, (input signal = -6 dB, 16384 pts FFT).

III. Systematic Design of the Current Mode Integrators

In this section, we present a systematic method to design continuous-time $\Sigma\Delta$ modulators with current-mode integrators, Fig.7.

A. Discrete-time to Continuous-Time Transformation

The first problem we face in the design of continuous-time $\Sigma\Delta$ modulators with return-to-zero feedback, is how to find the coefficients of the desired noise transfer function. Since discrete-time $\Sigma\Delta$ modulators are easier to design and simulate, we have chosen to start from the coefficients of a well-known discrete-time $\Sigma\Delta$ modulator, and then use a transformation method to get the equivalent continuous-time $\Sigma\Delta$. A discrete-time to continuous-time transformation method, based on the modified z transform technique, has been introduced in [8] and [7]. Using this transformation method we can get the continuous-time $\Sigma\Delta$ coefficients taking into account the return-to-zero feedback signal. As described in section II.A., these coefficients should be scaled, using equation(6), in order to reduce harmonic distortion due to g_m variation.

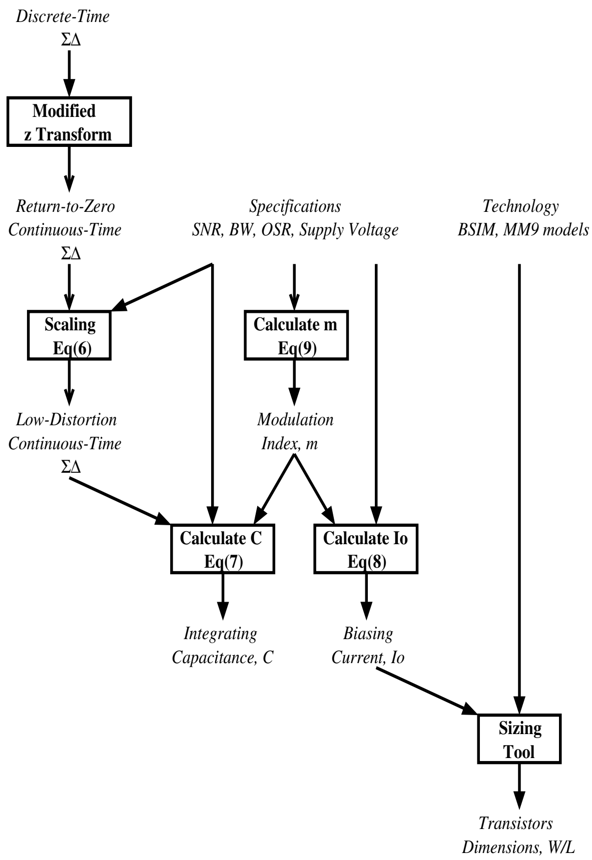

Fig. 7. Systematic design method of current-mode integrators for continuous-time $\Sigma\Delta$ modulators.

B. Circuit Design

Thermal noise calculations determine the minimum integrating capacitance C, and the minimum biasing current I_0 necessary to achieve the required signal-to-noise ratio.

C and I_0 can be expressed in function of the different specifications of the modulator: signal-to-noise ratio SNR, input signal bandwidth BW, oversampling ratio OSR, and the integrator gain A_{int}, by the following relations, derived in [9]:

$$C = \frac{40\ SNR\ 4kT}{A_{int}\ m^2\ A_{\Sigma\Delta}^2\ V_{EG_{1_0}}^2\ OSR} \quad (7)$$

$$I_0 = \frac{40\ SNR\ 4kT\ BW}{m^2\ A_{\Sigma\Delta}^2\ V_{EG_{1_0}}} \quad (8)$$

where the modulation index $m = \frac{I_{in_{max}}}{I_0}$ can be expressed in function of the effective gate voltages, $V_{EG_{1_0}} = (V_{GS_1} - V_{TH_1})_{I_{in}=0}$ and $V_{EG_{3_0}} = (V_{GS_3} - V_{TH_3})_{I_{in}=0}$, by the following relation [9]:

$$\sqrt{1+m}\ (V_{EG_{1_0}} + V_{EG_{3_0}}) - \sqrt{1-m}\ V_{EG_{1_0}} - V_{TH_1} = 0 \quad (9)$$

$A_{\Sigma\Delta}$ is the gain of the input signal which gives maximum signal-to-quantization-noise ratio, usually $A_{\Sigma\Delta}$ is equal to 0.5.

Knowing the biasing current and the effective gate voltages, we can calculate the dimensions of the differ-

TABLE II

Specifications of the 3rd order $\Sigma\Delta$ modulator.

$SNDR$	80 dB
BW	100 kHz
OSR	128
f_s	25.6 MHz
A_{int_1}	0.03
$A_{\Sigma\Delta}$	0.5

ent transistors in the integrator. For this, we used a sizing tool, COMDIAC [10], which uses the complete BSIM and MM9 models to size transistors.

Note that the transistors lengths have to be sufficiently large to reduce the $\frac{1}{f}$ noise.

C. Design Automation

The systematic design method, described above and illustrated in Fig.7, has been implemented in a design automation program. This program takes the different specifications of the $\Sigma\Delta$ modulator as input and generates in the output a sized netlist of the current-mode integrator.

IV. Design Examples

Using the design automation program described in the previous section, the third order modulator $\Sigma\Delta_1$ of table I has been designed for the specifications listed in table II. The circuit characteristics of the generated netlist are listed in table III. One important advantage of the design automation program is that very little effort is required to design the modulator in a different technology process. Circuit I is in a 0.6μm process and Circuit II is in a 0.18μm process. These circuits have been simulated and identical performances have been achieved. Circuit II has been implemented in a 0.18μm CMOS process, with polysilicon/n-well capacitors. Measurement results from silicon implementation of Circuit II matched the expected performances and circuit characteristics of table I and II. The complete circuit including the biasing circuit has a power consumption of 5mW.

TABLE III

First integrator circuit characteristics.

	Circuit I	Circuit II
Technology Process	0.6μm	0.18μm
Supply Voltage	3.0 V	1.8 V
Modulation Index, m	0.8	0.7
Integrating Capacitance, C	212 pF	794 pF
Biasing Current, I_0	64μA	150μA
Power Consumption	1.15 mW	1.62 mW

V. Conclusion

In this paper, we have analyzed the main sources of harmonic distortion in current-mode continuous-time $\Sigma\Delta$ modulators. The integrator gain of the first integrator has to be very low in order to achieve high linearity. Current mismatch, as high as 1%, has shown to introduce offset, but has little effect on harmonic distortion. A systematic design method has been used to implement a design automation program for current-mode integrators for continuous-time $\Sigma\Delta$ modulators. Two third order modulators have been designed in different technologies. The circuits satisfy the required specifications of linearity and signal-to-noise ratio.

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