LOW-POWER DESIGN OF LOW-VOLTAGE CURRENT-MODE INTEGRATORS FOR CONTINUOUS-TIME $\Sigma\Delta$ MODULATORS.

Hassan Aboushady and Marie-Minerve Louërat
Université Paris VI, Laboratoire LIP6
4 Place Jussieu, 75252 Paris Cedex 05, France
Email: Hassan.Aboushady@lip6.fr

***Abstract*—In this paper, we present a method to design low-power low-voltage current-mirror based integrators for continuous-time $\Sigma\Delta$ modulators. It is shown that, by proper biasing of the mirror transistors, very high modulation index can be achieved at low-voltage supply. Careful analysis of the current-mode integrator shows that there exists an optimum supply voltage for minimum power consumption. Simulation results show that proper choice of the supply voltage can reduce the power consumption of the integrator by 40%.

I. INTRODUCTION

Nowadays, continuous-time $\Sigma\Delta$ modulators are receiving an increasing attention in low-power [1] [2], and high speed [3], applications. Current-mirror based current-mode circuits are also used in high-speed low-voltage applications [4]. Recently, theoritical analysis have shown in [5], that the optimum operating supply voltage for switched-currents circuits are always less than those assigned by the employed process.

In this paper, we present a design method for the high swing cascode current mirror [6], Fig.1. This method is used to obtain the maximum modulation index $m = \frac{I_{in}}{I_0}$, where I_{in} is the input current and I_0 is the biasing current. It is shown, by theoritical analysis and simulations, that maximum modulation index is obtained for supply voltages significantly lower than the maximum supply voltage of a given technology. Then we will define the design equations of a current-mirror based integrator for continuous-time $\Sigma\Delta$ modulator. The biasing current and the capacitance of this integrator are chosen to satisfy the thermal noise requirements and the bandwidth specifications of the modulator. It is found that there exists an optimum operating supply voltage for minimum power consumption of the integrator. Two design examples, of continuous-time $\Sigma\Delta$ integrators, are given to validate the design procedure.

II. CASCODE CURRENT MIRROR MODULATION INDEX

In this section, we will describe a method to bias the cascode current mirror, shown in Fig.1. This method gives maximum modulation index m for a given $V_{EG_{1_0}}$ and $V_{EG_{3_0}}$, the effective gate voltage $(V_{GS} - V_{TH})$ for $I_{in} = 0$, of the mirror transistor M_1 and the cascode transistor M_3 respectively. This method also gives the optimum value for the cascode transistor biasing voltage V_{BC} in order to obtain maximum modulation index.

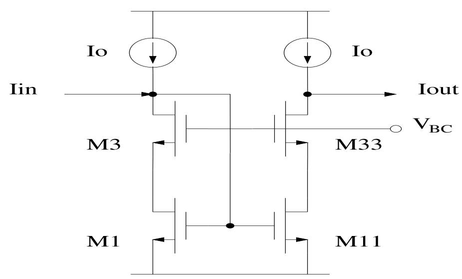

Fig. 1. Cascode current mirror.

Using the simplified square model of a MOS transistor in the saturation region, we get the following relation for the effective gate voltage, (appendix A):

$$V_{EG} = \sqrt{1 \pm m}\ \ V_{EG_0} \tag{1}$$

Condition for the mirror transistor M_1 to be operating in the saturation region:

$$\begin{aligned} V_{DS_1} &\geq V_{GS_1} - V_{TH_1} \\ V_{BC} - V_{GS_3} &\geq V_{GS_1} - V_{TH_1} \\ V_{BC} &\geq V_{EG_1} + V_{EG_3} + V_{TH_3}. \end{aligned} \tag{2}$$

Condition for the cascode transistor M_3 to be operating in the saturation region:

$$\begin{aligned} V_{DS_3} &\geq V_{GS_3} - V_{TH_3} \\ V_{GS_1} - V_{DS_1} &\geq V_{GS_3} - V_{TH_3} \\ V_{GS_1} - V_{BC} + V_{GS_3} &\geq V_{GS_3} - V_{TH_3} \\ V_{BC} &\leq V_{EG_1} + V_{TH_1} + V_{TH_3}. \end{aligned} \tag{3}$$

By substitution, from Eq.(1) in Eq.(2) and Eq.(3) we get

$$V_{BC_{min}} = \sqrt{1+m}\ \ (V_{EG_{1_0}} + V_{EG_{3_0}}) + V_{TH_3} \tag{4}$$

$$V_{BC_{max}} = \sqrt{1-m}\ \ V_{EG_{1_0}} + V_{TH_1} + V_{TH_3} \tag{5}$$

In order to get maximum modulation index m we equate these two equations. Equating Eq.(4) and Eq.(5), we get

$$\sqrt{1+m}\ (V_{EG_{1_0}} + V_{EG_{3_0}}) - \sqrt{1-m}\ V_{EG_{1_0}} - V_{TH_1} = 0 \tag{6}$$

Since $V_{BC} = V_{GS_{3_0}} + V_{DS_{1_0}}$ and by substitution in Eq.(5) we can deduce the value of V_{DS_1}

$$V_{DS_1} = \sqrt{1-m}\ \ V_{EG_{1_0}} - V_{EG_{3_0}} + V_{TH_1} \tag{7}$$

Knowing V_{DS_1}, we can estimate V_{TH_3} and deduce V_{BC}.

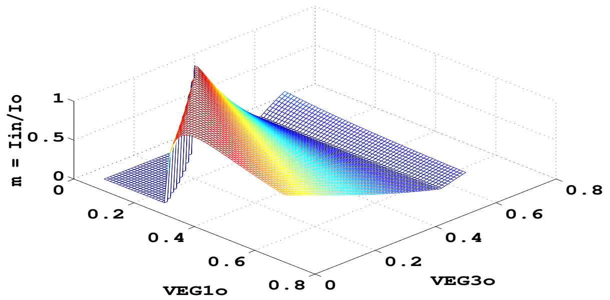

Fig. 2. The modulation index, m, in function of $V_{EG_{1_0}}$ and $V_{EG_{3_0}}$ with $V_{TH} = 0.566$, Eq.(6).

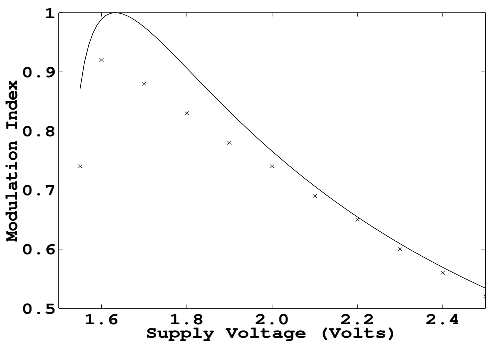

Fig. 3. The modulation index m in function of the supply voltage V_{DD}, $V_{EG_{3_0}} = 0.15$V and $V_{GS_{1_0}} = \frac{V_{DD}}{2}$, (-) Calculated using Eq.(6), (x) measured by simulation.

Using equation (6), the modulation index m can be calculated in function of $V_{EG_{1_0}}$ and $V_{EG_{3_0}}$. This is illustrated in Fig.2, for a $0.25\mu m$ process, with $V_{TH_1} = 0.566$V. From Fig.2, we can see that very high values of the modulation index m can be obtained for small values of $V_{EG_{1_0}}$ and $V_{EG_{3_0}}$. This is an interesting result which supports what has already been claimed that current mode circuits are adapted to operate at low voltage [5]. In Fig.3, Eq.(6) is used to plot the modulation index in function of the supply voltage V_{DD}, $V_{EG_{3_0}}$ is fixed to 0.15V. Although Eq.(6) was derived from the simple square model of the MOS transistor, the simulation results of the modulation index, shown in Fig.3, are very close to the values predicted by the equation.
It is well-known that in analog circuits low voltage supply does not necessarly mean lower power consumption. In the following section, we will develop relations for the biasing current, I_0, of a $\Sigma\Delta$ integrator. We will see that there exists an optimum supply voltage, V_{DD}, where minimum power consumption is obtained.

III. Design of the Current Mode Integrators

A differential current-mode second-order continuous-time $\Sigma\Delta$ modulator is shown in Fig.4. Each integrator has a gain A_{int_1} and A_{int_2} for the first and the second integrator respectively. The feedback coefficients are realized using two feedback DACs. Fig.5 shows the first integrator with the feedback

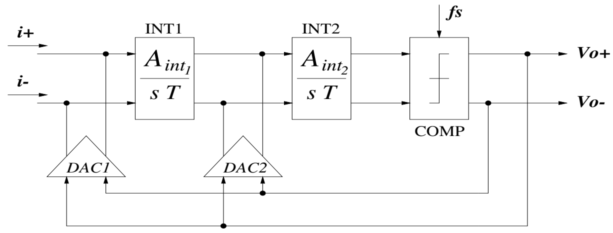

Fig. 4. Differential current-mode continuous-time $\Sigma\Delta$ Modulator.

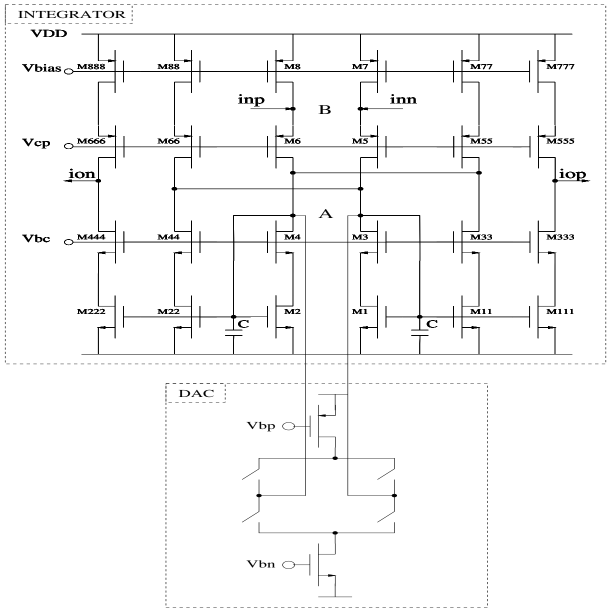

Fig. 5. Differential current-mode integrator with feedback DAC.

DAC. The integrator circuit depicted in Fig.5 is similar to current integrator presented in [4], except that the input signal is applied to node B instead of node A. The reason behind this is to reduce the input impedance of the integrator. The feedback switched current sources have sufficiently high output impedance to draw current into node A.
Neglecting output conductances and parasitic capacitances and assuming identical transistors, small-signal analysis of the integrator circuit yields the following transfer function:

$$H(s) = \frac{i_{op} - i_{on}(s)}{i_{ip} - i_{in}(s)} = \frac{g_m}{sC} \tag{8}$$

where $g_m = \frac{2\ I_0}{V_{EG_{1_0}}}$ is the transconductance of the mirror transistor M_1, and C is the integrating capacitance.
Comparing Eq.8 to the transfer function of the $\Sigma\Delta$ integrator, shown in Fig.4, it is obvious that for proper operation of the modulator the following relation must be satisfied:

$$\frac{g_m}{C} = \frac{A_{int}}{T} = A_{int}\ \ f_s \tag{9}$$

where f_s is the sampling frequency of the modulator.
In order to reduce power consumption we would like the biasing current, I_0, to be as small as possible. This can be accomplished either by having a small tranconductance, g_m, or

a small effective gate voltage, $V_{EG_{1_0}}$, for the mirror transistor M_1. Assuming that node A, Fig.5, is biased at half the supply voltage, then $V_{EG_{1_0}}$ is determined by the supply voltage and $V_{GS_{1_0}} = \frac{V_{DD}}{2}$.
From relation (9), we can see that a small g_m will necessarily mean a small integrating capacitance C. However, the value of C must be chosen carefully to satisfy the signal-to-thermal-noise-ratio, SNR_{Th}, requirements of the $\Sigma\Delta$ modulator.

In the following, we will present a design procedure used to find the minumum integrating capacitance, C, required to achieve a given SNR_{Th}. Starting from this capacitance, C, we can find the transconductance, g_m, for the integrator and the corresponding biasing current I_0.

The effective gate voltage of the integrator PMOS current source is taken equal to the effective gate voltage of the NMOS mirror transistors: $g_m = g_{m_n} = g_{m_p}$. Since the biasing current of the DAC is equal to $\frac{I_0}{2}$, we can say that: $g_{m_{dac}} = \frac{g_{m_{int}}}{2} = \frac{g_m}{2}$. The cascode transistors have negligible effect on the input referred thermal noise power. The power spectral density of thermal noise at the integrator input can be expressed by [7]:

$$S_i = 40\ g_m\ 4KT. \tag{10}$$

The signal bandwidth in a $\Sigma\Delta$ modulator is defined by: $\frac{fs}{2\ OSR}$, where OSR is the oversampling ratio. From Eq.(9), we can say that $f_s = \frac{1}{A_{int}} \frac{g_m}{C}$. The input referred noise power is then equal to:

$$\overline{i_{in}^2} = \frac{5}{A_{int}} \frac{g_m^2}{C} \frac{4kT}{OSR} \tag{11}$$

On the other hand, the signal power can be defined as:

$$\text{Signal Power} = \frac{1}{2}\ A_{\Sigma\Delta}^2\ m^2\ I_0^2 \tag{12}$$

where $A_{\Sigma\Delta}$ is the gain of the input signal which gives maximum signal-to-quantization-noise ratio, usually $A_{\Sigma\Delta}$ is equal to 0.5. From Eq.(11) and Eq.(12), and substituting I_0 by $\frac{g_m}{2} V_{EG_{1_0}}$, we find the following expression for the integrating capacitance:

$$C = \frac{40\ SNR_{Th}\ 4kT}{A_{int}\ m^2\ A_{\Sigma\Delta}^2\ V_{EG_{1_0}}^2\ OSR}. \tag{13}$$

By substitution, from Eq.(13) into Eq.(9) and after some manipulations, we get the following relation for the biasing current:

$$I_0 = \frac{40\ SNR_{Th}\ 4kT\ BW}{m^2\ A_{\Sigma\Delta}^2\ V_{EG_{1_0}}}. \tag{14}$$

Using Eq.(13) and Eq.(14), and for the $\Sigma\Delta$ modulator specifications listed in table I, we show, in Fig.6 and Fig.7, the effect of reducing the supply voltage on the integrating capacitance and the power consumption, respectively. It is shown that, there exists an optimum supply voltage where power consumption is minimum. This is same supply voltage where maximum modulation index was obtained, Fig.3. This comes from the fact that the biasing current is inversely proportional to the square of the modulation index, Eq.(14).

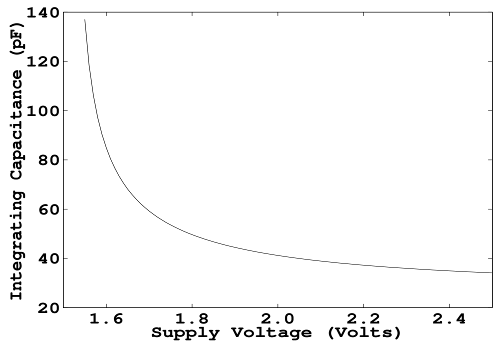

Fig. 6. The integrating Capacitance, C, in function of the supply voltage V_{DD}, Eq.(13), $V_{EG_{1_0}} = 0.15$V and $V_{GS_{1_0}} = \frac{V_{DD}}{2}$.

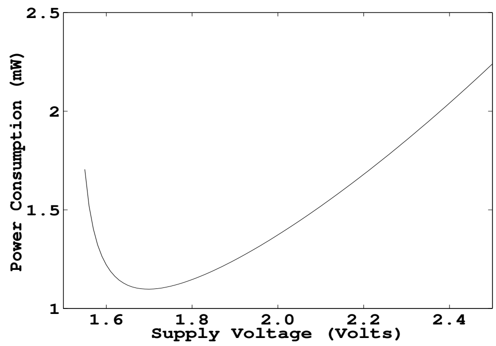

Fig. 7. The biasing current, I_0, in function of the supply voltage V_{DD}, Eq.(14), $V_{EG_{1_0}} = 0.15$V and $V_{GS_{1_0}} = \frac{V_{DD}}{2}$.

In this section, we have developed relations for the integrating capacitance, C, and the biasing current, I_0, in function of the modulation index and the effective gate voltage, $V_{EG_{1_0}}$, of the mirror transistor. In the next section, we will use these equations to design two integrators with different supply voltages.

IV. Design Example

In order to verify the performances predicted by the Eq.(6), Eq.(13) and Eq.(14), developed in the previous section, we will design two continuous-time $\Sigma\Delta$ modulators. The two modulators have the same specifications, described in table I, but are operating at different supply voltages. The two values chosen for the supply voltage are $V_{DD} = 1.7$V and $V_{DD} = 2.5$V. The first is the supply voltage at which minimum power consumption was obtained, Fig.7, and the latter is the maximum supply voltage for the available $0.25\mu m$ process.

The integrators circuit characteristics of each modulator are as described in table II. As predicted in the previous sections, biasing current and power consumption are lower in the low-voltage design than in the maximum supply voltage design. From table II, we can see that the biasing current has been re-

TABLE I

Specifications of the 2^{nd} order $\Sigma\Delta$ modulator.

SNR_{Th}	80 dB
BW	100 kHz
OSR	128
f_s	25.6 MHz
A_{int}	0.5
$A_{\Sigma\Delta}$	0.5

TABLE II

Integrators circuit characteristics ($0.25\ \mu m$ CMOS process).

	Design I	Design II
V_{DD}	1.7 V	2.5 V
$V_{EG_{1_0}}$	0.34 V	0.69 V
$V_{EG_{3_0}}$	0.15 V	0.15 V
m	0.87	0.53
C	27 pF	12 pF
I_0	133 μA	150 μA
Power Consumption	1.36 mW	2.25 mW

duced by 12% and the power consumption of the 1.7V design is 40% lower than the 2.5V design. This is mainly due to the high modulation index achieved in the 1.7V design. On the other hand, the integrating capacitance of the low-voltage design is 56% higher than the maximum power supply voltage design. Note however that the values of the integrating capacitance are lower than those predicted by Eq.(13) in Fig.6. That is because the parasitic capacitances have been taken into account and substracted from the values of Fig.6.

The second order $\Sigma\Delta$ modulator, shown in Fig.4, was simulated using ideal models for all elements except the integrators. The power spectral density of the output from the 1.7V design is identical to the power spectral density of the output from the 2.5V design. Both power spectral densities are shown in Fig.8.

V. Conclusion

In this paper, we have presented a design method for the cascode current mirror. It has been shown that, by properly choosing the effective gate voltages of the mirror transistor and the cascode transistor, very high modulation index can be achieved at low-voltage supply. When used in a $\Sigma\Delta$ modulator, the optimum supply voltage of the current-mode integrator, where power consumption is minimum, is significantly lower than the maximum supply voltage. This makes current-mode circuits particularly well-suited for low-voltage operation. The theoritical analysis has been confirmed by the realization of two integrators for continuous-time $\Sigma\Delta$ modulator. The integrator operating at low-voltage supply consumes 40% less power than the integrator operating at maximum supply voltage.

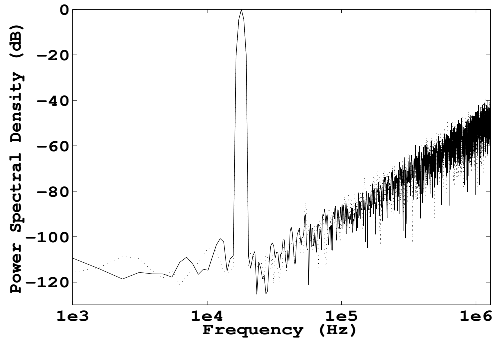

Fig. 8. The power spectral density of a second order $\Sigma\Delta$ modulator with ideal models for all elements except the integrators, (-) design I (1.7V), (:) design II (2.5V), (input signal = -6 dB, 32768 pts FFT).

A Appendix

Starting from the simple square model of a MOS transistor in the saturation region:

$$I = \frac{\beta}{2}(V_{GS} - V_{TH})^2 = \frac{\beta}{2}V_{EG}^2$$

The effective gate voltage, V_{EG}, can be written as:

$$V_{EG} = \sqrt{\frac{2I}{\beta}} = \sqrt{\frac{2(I_0 \pm I_{in})}{\beta}}$$

$$V_{EG} = \sqrt{1 \pm m}\ \sqrt{\frac{2I_0}{\beta}} = \sqrt{1 \pm m}\ V_{EG_0}$$

where, $m = \frac{I_{in}}{I_0}$, is the modulation index.

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