Models for Delay Estimation taking into account both Cross-Talk and Wire Resistance for Timing Analysis

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Abstract : While transistor gate lengths are continuously decreasing, signal inter-coupling capacitance are increasing with respect to substrate capacitance. One of the important effects of this parasitic capacitance is the modification of the signal propagation time which becomes dependant on coupling signals. In this paper, we present different methods which allow to estimate worst case delay in function of coupling signal transient periods. These estimations are intended to be used during timing analysis of circuits with large number of transistors (several millions). A special care has been taken in order to minimize CPU time and data storage size. In addition, it is also very important to take into account wire resistance in recent technologies. Our estimations allow to account for these resistance in RC trees.

1 INTRODUCTION.

During timing analysis which takes into account interconnect resistance, gate delay and wire delay are completely decoupled. Gate load are often modeled either by a single capacitance or by a π-network [5]. The line propagation time between the transmitter and the receiver is determined using for example Elmore's delay [3][4]. In CMOS technologies, as a first order, we can consider that gate propagation time depends only on the *fixed* load, and only slightly on the *variable* input signal slope. A simple iteration in which input slopes are first determined, followed by a second one in which propagation time is computed, allow to obtain an approximated delays within 5% with respect to Spice-like simulators [1].

Unfortunately, this approach can not be used to account for signal coupling capacitance, since the load seen by the gates is subjected to change depending on coupling signal transients. This load variation has a direct influence on gate propagation time and RC network delay[6].

In this paper, we propose different methods in order to take into account this effect, while minimizing both CPU time and data storage size in the same time.

First, we consider modifications introduced in Elmore delay equation for RC networks using Miller effect to take into account signal coupling capacitance. Next, we consider modifications introduced to the load seen by a given gate in first and third orders. Finally, means to correct for Miller's effect limitations are presented.

2 MILLER EFFECT.

Case of a single capacitance :

Miller effect allows to evaluate for each coupling capacitance, an equivalent capacitance C_{eq} with respect to the substrate. The current in the coupling capacitance between the two signals 1 and 2 is determined assuming that these two signals are driven by ideal voltage sources (Fig 1).

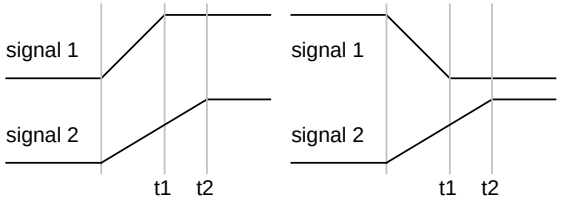

Figure 1

In the case that the two signals switch in the same direction, we have for signal 1 (case T1<T2) :

$$C_{eq} = C \cdot \frac{T2 - T1}{T2} \quad (1)$$

And for signal 2 :

$$C_{eq} = 0.C \quad (2)$$

In the case that the two signals switch in the same direction, we have for signal 1 (case T1<T2) :

$$C_{eq} = C \cdot \frac{T2 + T1}{T2} \quad (3)$$

and for signal 2 :

$$C_{eq} = 2.C \quad (4)$$

As a first order, in CMOS circuits, it is possible to assume that all slopes are almost identical, such that we can use the 0C/2C model, with only a slight error. However, if we also want to take into account differences in signal slopes, iterative methods should be employed. Initially, the 0C/2C (eq (2) and (4)) model is used in order to obtain a first evaluation of gate loads and to deduce the corresponding approximate signal slopes. It becomes possible, then, to recalculate more precisely gate loads and to deduce the corresponding signal slopes. This operation is repeated until the convergence of all signal slopes. Unfortunately, in some particular cases, this method does not converge. In these cases, as we are usually concerned with worst case delays, we simply retain the iteration –after the first one- that gives the worst case delay.

Interconnections with wire resistance :

While taking into account interconnect wire resistance, signal slopes on nodes are typically not identical. If we want to account for this effect, this involve retaining directly or indirectly electrical information on all nodes. However, this is in contradiction with our goal to minimize data storage size in order to perform timing analysis of large chips. So, we have made the choice of assuming all signal slopes on all nodes of a given network to be identical, and these signal slopes are computed at the output of each gate. Despite of the fact that this choice can be contested, it allows to greatly simplify electrical models as shown in the rest of this paper. In most cases, this choice has not a direct impact on the delay's precision.

3 APPLICATION OF MILLER EFFECT TO ELMORE DELAY

Miller theory can be easily applied when using Elmore delay to estimate interconnect delays due to signal coupling. Elmore delay between two nodes of a network is given by :

$$Ed = \sum_{i \in \xi} Ri \sum_{j \in \delta} Cj \tag{5}$$

where ξ is the ordered set of nodes from the transmitter to the receiver, and δ is the set of nodes which follows node *i*. Changing a capacitance on the network modifies all Elmore delays given by the relation :

$$\Delta Ed = \Delta C \cdot \omega \tag{6}$$

where ω is the sum of common resitances between the transmitter to the receiver and from the transmitter to the changing capacitance. To realize this operation, each capacitance must have a list where each element contains both an Elmore delay reference and the common resistance value ω. When a set of *n* coupling capacitances between two signals are modified, the variation of a particular Elmore delay is given by :

$$\Delta Ed = \sum_{i=1}^{n} (\omega_i \cdot \Delta C_i) \tag{7}$$

This expression used as it is practically useless due to the large amount of data required to be stored if there are many coupling capacitances between the two signals. If signal slopes are assumed to be identical on each node of the network, we can apply Miller theory to simplify this expression as follows: All coupling capacitances are multiplyed by the same constant *m* representing the Miller effect.

$$C_{eq} = m \cdot C \tag{8}$$

And for each capacitance, we have :

$$\Delta C_i = C_{ieq} - C_i \tag{9}$$

So, we can write

$$\Delta C_i = C_i \cdot (m-1) \tag{10}$$

such that the variation of the Elmore delay becomes

$$\Delta Ed = \sum_{i=1}^{n} (\omega_i \cdot C_i \cdot (m-1)) \tag{11}$$

Now, the only coupling-dependant variable is *m*. So, we can write more concisely :

$$\Delta Ed = k \cdot (m-1) \tag{12}$$

with

$$k = \sum_{i=1}^{n} (\omega_i \cdot C_i) \tag{13}$$

Results Interpretation :

We have represented, with the use of only one constant *k*, the Elmore delay variation of a network coupled with an other one through *n* capacitances. This has been made possible by assuming the Miller effect to be the same on all nodes of the network.

4 MODIFICATION OF THE LOAD SEEN BY THE GATE.

The fact of changing the load seen by the gate also changes the gate propagation time. When the load is only represented by a simple capacitance which represents the total capacitance on the network, applying Miller effect becomes obvious. However, this is not so simple when we consider the load as a π network. Thus, we want to determine how does this load change when one or more capacitance change on the network.

In the case of RC trees, the π network can be computed with the 3rd order truncated polynomial of the network admittance [2] :

$$y(p) = y_1 \cdot p + y_2 \cdot p^2 + y_3 \cdot p^3 \tag{14}$$

From this equation, elements constituting the π network (Fig 2) are determined with :

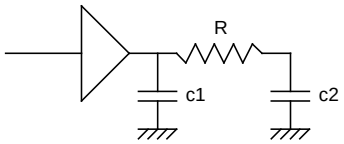

Figure 2

$$R = \frac{-y_3^2}{y_2^3},\ C_2 = \frac{y_2^3}{y_3},\ C_1 = y_1 - C_2 . \tag{15}$$

This admittance is computed recursively from the receiver to the transmitter, by using the resistance and the capacitance transfer functions which are in case of resistance :

$$\begin{cases} y_1u = y_1d \\ y_2u = y_2d - R \cdot y_1d^2 \\ y_3u = y_3d - 2 \cdot R \cdot y_1d \cdot y_2d + R^2 \cdot y_1d^3 \end{cases} \tag{16}$$

and in case of capacitance :

$$\begin{cases} y_1u = y_1d + C \\ y_2u = y_2d \\ y_3u = y_3d \end{cases} \tag{17}$$

In case of *n* parallel branches, we have :

$$\begin{cases} y_1u = \sum_{i=1}^{n} y_1d_i \\ y_2u = \sum_{i=1}^{n} y_2d_i \\ y_3u = \sum_{i=1}^{n} y_3d_i \end{cases} \tag{18}$$

With $y_i d$ representing the terms corresponding to the admittance on the nodes after the element, and $y_i u$ representing the terms corresponding to the admittance on the nodes before the element. By construction, the term y_1 represents the total capacitance of the network. Now, we show that it is possible to determine how does the y_i seen by the gate change in function of the variation of only one capacitance in the network.

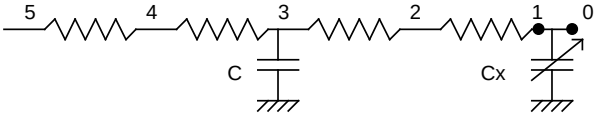

Figure 3

When the capacitance C_x, and only C_x, change, we can write for node 1 in Fig 3 :

$$\begin{cases} \Delta y_1 1 = \Delta y_1 0 + \Delta C_x \\ \Delta y_2 1 = \Delta y_2 0 \\ \Delta y_3 1 = \Delta y_3 0 \end{cases} \rightarrow \begin{cases} \Delta y_1 1 = \Delta C_x \\ \Delta y_2 1 = 0 \\ \Delta y_3 1 = 0 \end{cases} \quad (19)$$

While for the other capacitance *C* before C_x, we have :

$$\begin{cases} \Delta y_1 u = \Delta y_1 d + \Delta C \\ \Delta y_2 u = \Delta y_2 d \\ \Delta y_3 u = \Delta y_3 d \end{cases} \rightarrow \begin{cases} \Delta y_1 u = \Delta y_1 d \\ \Delta y_2 u = \Delta y_2 d \\ \Delta y_3 u = \Delta y_3 d \end{cases} \quad (20)$$

Capacitance, then, propagate without any effect on the variation of admittance. In case of the resistance *R* before C_x, we have the following recursive equations :

$$\begin{cases} \Delta y_1 u = \Delta y_1 d \\ \Delta y_2 u = \Delta y_2 d - 2.R.\Delta y_1 d.y_1 d \\ \Delta y_3 u = \Delta y_3 d - 2.R.\Delta y_1 d.y_2 d - 2.R.y_1 d.\Delta y_2 d + 3.R^2.\Delta y_1 d.y_1 d^2 \end{cases} \quad (21)$$

By recursion, we can show that, on the emitter, we have :

$$\begin{cases} \Delta y_1 = \Delta C_x \\ \Delta y_2 = \Delta C_x \cdot \alpha_2 \\ \Delta y_3 = \Delta C_x \cdot \alpha_3 \end{cases} \quad (22)$$

Coefficient calculation takes place in the same time as that of admittance using the following recursive equations :

$$\begin{cases} \alpha_2 u = \alpha_2 d - 2 \cdot R \cdot y_1 d \\ \alpha_3 u = \alpha_3 d - 2.R.y_2 d - 2.R.\alpha_2 d.y_1 d + 3.R^2.y_1 d^2 \end{cases} \quad (23)$$

For the y_2 and y_3 terms, first order truncation is not sufficient. Instead, we use Taylor series as follows :

$$\begin{cases} y_1 = y_1 i + \Delta C_x \\ y_2 = y_2 i + \alpha_2.\Delta C_x + \frac{1}{2}.\beta_2.\Delta C_x^2 \\ y_3 = y_3 i + \alpha_3.\Delta C_x + \frac{1}{2}.\beta_3.\Delta C_x^2 + \frac{1}{6}.\gamma_3.\Delta C_x^3 \end{cases} \quad (24)$$

where y_1i, y_2i and y_3i represent the initial admittance. In the same way as α_2 and α_3, we can deduce β_2, β_3 and γ_3 as follows :

$$\begin{cases} \beta_2 u = \beta_2 d - 2.R \\ \beta_3 u = \beta_3 d - 4.\alpha_2.R - 2.\beta_2 d.R.y_1 d + 6.R^2.y_1 d \\ \gamma_3 u = \gamma_3 d - 6.y_2 d.R.\beta_2 d + 6.R^2 \end{cases} \quad (25)$$

These five coefficients : α_2, α_3, β_2, β_3 and γ_3 allow to calculate exactly the coefficient y_i variations seen by the gate load, and hence the π-network, when the capacitance C_x changes. Strictly speaking, this approach is valid when only one capacitance changes. Practically, we can apply this method in a large category of cases by changing more than one capacitance without loosing much precision. In this case, we have for a set of *n* capacitance between two coupled signals :

$$\begin{cases} y_1 = y_1 i + \sum_{i=1}^{n} \Delta C_i \\ y_2 = y_2 i + \sum_{i=1}^{n} \alpha_{2i}.\Delta C_i + \frac{1}{2}.\sum_{i=1}^{n} \beta_{2i}.\Delta C_x^2 \\ y_3 = y_3 i + \sum_{i=1}^{n} \alpha_{3i}.\Delta C_x + \frac{1}{2}.\sum_{i=1}^{n} \beta_{3i}.\Delta C_x^2 + \frac{1}{6}.\sum_{i=1}^{n} \gamma_{3i}.\Delta C_x^3 \end{cases} \quad (26)$$

Like in the case of Elmore delays, this approach is not useful if we have to store for each capacitance between two signals these five coefficients. However, we can proceed in the same way as that of the Elmore delay calculation by considering that all signal slopes are identical on all network nodes. We can then calculate the variation of the capacitance due to Miller effect. With equation (10), we have :

$$\begin{cases} y_1 = y_1 i + x_{11}.(m-1) \\ y_2 = y_2 i + x_{12}.(m-1) + x_{22}.(m-1)^2 \\ y_2 = y_3 i + x_{13}.(m-1) + x_{23}.(m-1)^2 + x_{33}.(m-1)^3 \end{cases} \quad (27)$$

where :

$$x_{11} = \sum_{i=1}^{n} C_i \quad (28) \qquad x_{12} = \sum_{i=1}^{n} \alpha_{2i}.C_i \quad (29)$$

$$x_{22} = \frac{1}{2}.\sum_{i=1}^{n} \beta_{2i}.C_i^2 \quad (30) \qquad x_{13} = \sum_{i=1}^{n} \alpha_{3i}.C_i \quad (31)$$

$$x_{23} = \frac{1}{2}.\sum_{i=1}^{n} \beta_{3i}.C_i^2 \quad (32) \qquad x_{33} = \frac{1}{6}.\sum_{i=1}^{n} \gamma_{3i}.C_i^3 \quad (33)$$

Results Interpretation :

In the first part of this paper, we have shown how to take into account the variation of equivalent coupling capacitance in order to determine worst case delay by using Miller effect. It should be noticed that when two signals switch simultaneously, we obtain very accurate results compared to Spice-like simulators. However, this is not considered as the worst case delay.

5 COUPLING NOISE DURING WORST CASE PROPAGATION TIME EVALUATION

We notice that switching noise can either increase or decrease signal dynamic range, and consequently change significantly the corresponding propagation time. This can take place when a signal switches

slightly before or after the moment it is subjected to noise from another switching signal (Fig 4) :

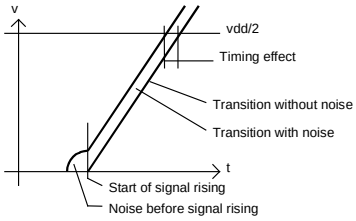

Figure 4

While Miller theory allows to determine, in a relatively accurate way, signal slope during switching, it does not allow to account for the noise effect on signal delay, which may become sometimes very large. Unfortunately, accurate noise calculation is a very time-consuming process. We propose to account for this effect in an rather approximate way by ignoring interconnect resistance. This effect is then modeled under the form of a simple delay time to be added to or subtracted from the gate delay time. In order to determine this noise effect, we use the following equivalent circuit:

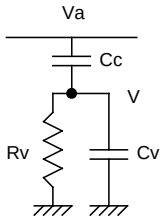

Figure 5

In Fig. 5, R_v is the linearized resistance of the victim signal, C_v is the total victim signal capacitance with respect to the substrate, and C_c is the coupling capacitance between the two signals. We model the signal on the aggressor with a voltage ramp from V_0 to V_1 during a time T, corresponding to a slope k. We have on node V a maximum potential given by:

$$V_{\max} = R_v.C_c.k.\left(1 - e^{-\frac{V_1 - V_0}{R_v.(C_c + C_V).k}}\right) \qquad (34)$$

Total noise is computed by adding all elementary noise from each aggressor. The delay effect is, then, simply evaluated from the noise and the slope of the victim signal as follows:

$$\Delta T = \frac{\sum V_{\max}}{slope} \qquad (35)$$

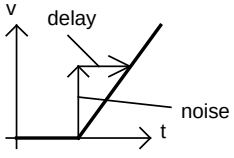

Figure 6

Results Interpretation :

For each signal aggressor, while storing only C_c and C_v, it is possible to consider switching noise effect on signal timing. In addition, we can also evaluate the signal sensitivity with respect to coupling noise. However, the resistance R_v depends only of the victim signal.

6 TIMING ANALYZER USING THE ABOVE MODELS

Data Structures.

Considering the following example :

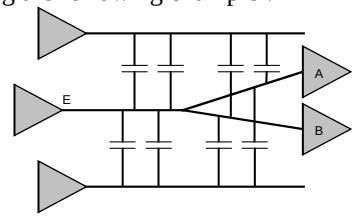

Figure 7

According to the above model, when a signal is stressed by *n* other signals, we need to store for each aggressor the following data :

- Five constants for admittance effect,
- For each victim signal receiver, a constant needed for Elmore effect.
- The capacitance C_c and C_v.

In this simple example shown in Fig. 7, the victim signal E is stressed with two other ones. We thus have only to store the following data needed to evaluate propagation delay :

- y_1i, y_2i, y_3i
- R_v
- A1 :
  - $Ed_{E\to A}$: k
  - $Ed_{E\to B}$: k
  - π : α_2, α_3, β_2, β_3, γ_3
  - Noise : C_c, C_v
- A2 :
  - $Ed_{E\to A}$: k
  - $Ed_{E\to B}$: k
  - π : α_2, α_3, β_2, β_3, γ_3
  - Noise : C_c, C_v

The main advantage of this approach is that the total information size needed to compute propagation delay is independent of the network size. In addition, we have completely decoupled electrical information between all networks.

Algorithm :

In order to determine the propagation delay of a set of N coupled signals using the above data structure, we propose the following algorithm :

To each signal is associated a modified admittance `y'` corresponding to coupling effects, a list of modified Elmore delays `Ed'`, and the total `noise.` Initially, we have already done a timing analyses without taking into account the effect of capacitance coupling and a stability analysis, which allow to determine the possibility of simultaneous switching of two coupled signals.

It has been shown that taking into account signal slopes during Miller effect calculations is an iterative

procedure which can sometimes fail to converge. So, we fix a maximum number of iterations. The stop condition is chosen such that no variation delay exceeds 1ps.
In the algorithm description, we note that S:A is an information A of the data structure corresponding to the signal S.

```
i=1.
While i≤Imax Or Stop Condition is
True :
  For each signal V from N :
    Initialize V:y'=V:y.
    Initialize delay V:Ed'=V:Ed.
    Initialize V:noise=0.
    For each aggressor A of V :
      If A and V can switch
      simultaneously :
        If i=1 :
          Determine Miller effect m
          from eq. (2) and (4).
        Else :
          Determine Miller effect m
          from eq. (1) to (4).
        End If.
        Determine change of V:y'
        from eq. (27).
        Determine noise V:bruit
        from eq. (34).
      End If.
    End For.
    Determine signal slope.
  End For.
  For each signal V from N :
    Determine signal gate delay.
  End For.
End While.
```

USAGE AND LIMITATIONS

In this section, we introduce some examples on the use of such representation. In the following examples gate delay, loaded by a π-network or by a single capacitance is calculated using a Spice-like simulator.
Actual worst case delay are not easily determined using an electrical simulator. When there is only one aggressor, it is possible to sweep the aggressor switching instant at the input in order to determine accurately the worst case delay. In case of several aggressors, we determine the input configuration which allows to obtain the worst case delay by successive approximations.

7 Simulation results :

The used technology is a 0.25µm one. The size of the inverter transistors are 1.25µm/2.5µm. Routing wires are decomposed to multiple elementary RC cells each corresponding to 1µm of wire length. For example, a wire portion of 100µm is represented during simulations with 100 basic cells as shown in Fig 8 :

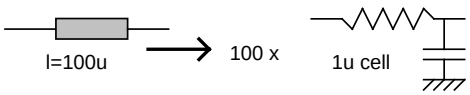

Figure 8

Inverter input capacitance is around 10fF.

Case 1 :

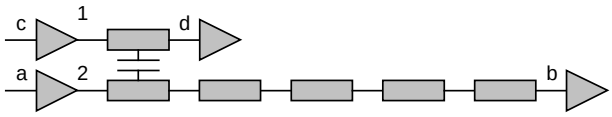

Figure 9

In figure 9, each piece of wire is 100µm long, and has a resistance of 62,5Ω. The substrate capacitance of signal 1 is 16fF, and that of signal 2 is 52fF. The coupling capacitance is 9fF.
Table 1 shows the propagation delay time obtained using the electrical simulator.

Table 1

Eldo	Tp min (pS)	Tp (pS)	Tp max (pS)
A→B	54.6	69.3	83.1
C→D	27.6	33.7	36.3

While table 2 shows those calculated by the proposed model.

Table 2

Models	Tp min (pS)	Tp max (pS)
A→B	54.7	86.2
C→D	29.0	36.2

Obviously, the proposed model has allowed to obtain results very close to the actual simulated ones. However, these results do not show that while calculating the minimum propagation time between nodes C and D, the approximation used to evaluate the admittance seen by the gate does not work. In fact, among the obtained y_i values, negative element values are obtained. Our model implementation handle this case through a first order model by using y_1.
Miller effect modeling has converged in three iterations, with *m*=0,549 for signal 1 and *m*=0 for signal 2.

Case 2 :

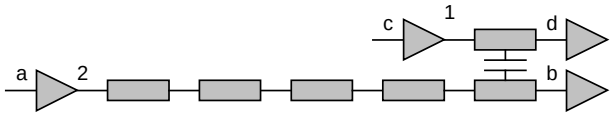

Figure 10

In figure 10, with respect to the previous case, we have only moved the coupling to the end of the second line.
Table 3 shows electrical simulator delay results :

Table 3

Eldo	Tp min (pS)	Tp (pS)	Tp max (pS)
A→B	53.6	69.4	83.8
C→D	27.6	33.4	36.2

While table 4 shows our model ones. :

Table 4

Models	Tp min (pS)	Tp max (pS)
A→B	58.3	86.7
C→D	29.8	35.9

In this case, results are only slightly less accurate, but remain fairly good.

Case 3 :

In the figure 11, the two lines are now coupled through all their length.

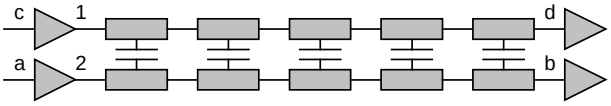

Figure 11

Table 5 shows electrical simulator delay results :

Table 5

Eldo	Tp min (pS)	Tp (pS)	Tp max (pS)
A→B	39.7	79.3	146.8
C→D	39.7	79.3	146.8

While table 6 shows our model ones. :

Table 6

Models	Tp min (pS)	Tp max (pS)
A→B	38.4	154.9
C→D	38.4	154.9

In the case of minimum propagation times, a first order model has been used.

Case 4 :

In figure 12, we have three aggressors and a tree structure:

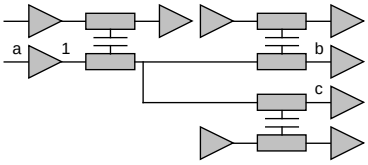

Figure 12

Table 7 shows electrical simulator delay results :

Table 7

Eldo	Tp min (pS)	Tp (pS)	Tp max (pS)
A→B	28.5	67.4	114.0
A→C	28.5	67.4	114.0

While table 8 shows our model ones.

Table 8

Models	Tp min (pS)	Tp max (pS)
A→B	33.5	120.4
A→C	33.5	120.4

In this example, minimum propagation time is slightly less accurate. However, practically this error is not critical since statistically, the three-entry configuration that allows to obtain the shortest delay time is less probable.

8 CONCLUSION :

The accuracy of the proposed model is reasonably good enough for the given examples. However, when line resistance increases with respect to gate equivalent switching resistance, or when coupling is too tight, we observe a gradual degradation of the model accuracy.
If the number of signals, facing a delay calculation problem, is not very large, the fact of systematic determination of worst the case delay compensates the resulting error.

The proposed method has several advantages which helps in the design of timing analyzer tools. First, electrical coupling information between networks has been completely suppressed. Next, a third order method representing the influence of the variation of coupling capacitance on the load seen by the gates, together with the corresponding modifications introduced in the Elmore delay equation, is presented.
This results in a considerable decrease in the amount of information needed per signal as shown in the given examples. In the first one, more than 6000 integers or floats are usually needed in order to represent the two RC networks, whereas only about 20 ones are needed on the proposed representation.
In the same time, once it has been determined which are the signals that risk to switch on the same time, delay estimations and corrections become almost immediate.

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