SWITCH SIZING FOR VERY LOW-VOLTAGE SWITCHED-CAPACITOR CIRCUITS

M. Dessouky *M.-M. Louërat* *A. Kaiser*

Ain Shams University-ECE
1 El-Sarayat St., Cairo, Egypt
Mohamed.Dessouky@ieee.org

UPMC 55/65-LIP6-ASIM
4 Place Jussieu, Paris, France
Marie-Minerve.Louerat@lip6.fr

IEMN-ISEN-UMR CNRS 9929
41 Bld. Vauban, Lille, France
Andreas.Kaiser@isen.fr

ABSTRACT

A simple series switch sizing procedure is presented taking into account very low-voltage switch operation. Under these conditions, the switch conducts not only in the linear region, but also in saturation. The procedure has been implemented in an automatic sizing tool and used to optimize separately switch sizes in a very low-voltage Delta-Sigma modulator. This has allowed to minimize clock feedthrough while satisfying all settling requirements.

1. INTRODUCTION

The increasing interest in low-voltage, low-power integrated circuits has led to modifying the existing circuit techniques. In switched-capacitor (SC) circuits, reducing the supply voltage increases drastically the switch resistance. Recently, two main approaches were introduced to allow very low-voltage operation: The switched op-amp technique eliminates critical switches [1], [2], while the bootstrapped switch technique allows rail-to-rail operation of a single *n*-switch in standard CMOS processes [3], [4], [5]. Obtained results show the feasibility of very low-voltage high performance circuits using common SC techniques in advanced low-voltage processes.

The above mentioned techniques allow all switches to be turned on, but not always in the linear region. Since the switch overdrive voltage $V_{EG} = V_{GS} - V_{TH}$ is only a few hundred mV at most, it is not possible to size switches by only taking into account their on-resistance [6]. Switch sizing is an important aspect which affects the overall performance of SC circuits. Since the switch resistance depends also on the source and drain voltages, under-sized switches may directly increase harmonic distortion due to un-complete settling. On the other hand, over-sized switches increase clock feedthrough. In [7], a simplified integrator model is presented that takes into account the finite switch resistance. However, only linear region operation is considered which is not sufficient for very low-voltage operation as will be shown later. In this paper, a simple method is introduced in order to allow series switch sizing in very low-voltage SC circuits.

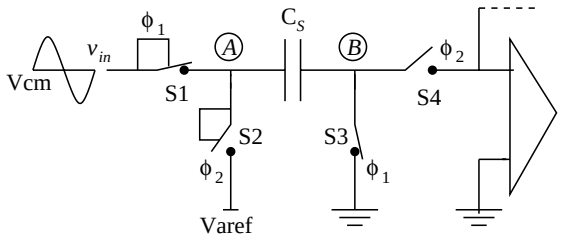

Figure 1. Low-voltage SC integrator: Input sampling.

2. SWITCH SYNTHESIS

Switches in their on-state are always considered as a small series resistance. However, the small switch overdrive does not guarantee its operation in the linear region. Specifically, if the switch has a high drain-source voltage in its off-state, the switch starts conducting in the saturation region if $V_{DS} > V_{EG}$ [6]. The drain-source voltage then decreases due to charging/discharging the series capacitance and eventually the switch enters in the linear region.

Fig. 1 shows the sampling and integration phases of the sampling capacitor in a SC integrator based on the low-voltage SC schemes presented in [5]. The reference potential V_{aref} might be either V_{SS} or $V_{cm} = V_{DD}/2$ [5]. Switches S1 and S2 are bootstrapped switches while S3 and S4 are n-switches. During the integration phase (ϕ_2), node B is connected to the virtual ground opamp input (at V_{SS}) while node A is connected to V_{aref}. First, consider the sampling phase (ϕ_1): Node B does not change its potential since it is also connected to V_{SS}. The drain-source voltage of S3 remains at zero potential which guarantees the operation of S3 in the linear region. This in not the case for S1 which connects node A to the input signal that is assumed to swing from V_{DD} to V_{SS}. At both extremes, the switch drain-source voltage is thus around $\|V_{DD} - V_{aref}\|$ at the switching moment. If the overdrive of the bootstrapped switch V_{EG} is less than its drain-source voltage, S1 then *starts* conducting in the saturation region. It then enters the linear region as the charging goes on and the drain-source voltage moves towards zero. During the integration phase (ϕ_2), C_S is discharged through switches S2 and S4. Similar to S1, according to the input voltage, S2 can also start conducting in the saturation region

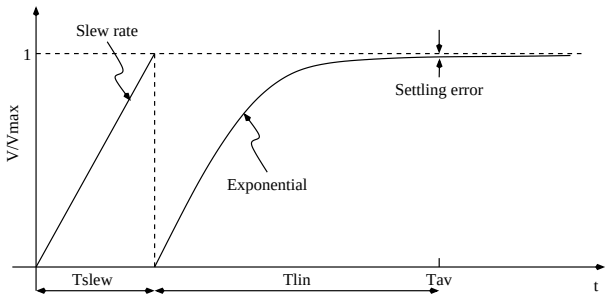

Figure 2. Voltage across C_S: Worst-case settling.

then moves to the linear region. On the other hand, S4 is always in the linear region while conducting.

During either the sampling or integration phases there exist two series switches charging/discharging the sampling capacitor C_S. One of these switches is always in the linear region while the other may occasionally starts conducting in the saturation region, according to the input signal, in which the switch's current is held constant at I_{Dsat} and the switch is said to *slew* at a rate given by

$$SR_{switch} = \frac{I_{Dsat}}{C_S} \tag{1}$$

for a certain time t_{slew}. The switch then enters the linear region where charging of C_S is continued with a time constant τ for a certain time $t_{lin} = t_{av} - t_{slew}$, where t_{av} is the available time. In the linear region the two series switches can be represented by linear resistances R_1 and R_2. Charging accuracy is measured using the settling error ϵ such that

$$t_{lin} = (R_1 + R_2)C_S ln\left(\frac{1}{\epsilon}\right) = t_{lin1} + t_{lin2} \tag{2}$$

where

$$t_{lin1} = R_1 C_S ln\left(\frac{1}{\epsilon}\right) \qquad t_{lin2} = R_2 C_S ln\left(\frac{1}{\epsilon}\right) \tag{3}$$

Switch sizes are chosen to yield a certain settling error ϵ in a given period of time t_{av}. During sizing, t_{av} is divided into slewing t_{slew}, and linear t_{lin} times. From equation (2), the linear settling time t_{lin} is further divided into t_{lin1} and t_{lin2}, given by equations (3), each depending on one of the two switches, such that

$$t_{av} = t_{slew} + t_{lin} = t_{slew} + t_{lin1} + t_{lin2} \tag{4}$$

This allows the two switches to be sized *separately* given only the sampling capacitance C_S. The slewing switch determines t_{slew} and t_{lin1} while the other switch determines t_{lin2}. The following section describes how sizes are calculated from these parameters.

3. SWITCH SIZING PROCEDURE

In this section, we discuss the procedure for switch sizing, given the following input parameters:

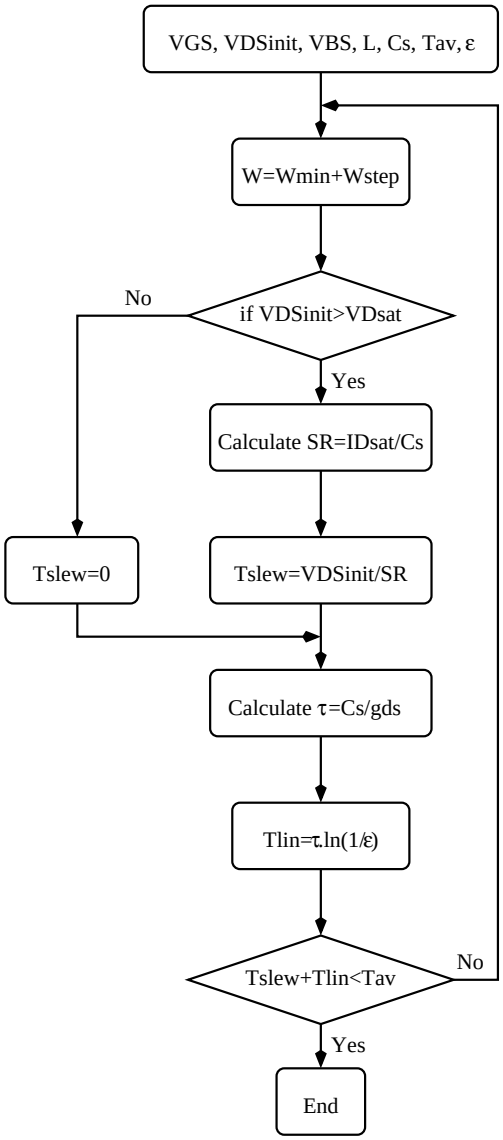

Figure 3. Automatic switch sizing procedure.

- Transistor length.
- Series capacitance C_S.
- Gate-source voltage V_{GS}.
- Initial drain-source voltage V_{DSinit}.
- Bulk-source voltage V_{BS}.
- Available time for charging the load capacitance t_{av}.
- Settling error ϵ.

Worst-case settling is assumed by considering that the available time t_{av} will be divided into a slewing time t_{slew} during which the switch slews throughout the voltage range from $V_{DS} = V_{DSinit}$ down to $V_{DS} = 0$ in addition to a linear time t_{lin} during which slewing is neglected and a linear settling to the required settling error is assumed as shown in Fig. 2. The sizing procedure is summarized in Fig. 3. It starts from the minimum transistor width W_{min}. If the transistor starts in the saturation region, it calculates the switch SR using equation (1). The slewing time is then calculated referring to

Fig. 2 by

$$t_{slew} = \frac{V_{DSinit}}{SR_{switch}} \quad (5)$$

The linear time is then calculated using

$$t_{lin} = \tau ln\left(\frac{1}{\epsilon}\right) = \frac{C_S}{g_{ds}} ln\left(\frac{1}{\epsilon}\right) \quad (6)$$

Then if the total time $t_{slew} + t_{lin}$ is less then the given available time t_{av}, then sizing is accomplished, if not the process is repeated by incrementing the transistor width which in turn increases the saturation current (and consequently the switch SR) and the drain-source conductance g_{ds} both leading to decrease t_{slew} and t_{lin} respectively.

4. EXAMPLE: BOOTSTRAPPED SWITCH SIZING

The bootstrapped switch shown in Fig. 4 [5] as well as the accompanying bootstrapping circuit are both sized based on the basic switch sizing procedure described in the previous section. This section introduces the corresponding automatic sizing procedure. It has the same input parameters as that of a simple switch (section 3).

First, the main switch MNSW is sized. Secondly, the value of C_{offset} is determined. Since C_{offset} is first charged to V_{DD}, the gate voltage of MNSW at the end of ϕ_1 is given by

$$v_G = \frac{C_{offset}}{C_{offset} + C_G}(v_{in} + V_{DD}) \quad (7)$$

while the voltage on the offset capacitance is given by

$$v_{offset} = \frac{C_{offset}}{C_{offset} + C_G} V_{DD} - \frac{C_G}{C_{offset} + C_G} v_{in} \quad (8)$$

where C_G is the parasitic capacitance on the gate side of C_{offset} given by

$$C_G = C_{gsw} + C_{g1} + C_{g8} + C_{g6} + C_{g4} + C_{wellB} \quad (9)$$

The capacitance C_{offset} must be large enough to supply sufficient charge to the gate of MNSW when it is turned on. A significant voltage reduction across C_{offset}, due to capacitance division, might drive node B (and consequently the N-well of MP4) below V_{DD} causing latch-up. The capacitance C_{offset} is thus chosen to at least 10 times that of C_G. Given the size of MNSW, C_G is estimated to be $C_G = 5C_{gsw} + C_{wellB}$.

Finally, the sizes of the remaining switches in the bootstrapping circuit are determined using the same procedure described in section 3. Bias voltages which are easily determined from Fig. 4. The load capacitance seen by each switch, as well as the available time for charging t_{av} must be calculated. These two values are determined and shown in table 1 where

$$C_P = \frac{C_{offset} C_G}{C_{offset} + C_G} \quad (10)$$

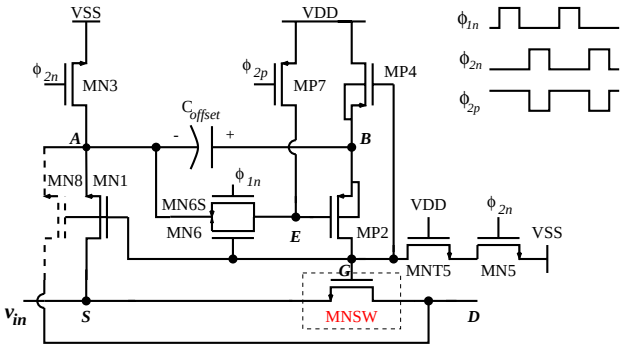

Figure 4. Bootstrapped switch [5].

Switch	Load Capacitance	t_{av}
MNSW	C_S	t_{avsw}
MN1/MN8	$C_P + C_{offsetbp}$	$0.1 \times t_{avsw}/2$
MP2	C_P	$0.1 \times t_{avsw}/2$
MN3	$C_{offset} + C_{offsetbp}$	$t_{avsw}/2$
MP4	C_{offset}	$t_{avsw}/2$
MN5/MNT5	C_G	$0.1 \times t_{avsw}/2$
MN6/MN6S	C_{g2}	$0.1 \times t_{avsw}/2$
MP7	C_{g2}	t_{avsw}

Table 1. Load capacitance and charging available time t_{av} for each switch in the bootstrapping circuit shown in Fig. 4.

and $C_{offsetbp}$ is the bottom plate capacitance of C_{offset}. The available time for switches acting during the on-phase of MNSW, ϕ_1, is set to $0.1 \times t_{avsw}$, where t_{avsw} is the available time for MNSW. This value is then divided by two if two series switches are responsible for the charging/discharging process as explained in section 2. However, for MN3, MP4 and MP7 whose charging time is not critical to the operation of MNSW, the corresponding available time is set to be equal to t_{avsw}. In addition, the settling error ϵ for all switches in the bootstrapping circuit is not critical to circuit operation, so a value of 1% is usually sufficient.

5. EXAMPLE: INTEGRATOR SWITCH SIZING

As a second example, consider switch sizing of the integrator shown in Fig. 1, with $V_{aref} = V_{SS}$ (in this case, an additional charge cancellation SC circuit is needed at node B, refer to [5]). The integrator has a supply voltage of 1V and a clock frequency of 5MHz in a standard CMOS technology with n/p-transistor threshold voltages of 580/600 mV. First, consider S1 and S3 sizing (sampling switches) using the procedure described in sections 3 and 4. Input parameters are summarized in table 2. The input signal is a rail-to-rail one so that the worst-case drain-source voltage of S1 at the switching moment is 1V. The bootstrapping circuit of S1 holds its V_{GS} at 1V. Due to the use of non-overlapping, delayed clock phases, the ϕ_1 duty cycle is only 0.35, which is divided between S1 and S3 as described by equation (4),

Input Parameters	S1	S3
V_{DSinit}	1.0V	0.1V
V_{GS}	1.0V	1.0V
V_{BS}	-1.0V	0.0V
C_S	1.0pF	1.0pF
t_s	200ns	200ns
duty	0.2	0.15
ϵ	1.0E-3	1.0E-3

Table 2. Input parameters for S1 and S3 sizing (Fig. 1).

Switch	W/L (μm)
MNSW	5.4/0.35
MN1/MN8	1.2/0.35
MP2	2.0/0.35
MN3	0.75/0.35
MP4	2.1/0.35
MN5/MNT5	0.5/0.35
MN6/MN6S	0.5/0.35
MP7	0.5/0.35

Table 3. Bootstrap switch S1 transistor sizes.

where $t_{av} = duty \times t_s$.

Obtained transistor sizes for S1 are summarized in table 3 taking minimum transistor lengths, while that of S2 was found to be 1.4/0.35. Fig. 5 shows obtained simulation results. It also shows terminal voltages of S1, which starts conducting in saturation such that the voltage around C_s is linear, then it becomes exponential as S1 enters the ohmic region. The last graph shows the settling error ϵ.

Switches in a 1-V $\Delta\Sigma$ modulator implementation [5] have been all sized separately in a similar process. This optimizes switch sizes for low-voltage operation which are large compared to normal SC circuits due to the small switch overdrive. Consequently, this allows to minimize as much as possible clock feedthrough due to large switch gate capacitances. In order to avoid any performance degradation due to switch settling, all switches are required to settle to the accuracy of the modulator.

6. CONCLUSIONS

While switch sizing is an important issue when designing standard switched-capacitor circuits, this becomes more critical under very low-voltage operation due to the limited switch overdrive voltage. In this paper, series switch sizing was discussed and a simple procedure was proposed and demonstrated through two design examples.

The presented procedure renders the problem of switch sizing optimization a simple task that is easily repeated for each separate switch in a given circuit. This enhances the overall circuit settling and linearity performance.

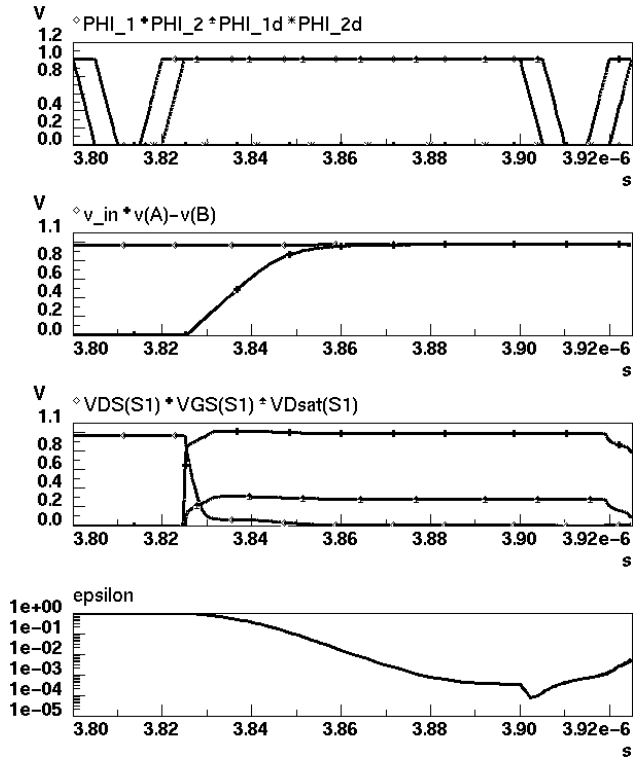

Figure 5. Simulation results of Fig. 1 during ϕ_1.

7. REFERENCES

[1] J. Crols and M. S. J. Steyaert, "Switched-opamp: An approach to realize full CMOS switched-capacitor circuits at very low power supply voltages," *IEEE J. of Solid-State Circuits*, vol. 29, pp. 936–942, Aug. 1994.

[2] A. Baschirotto and R. Castello, "A 1V 1.8-MHz CMOS switched-opamp SC filter with rail-to-rail output swing," *IEEE J. of Solid-State Circuits*, vol. 32, pp. 1979–1986, Dec. 1997.

[3] M. Dessouky and A. Kaiser, "Input switch configuration suitable for rail-to-rail operation of switched-opamp circuits," *IEE Electron. Lett.*, vol. 35, pp. 8–10, Jan. 1999.

[4] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14MS/s CMOS pipeline analog-to-digital converter," *IEEE J. of Solid-State Circuits*, vol. 34, pp. 599–606, May 1999.

[5] M. Dessouky and A. Kaiser, "Very Low-voltage $\Delta\Sigma$ Modulator with 88dB Dynamic Range using Local Switch Bootstrapping," *IEEE J. of Solid-State Circuits*, vol. 36, pp. 349–355, Mar. 2001.

[6] V. Peluso, M. S. J. Steyaert, and W. Sansen, "A 1.5V-100μW $\Sigma\Delta$ Modulator with 12-b Dynamic Range Using the Switched-Opamp Technique," *IEEE J. of Solid-State Circuits*, vol. 32, pp. 943–952, July 1997.

[7] Y. Geerts, A. M. Marques, M. S. J. Steyaert, and W. Sansen, "A 3.3-V, 15-bit, Delta-Sigma ADC with a Signal Bandwidth of 1.1 MHz for ADSL Applications," *IEEE J. of Solid-State Circuits*, vol. 34, pp. 927–936, July 1999.