FDP : FAULT DETECTION PROBABILITY FUNCTION FOR ANALOG CIRCUITS

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ABSTRACT

In analog integrated circuits, process variations result in physical parameter variations. Simulated performance values must then be considered with their tolerance intervals. Consequently, contrarily to digital circuits where the outputs are either '0' or '1' such that we can decide without ambiguity whether a fault is detectable or not, for analog circuits fault detectability is still a vague problem since the fault can either be completely detectable, partially detectable or completely undetectable which makes it very difficult to take a decision. In order to solve this decision problem, we have introduced the fault detection probability (FDP) function which allows to formalize the problem of analog fault detection subjected to parameter variations.

1. INTRODUCTION

The growing need of analog and mixed-signal circuits has recently motivated research in analog testing. Even if the area of the analog part in a mixed circuit represents less than 15% of the total area, the test of this analog part contributes significantly to the global manufacturing cost of the mixed circuit. Traditionally, analog circuits are tested by functional tests which are known to be costly and not efficient. In order to improve the quality and reduce the cost of analog circuit testing, recent research addresses the area of structural testing of analog circuits [1] and [2].

Usually, we use a fault-based technique to test analog circuits [3]. But, due to process parameter deviations, measured performances are to be considered with their tolerance intervals. Deviations from nominal values are caused by many factors such as manufacturing processes, model approximations, aging and surrounding environment. Using only the nominal values to compute analog fault coverage and evaluate the effectiveness of such set of stimuli can result in a significant difference from the reality. So, to have an accurate analog fault detection, we need to consider the effect of tolerances on circuit specifications. The most widely used approach to account for parameter variations is the Monte Carlo simulation [4] and [5]. Other approaches include : interval simulations [6] and [7] and constraint logic programming [8]. In these approaches, we first compute performance intervals for good and faulty circuits and then we compare the two intervals to decide if the fault is detectable or not. Until now, there is no concrete method to quantify by a real number how much a given fault can be detected by a given test with a certain risk α of error probability.

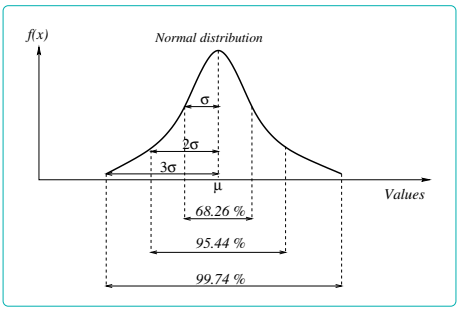

Figure 1: Normal or Gauss distribution.

In this work we propose a new approach for fault detection and fault coverage based on a fault detection probability (FDP) function. We will also use the FDP function to improve the speed of our fault simulation algorithm presented in [9] by using two early-stop rules to reduce the number of simulations needed to compute the FDP function and fault coverage. This paper is organized as follow : Section 2 gives some definitions and theorems of the statistical and the probability theory used in this paper. In section 3, we introduce the fault detection probability *(FDP)* function, and section 4 describes the new analog fault simulation based on *FDP* function. Some results and conclusions are given in sections 5 and 6.

2. STATISTICAL AND PROBABILITY THEORY

2.1. Normal distribution

The normal or Gauss distribution is defined as the distribution with the density:

$$f(x) = \frac{1}{\sqrt{2\pi}\sigma} \exp \frac{-(x-\mu)^2}{2\sigma^2} \tag{1}$$

Here, μ is the mean and σ is the standard deviation. For a risk α ($\alpha = 95\%, 99\%, \cdots$) or confidence level $1-\alpha$, we define the corresponding confidence interval $I_x = [\mu - k_\alpha \sigma, \mu + k_\alpha \sigma]$ as the interval satisfying

$$P(\mu - k_\alpha \sigma < X \leq \mu + k_\alpha \sigma) = 1 - \alpha \tag{2}$$

For a normal distribution, table 1 gives the values of k_α for different risks α (see figure 1). Practically speaking, for a given risk α, this means that all the values will lie between $\mu - k_\alpha \sigma$ and $\mu + k_\alpha \sigma$.

risk α	confidence level $1-\alpha$	k_α
0.10	90%	1.645
0.05	95%	1.960
0.01	99%	2.576

Table 1: k_σ for different risks α.

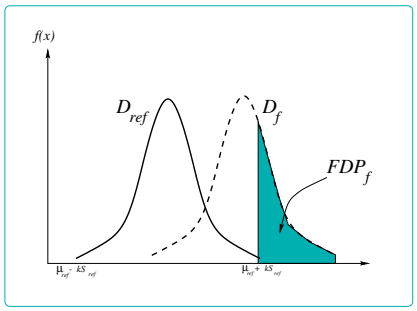

Figure 2: Definition of the fault detection probability (FDP).

2.2. Confidence intervals for μ

As an approximation of the mean μ and standard deviation σ, we may take the mean $\bar{x}$ and standard deviation S of a corresponding sample:

$$\bar{x} = \frac{\sum_{i=1}^{n} x_i}{n} \quad and \quad s = \sqrt{\frac{(\sum_{i=1}^{n} (x_i - \bar{x})^2}{n-1}} \tag{3}$$

where n is the size of the sample. Using the knowledge of the t-distribution of *Student*, the confidence interval for μ of the normal distribution with unknown σ is

$$I_\mu = [\bar{x} - t_{\alpha[n-1]} \frac{s}{\sqrt{n}}, \bar{x} + t_{\alpha[n-1]} \frac{s}{\sqrt{n}}] \tag{4}$$

where $t_{\alpha[n-1]}$ is the *Student* parameter of the t-distribution with risk α and $(n-1)$ degrees of freedom. Table 2 gives some values of $t_{\alpha[n-1]}$ for different values of α and n.

risk α	$t_{\alpha[n-1]}$ of *Student*			
	$(n=5)$	$(n=10)$	$(n=20)$	$(n=30)$
0.10	2.132	1.833	1.729	1.699
0.05	2.776	2.262	2.093	2.045
0.01	4.604	3.250	2.861	2.756

Table 2: $t_{\alpha[n-1]}$ for different values of α and n.

3. FAULT DETECTION PROBABILITY (FDP) FUNCTION

3.1. Definition

The main idea behind the FDP function is to quantify by a number $\in [0,1]$ how much a fault can be detected by a given test. Let's consider that D_{ref} and D_f are the distributions of the output values of the good circuit (reference) and the faulty circuit respectively, and I_{ref} and I_f are their correspondent confidence intervals. The FDP function must satisfy the follow three conditions (see figure 3) :

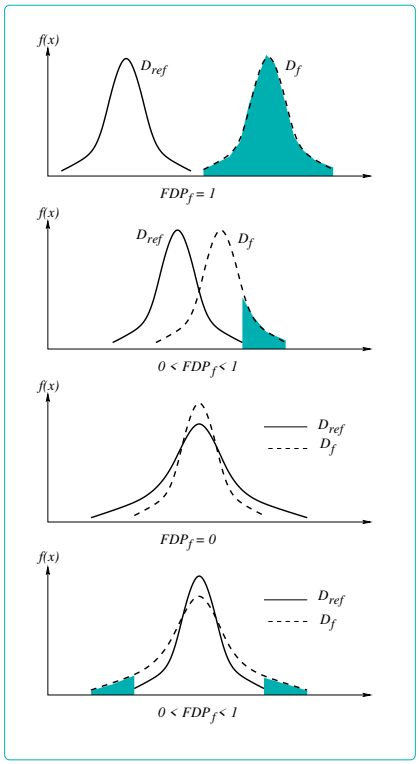

Figure 3: Different FDP values.

1. If $I_f \subset I_{ref}$ then the fault is completely undetectable and the FDP must be equal to 0.
2. If $I_f \cap I_{ref} = 0$ the fault is completely detectable and the FDP must be equal to 1.
3. Else the fault is partially detectable (or partially undetectable) and $0 <$ FDP < 1.

The FDP function is defined as follows:

$$FDP_f = 1 - \int_{I_{ref}} D_f(x)\, dx \tag{5}$$

with $I_f = [\mu_{ref} - k_\alpha \sigma_{ref}, \mu_{ref} + k_\alpha \sigma_{ref}]$. Since $\int_{I_{ref}} D_f(x)\, dx$ represents the probability that a faulty value V_f be inside the reference distribution D_{ref}, FDP_f represents the probability that a faulty value be outside the reference distribution D_{ref}, which is equivalent to the probability that a fault f will be detected (see figure 2). We can easily show that FDP_f verifies the above three conditions. If we assume that a faulty distribution D_f follows a normal distribution with a mean value $\bar{x}_f$ and standard deviation s_f, then the FDP function becomes :

$$FDP = 1 - \int_{I_{ref}} \frac{1}{\sqrt{2\pi} s_f} \exp\left(-\frac{(x-\bar{x}_f)^2}{2s_f^2}\right) dx \tag{6}$$

3.2. Computation of FDP

The FDP definition given by (5) has only one inconvenience, namely, the need to compute a large number of simulations for each faulty circuit to get the distribution D_f. In order to reduce the number of simulations, we propose two early-stop rules.

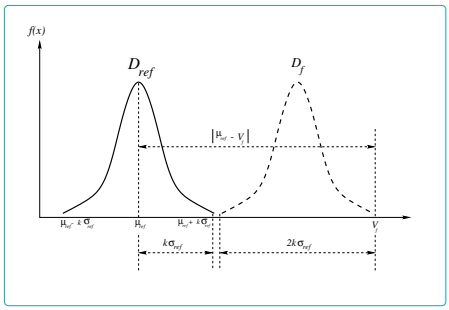

Figure 4: Computation of FDP : case $|\mu_{ref} - V_f| \geq 3k_\alpha\sigma_{ref}$.

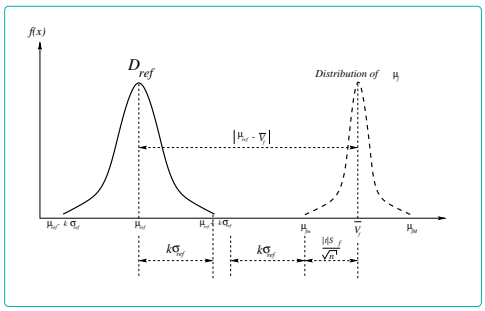

Figure 5: Comp. of FDP : case $|\mu_{ref} - \overline{v}_f| \geq 2k_\alpha\sigma_{ref} + |t|\frac{S_f}{\sqrt{n}}$.

3.2.1. *First rule*

Let V_f represents the current simulated value of the faulty circuit. According to (2) we know that $V_f \in I_f$ ($I_f = [\mu_f - k_\alpha\sigma_f, \mu_f + k_\alpha\sigma_f]$ is the confidence interval of the faulty distribution D_f), and if we assume that $\sigma_f = \sigma_{ref}$, we can show that:

$$|\mu_{ref} - V_f| \geq 3k_\alpha\sigma_{ref} \implies FDP_f = 1 \qquad (7)$$

So, if the simulated value V_f satisfies the condition $|\mu_{ref} - V_f| \geq 3k_\alpha\sigma_{ref}$, then we can stop the simulations and put $FDP_f = 1$ (see figure 4).

3.2.2. *Second rule*

If now, we consider the estimated mean $\overline{v}_f$ of the n first simulations. According to (4), we know that $\mu_f \in I_{\mu f} = [\mu_{fm}, \mu_{fM}]$ with $\mu_{fm} = \overline{v}_f - |t|\frac{S_f}{\sqrt{n}}$, $\mu_{fM} = \overline{v}_f + |t|\frac{S_f}{\sqrt{n}}$ and $t = t_{\alpha[n-1]}$ is the student parameter, so we can show that:

$$|\mu_{ref} - \overline{v}_f| \geq 2k_\alpha\sigma_{ref} + |t|\frac{S_f}{\sqrt{n}} \implies FDP_f = 1 \qquad (8)$$

As for the first rule, if the estimated mean $\overline{v}_f$ satisfies the condition $|\mu_{ref} - \overline{v}_f| \geq 2k_\alpha\sigma_{ref} + |t|\frac{S_f}{\sqrt{n}}$, then we can stop the simulations and put $FDP_f = 1$ (see figure 5).

3.3. Fault coverage using the FDP function

Let's consider a set $T = \{T_1, T_2, \cdots T_n\}$ of n test patterns and a set $F = \{F_1, F_2, \cdots F_m\}$ of m faults. To get an accurate fault coverage FC of the set T, we used the FDP function as follows:

$$FC = \frac{\sum_{j=1}^{m} Max\{FDP_{i,j} | T_i \in T\}}{m} \qquad (9)$$

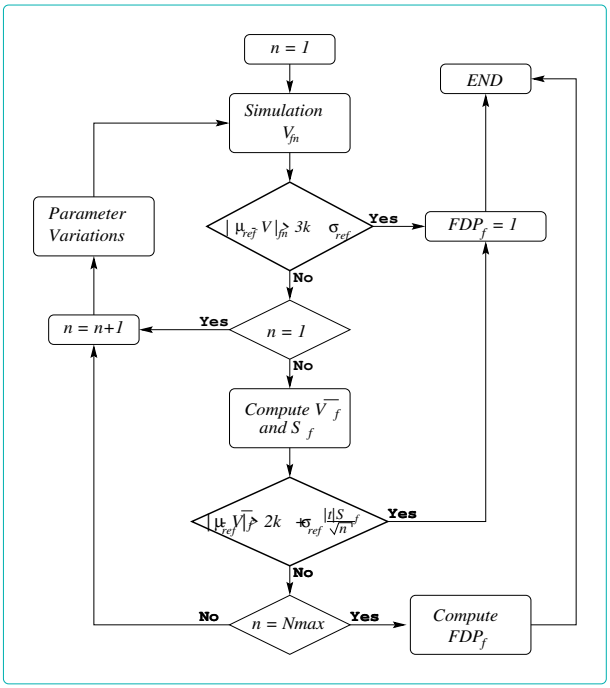

Figure 6: Fault simulation algorithm.

where $FDP_{i,j}$ represents the probability that the test T_i detects the fault F_j and $Max\{FDP_{i,j} | T_i \in T\}$ represents the best probability that can be obtained from all tests of the set T.

4. ANALOG FAULT SIMULATION USING THE FDP FUNCTION

Using the definition given in (6) and the two rules corresponding to the assumptions (7) and (8), we improved our fault simulation algorithm presented in [9]. The new fault simulation algorithm is shown in figure 6.

For each faulty circuit, the algorithm starts the simulations with nominal parameter values. If the simulated value v_f satisfies assumption (7) we have $FDP_f = 1$ and the simulation is stopped, else we proceed to parameter variations and re-evaluate the simulated value v_f. If the new v_f satisfies (7) then $FDP_f = 1$, else we compute the estimated $\bar{v}_f$ and s_f, if $\bar{v}_f$ satisfies assumption (8) then $FDP_f = 1$, else we repeat the above steps until the fault is detected or $n = Nmax$, where $Nmax$ represents the maximum number of simulations needed to compute the FDP value using definition (6).

5. RESULTS

We applied our approach to the current mode integrator shown in figure 7, designed for a $0.6\mu\ CMOS$ process [10]. All design parameters (W and L of the transistors and capacitance values) are assigned 5% of statistical variations.

We considered both catastrophic and parametric faults for transistors and capacitors. For catastrophic faults, we considered

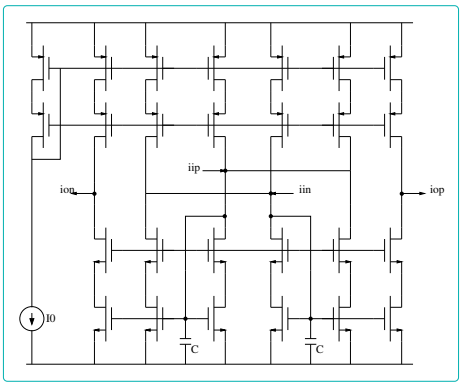

Figure 7: Current mode integrator.

type of faults	fault coverage		
	classical approach	Monte Carlo approach	our approach
catas.(54)	90.2%	85.5%	85.5%
param.(540)	84.3%	69.6%	70.4%

Table 3: Comparative fault coverage results.

only short faults while for parametric faults we considered 10 deviations per parameter from 10% to 100% by a step of 10%. For all transistors, we considered the occurrence of the two probable short faults : Gate Source Short (GSS) and Gate Drain Short (GDS) defined in [11]. So for the 26 transistors and 2 capacitors of the circuit, we have 54 catastrophic faults and 540 parametric faults. The current gain $(\frac{i_{op}-i_{on}}{i_{ip}-i_{in}})$ has been simulated using *AC* simulations in the frequency range $[0, 3Mhz]$.

Tables 3 and 4 compare obtained results to both the *Monte Carlo* (MC) and the classical fault simulation CS approaches with respect to both fault coverage and CPU time. For MC and our approach we took $Nmax = 10$ and the risk $\alpha = 0.05$. In the CS fault simulation approach, for each fault f, we undergo only one simulation to get the simulated value v_f of the faulty circuit, if v_f is outside the confidence interval I_{ref} of the reference circuit then the fault f is detectable $FDP_f = 1$, otherwise f is undetectable $FDP_f = 0$. It can be seen from the table 3 that our method is as accurate as the MC method, while the CS method is the least accurate one. For parametric faults, the small difference in the fault coverage between the MC approach $(FC = 69.6\%)$ and our approach $(FC = 70.4\%)$ is due to the fact that, for some parametric faults, the standard deviation σ_f of the faulty circuit is not equal to the standard deviation σ_{ref} of the reference circuit. Concerning the speed-up, we can see from table 4 that our approach is faster than the MC method, but the speed-up is more significant for catastrophic faults (3.71 times faster) than for parametric faults (1.85 times faster). This is due to the fact that parametric faults are more difficult to detect than catastrophic ones.

6. CONCLUSION

We propose a new approach for accurate fault detection of analog ICs. In order to include the effect of parameter deviations, the fault detection and fault coverage problems were formulated using a fault detection probability FDP function. We have demonstrated the advantages of our approach through a $CMOS$ current-mode integrator by computing the fault coverage of both catastrophic and parametric faults. An average of 2.5 CPU time speed-up with respect to the *Monte Carlo* approach is obtained. This method is currently being studied for the implementation of a fully automated fault simulation for complex analog circuits.

type of faults	CPU time (s)		
	classical approach	Monte Carlo approach	our approach
catas. (54)	63	632	170
param. (540)	632	6325	3426

Table 4: Comparative CPU time results.

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