A MOS Transistor Model for Peak Voltage Calculation of Crosstalk Noise

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ABSTRACT

To certify the correctness of a design, in deep submicron technologies, the verification process has to cover some new issues. The noise introduced on signals through the crosstalk coupling is one of these emerging problems. In this paper, we expose a first model to evaluate the peak value of the noise injected on a signal during the transition of its neighboring signals. Then, analysing the error introduced by each step of simplification in this model, we propose a new MOS transistor model.

1. INTRODUCTION

Multi-million transistor circuits are made using the latest processes. The features of these technologies include an increased number of metal levels, thinner metal width, increased wire height versus width ratio and smaller wire spacing. These new features introduce new causes of failure. This is the reason why designers spend up to 80 % of a design on the verification step. Therefore, some new verification tools are needed to check the robustness of VLSI circuits against these causes within a reasonable computation time.

It is well known that some up to lately neglected physical effects in submicron technologies, such as crosstalk, can significantly affect the behaviour of the circuit (timing and/or functional failure). Nowadays, the design methodologies [1] and tools, such as router, have to take into account the crosstalk phenomenon [2][3][4][5][6][7].

In this paper, we propose a simple and still accurate model to evaluate the impact of the crosstalk noise for each signal of the circuit. The next section describes the crosstalk phenomenon. Section 3 details a crosstalk noise model and the different steps of simplifications used to obtain an analytical expression of the noise's peak value. In the section 4 an improvement of this model is proposed. Some results are shown in section 5. We compare the noise evaluated from the proposed model against a SPICE simulation and finally concluding remarks and future works are depicted in the last section.

2. THE CROSSTALK NOISE

The crosstalk phenomenon is due to the existence of a capacitance between two neighboring wires. Whenever a wire makes a transition, a noise is produced through this coupling capacitance on the other wire of the couple. Let's consider two signals A and V driven by two inverters (Fig. 1). When the signal A makes a transition, a noise is injected on the signal V. If V is in a steady state, the noise has the form of a spike and is absorbed by the V's driver after some delay. On the contrary, if V is making its transition in the same time, the crosstalk noise leads to a shorter or a longer transition delay. The signal A is called the *aggressor* and V the *victim*.

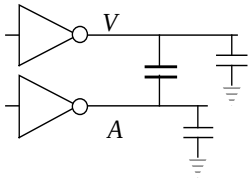

Fig. 1: Two signals in crosstalk coupling

In a real circuit, a given signal may be coupled with several thousand signals. However, at a given time, all the aggressors are not making a transition. The aggressors which are in a steady state and do not contribute to the noise produced on the victim are called *silent aggressors*. In turn, each aggressor may have many other couplings. When a given signal is considered as a victim, all the other victims of its aggressors are called *secondary victims*.

In submicron processes, many factors contribute to the apparition of the crosstalk noise: the shape of wires, the reduction of the distance between wires, the greater number of metal layers, etc. These factors tend either to reduce the capacitance to the ground or, to increase the coupling capacitance. Another parameter that determines the importance of the noise is the impedance of the aggressor and the victim's drivers.

3. PREVIOUS WORK

In a previous paper [10] we have proposed a model that ignores the RC interconnects but gives a satisfying estimation of the peak using a simple approach. In addition, this model takes into consideration some second order effects such as the existence of silent aggressors or secondary victims. Here we give an overview of this model. Let's consider the case of figure 2.

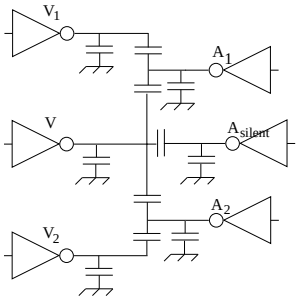

Fig. 2: Complex circuit

Like many other models, in the proposed approach a first approximation consists in replacing signal's drivers by a simple resistance. However, the victim and the aggressors are not approximated in the same manner. The transistors of the victim's driver are in their linear region whereas the aggressors make the most part of their transition in the saturated mode. Thus, two different equivalent resistors are calculated for each driver: a first resistance is used when the signal is considered as a victim and a second one when the signal is taken as an aggressor.

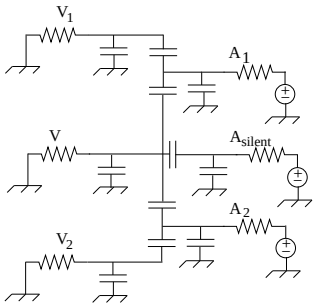

Fig. 3: Signal's divers replaced by resistance

In the next step, for each victim, the silent aggressors are replaced by an equivalent capacitance. Then, for each of the remaining active aggressors, their secondary victims are replaced by an equivalent capacitance.

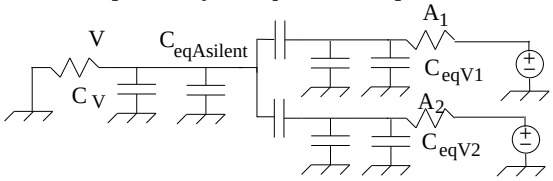

Fig. 4: Silent aggressors and other victims replaced by capacitance

Finally, active aggressors are replaced by an equivalent current source where the current decreases in an exponential form. Each current source is calculated such as the peak produced on the victim occur at the same time and have the same value as the peak induced by the corresponding aggressor.

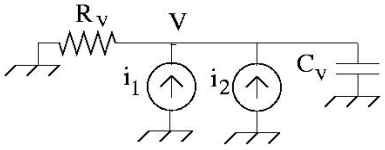

Fig. 5: Active aggressors replaced by current sources

Then, the effect of the different current sources are added and the victim's waveform is expressed:

$$v(t) = R_v \sum_{k=1}^{2} I_{0_k} \frac{\tau_{i_k}}{\tau_v - \tau_{i_k}} (e^{-t/\tau_v} - e^{-t/\tau_{i_k}})$$

where $\tau_v = R_v C_v$

I_{0k} is the current delivered by the current source k at the time 0, τ_{ik} is the time constant of the current source k.

The experience has shown that the absolute error of this method compared to an electrical simulation remains less than 20 %. These errors come mainly from three sources.

Approximating aggressors by an equivalent resistance is responsible of the major part of the error. Another problem is that replacing aggressors by an equivalent current source neglects the interaction between the aggressors. Even if it looks reasonable, the replacement of the victim's driver by an equivalent resistance can leads to a significant error. Actually, as long as the peak generated on the victim is below the saturation voltage of the victim's driver transistor, the approximation behaves correctly and the error remains reasonably low. However, if the configuration of the noise becomes such that the peak value exceeds the saturation voltage, the estimation diverges from the real value. Moreover, since the current delivered by the resistor is linear whereas the transistor is saturated, the peak is always underestimated. Furthermore, this error occurs for the high peak values where the risk of functional failure is important.

In this article, we propose an improvement of the previous model that tends to reduce the error introduced by the replacement of the signal drivers by a resistor.

4. MODELLING THE VICTIM'S DRIVER

4.1. Transistor model

The proposed approach is based on a specific modelling of the drain current in short channel transistor (MCC). Here we give a brief overview of this model. A detailed description of MCC can be found in [8][9].

In MCC, a MOS transistor and the current it can drive is characterized by 3 regions and the following expressions:

Blocked mode ($v_{gs}<V_t$) $i_{ds} = 0$

Linear mode ($v_{ds}<V_{sat}$) $i_{ds} = \frac{v_{ds} I_{sat}}{V_{sat}}$

Saturated mode($v_{ds}>V_{sat}$) $i_{ds} = \frac{W}{L} \frac{A(v_{gs} - V_t)^2}{(1 + B(v_{gs} - V_t))}$

Saturation voltage $V_{sat} = K(v_{gs} - V_t)$

In the linear mode, the current is proportional with the v_{ds} voltage. In the saturation region, the drain current is constant and does not depend on v_{ds}.

In this model A and B are two constant parameters that depend on the process and characterize the drain current. K is a constant representing the saturation factor. These parameters have to be set through a set of electrical simulations to make the MCC model be fitted to a given process.

This simple model has been used to develop several verification tools inside the Alliance CAD System including a static timing analysis and a first version of crosstalk noise estimator. However, the discontinuity between the linear and the saturated modes makes the evaluation of the peak value difficult when the peak exceeds the saturation voltage.

Thus, we propose a unified model of the drain current as an exponential function of v_{ds} :

$$i_{DS} = I_{sat}(1 - e^{\frac{-v_{DS}}{\alpha}})$$

where α is a parameter which depends on the process. Figure 6 shows the proposed current model compared to a Spice simulation for a 0.25µm technology. The different parameters of the model have been set to match the drain current for the high values of v_{gs}.

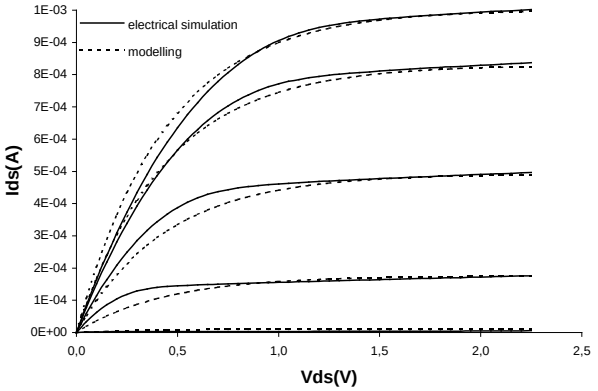

Fig. 6: Drain current vs. drain voltage given by electrical simulation and the proposed model

4.2. Discharge of a capacitance

Many current forms may be used to match the current driven by a transistor. Nevertheless, the model must respect some constraints. Applying the expression of the drain current to the case of the victim and the active aggressors in crosstalk coupling leads to some first order differential equations' system. The particular form of the drain current must be such that it eases the analytical resolution of this system. Resolving this system of differential equations needs several steps and cannot be exposed here due to the shortness of space. Here we details the discharge of a capacitance using the proposed model and how the analytical expression of the drain voltage can be obtained (fig. 7). The same technique may be used to resolve the system of differential equations that characterises the crosstalk phenomenon.

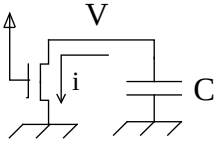

Fig. 7: Discharge of a capacitance in a transistor

The following first order non linear equation characterises the circuit:

$$I_{sat}(1 - e^{\frac{-v_{DS}}{\alpha}}) + C.v'_{DS} = 0$$

The resolution is obtained by making a variable replacement:

$$v_{DS}(t) = \alpha.\log(f)$$

$$\frac{1}{f}(I_{sat}(f - 1) + C.f') = 0$$

The expression of v_{ds} can be stated given the initial value $v_{ds}(0) = V_0$

$$v_{DS}(t) = \alpha.\log(1 + (e^{\frac{V_0}{\alpha}} - 1).e^{\frac{-I_{sat}}{C.\alpha}t})$$

Figure 8 illustrates a comparison between our expression and a Spice simulation for the same 0.25µm process.

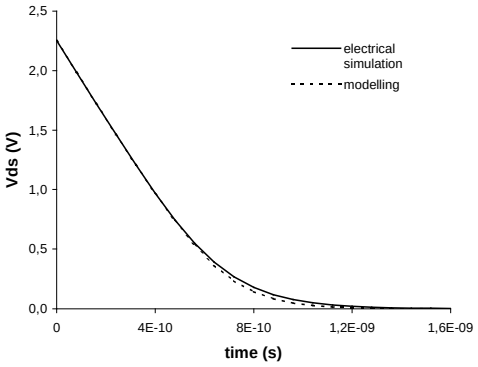

Fig. 8: Drain current versus drain voltage for electrical simulation and model

5. RESULTS

The implementation of this enhanced model in a prototype Crosstalk Noise Evaluation tool is currently under development.

However, a simple bench circuit can be used to check the relevance of the proposed transistor current model. The bench circuit is composed of a victim signal V surrounded by 3 active and 3 silent aggressors. Each aggressor is coupled to the signal V and to 3 other secondary victims via coupling capacitance.

Different set of coupling and ground capacitance have been experimented to produce different types of peak on the victim.

Tables 1 to 3 show the peak value and the corresponding absolute error obtained on the signal V. The comparison between the previous model and the enhanced model is performed by replacing the active elements of the circuit by an equivalent resistor or by the proposed transistor model. The two first lines concern the replacement of the victim's and the active aggressors' drivers. The third shows the combined effect of these two replacements. The absolute error is calculated by making the difference of the estimated peak and the peak obtained from a Spice simulation divided by Vdd.

The results are given for a 0.25µm process, where the supply voltage is 2,25V.

In the first situation, the peak value given by a Spice simulation is 0,38 V and is largely blow the saturation voltage.

Modelling	Previous model (V)	Error (%)	Enhanced model (V)	Error (%)
Victime	0,397	-0,6	0,357	1,2
Agressors	0,341	1,9	0,361	1,0
Vict + Ag	0,357	1,2	0,331	2,3

Table 1 : Previous vs. Enhanced model for a peak of 0,38V

As it can be observed the proposed model represents a better approximation for the aggressors that make their transitions mainly in their saturation region. However, the overall error obtained from the enhanced model is higher but remains reasonable. This error is mainly due to the fact that, the proposed current model is not accurate for low values of v_{DS}

For the second example, the peak value is 0,61 V and is close to the saturation voltage. In this case, the error for the two models are comparable.

Modelling	Previous model (V)	Error (%)	Enhanced model (V)	Error (%)
Victime	0,584	1,1	0,594	0,6
Agressors	0,495	5,0	0,555	2,4
Vict + Ag	0,489	5,3	0,533	3,3

Table 2 : Previous vs. Enhanced model for a peak of 0,61V

In the last case, a high peak (1,135 V) is produced on the victim.

Modelling	Previous model (V)	Error (%)	Enhanced model (V)	Error (%)
Victime	1,025	4,9	1,136	0,0
Agressors	0,960	7,8	1,136	0,0
Vict + Ag	0,888	11,0	1,135	0,0

Table 3 : Previous vs. Enhanced model for a peak of 1,135V

As expected, these first results show that the proposed improvement does not affect the error for the low values of the peak. Nevertheless, when the noise is such that the victim's driver enters in its saturation region, the error induced by the resistive model is largely reduced.

6. CONCLUSION AND FUTURE WORKS

The preliminary results obtained from the application of the proposed transistor model to the victim's driver seem to confirm the expected gain in the peak voltage calculation and push to experiment the application of the proposed model to a life size VLSI circuit.

The proposed transistor drain current leads to a more complex peak expression and requires several additional computation steps. However, this increase of the complexity is compensate by a significant reduction of the error for the high peaks. Thus, to limit the overhead of computation time introduced by the enhanced model, a mixed approach may represent a suitable trade-off. In this configuration, the noise verification tools operates in two steps. In a first step, a rough estimation of the peak is performed using the resistive model. Then, in the second step, the peak evaluation is improved by using the enhanced model for those signals that show a high peak value.

Besides, the crosstalk model has to be extended to take into account the interaction between aggressors and the RC of the interconnects.

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