An analytical MOS Transistor Model Dedicated to Crosstalk Noise Evaluation

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Abstract[1]: In deep submicron technologies, the noise introduced on signals through the crosstalk coupling is an emerging problem. This paper presents a new analytical MOS transistor model valid in all regions of operation and dedicated to crosstalk noise evaluation and review some useful methods and related work on crosstalk analysis. The same MOS transistor model can be used for the victim and aggressors drivers. The proposed model is validated by comparison to SPICE simulations.

Key-Words: MOS Transistor, Model, SPICE Simulation, Crosstalk Noise

1. Introduction

Multi-million transistor circuits are made using the latest processes. The features of these technologies include an increased number of metal levels, thinner metal width, increased wire height versus width ratio and smaller wire spacing. These new features introduce new causes of failure. This is the reason why designers spend up to 80 % of a design on the verification step. Therefore, new tools able to perform verifications in a reasonable delay on complex circuits are needed to be developed.

It is well known that some up to lately neglected physical effects in submicron technologies, such as crosstalk, can significantly affect the behaviour of the circuit (timing and/or functional failure). Nowadays, the design methodologies [1] and tools, such as router, have to take into account the crosstalk phenomenon [2][3][4][5][6][7]. Then, to certify the correctness of a design made by those tools, some new back-end verification tools have to be developed.

In this paper, we propose a simple and still accurate model to evaluate the impact of the crosstalk noise for each signal of the circuit. The next section describes the crosstalk phenomenon. Section 3 reviews some useful methods and related work on crosstalk analysis. Section 4 details the crosstalk noise model and his improvement. Some results are shown in section 5. We compare the noise evaluated from the proposed model against a SPICE simulation and finally concluding remarks and future works are depicted in the last section.

The crosstalk phenomenon is due to the existence of a capacitance between two neighboring wires. Whenever a wire makes a transition, a noise is produced through this coupling capacitance on the other wire of the couple. Let's consider two signals A and V driven by two inverters (Fig. 1). When the signal A makes a transition, a noise is injected on the signal V. If V is in a steady state, the noise has the form of a spike and is absorbed by the V's driver after some delay. On the contrary, if V is making its transition in the same time, the crosstalk noise leads to a shorter or a longer transition delay. The signal A is called the *aggressor* and V the *victim*.

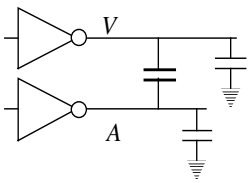

Fig. 1: Two signals in crosstalk coupling

In a real circuit, a given signal may be coupled with several thousand signals. However, at a given time, all the aggressors are not making a transition. The aggressors which are in a steady state and do not contribute to the noise produced on the victim are called *silent aggressors*. In turn, each aggressor may have many other couplings. When a given signal is considered as a victim, all the other victims of its aggressors are called *secondary victims*.

In submicron processes, many factors contribute to the apparition of the crosstalk noise: the shape of wires, the reduction of the distance between wires, the greater number of metal layers, etc. These factors tend either to reduce the capacitance to the ground or, to increase the coupling capacitance. Another parameter that determines the importance of the noise is the impedance of the aggressor and the victim's drivers.

[1] This study is part of a Ph.D. thesis currently undergoing at University of Paris 6 and funded by ST-Microelectronics.

2. Previous works

Many models have been proposed to estimate the peak value of the noise produced on a victim. Some of these models take into account the resistance-capacitance of the interconnect, others focus on studying the noise produced by the simultaneous transition of several aggressors:

- The PI Model [10] take into account coupled RC interconnects and gives a peak noise estimation on victim line caused by one aggressor. The peak noise value reported for multiple aggressors is the superposition of noise contributions [11]. Maximum error in the peak noise computation for an example three-aggressor case is about 30%.
- The model using the aggressor slope time [12] replaces the aggressors by the time when the aggressor net begins to fall and ends. It takes into account of multiple aggressor cases but not of RC interconnects. The error between an electrical simulation and this method is about 30 %, in the case of an aggressor, and about 7% in the case of 3 aggressors.
- [13] is a case study of a method developed in [14], which works with a RC tree and multiple aggressors. The over estimation of the peak noise is around 15 % in the case of a circuit powered by a 1.8v and with a fast rise time of 100ps. The accuracy of this model degrades with reduction in rise time of the aggressors.

In a previous paper [9] we have proposed a model that ignores the RC interconnects but gives a satisfying estimation of the peak using a simple approach. In addition, this model takes into consideration some second order effects such as the existence of silent aggressors or secondary victims. Here we give an overview of this model:

Let's consider the case of figure 2.

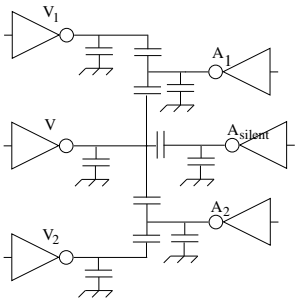

Fig. 2: Complex circuit

Like many other models, in the proposed approach a first approximation consists in replacing signal's drivers by a simple resistance (Fig. 3). However, the victim and the aggressors are not approximated in the same manner. The transistors of the victim's driver are in their linear region whereas the aggressors make the most part of their transition in the saturated mode. Thus, two different equivalent resistors are calculated for each driver: a first resistance is used when the signal is considered as a victim and a second one when the signal is taken as an aggressor.

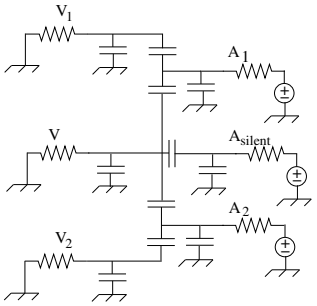

Fig. 3: Signal's divers replaced by resistance

In the next step, for each victim, the silent aggressors are replaced by an equivalent capacitance. Then, for each of the remaining active aggressors, their secondary victims are replaced by an equivalent capacitance.

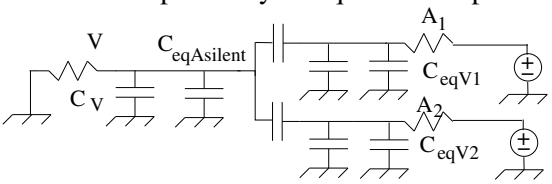

Fig. 4: Silent aggressors and other victims replaced by capacitance

Finally, active aggressors are replaced by an equivalent current source where the current decreases in an exponential form. Each current source is calculated such as the peak produced on the victim occur at the same time and have the same value as the peak induced by the corresponding aggressor.

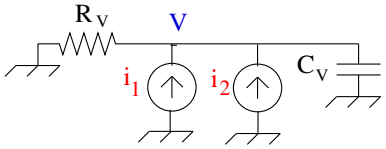

Fig. 5: Active aggressors replaced by current sources

Then, the effect of the different current sources are added and the victim's waveform is expressed:

$$v(t) = R_v \sum_{k=1}^{2} I_{0_k} \frac{\tau_{i_k}}{\tau_v - \tau_{i_k}} (e^{-t/\tau_v} - e^{-t/\tau_{i_k}})$$

The experience has shown that the relative error of this method compared to an electrical simulation remains less than 20 %. These errors come mainly from three sources.

Approximating aggressors by an equivalent resistance is responsible of the major part of the error. Another problem is that replacing aggressors by an equivalent current source neglects the interaction between the

aggressors. Even if it looks reasonable, the replacement of the victim's driver by an equivalent resistance can leads to a significant error. Actually, as long as the peak generated on the victim is below the saturation voltage of the victim's driver transistor, the approximation behaves correctly and the error remains reasonably low. However, if the configuration of the noise becomes such that the peak value exceeds the saturation voltage, the estimation diverges from the real value. Moreover, since the current delivered by the resistor is linear whereas the transistor is saturated, the peak is always underestimated. Furthermore, this error occurs for the high peak values where the risk of functional failure is important.

In this article, we propose an improvement of the previous model that tends to reduce the error introduced by this last approximation (Fig. 6).

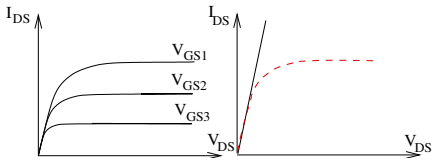

Fig. 6: Drain current/voltage for transistor and the resistance model

3. Modelling the victim's driver

3.1. Transistor model

The proposed approach is based on a specific modelling of the drain current in short channel transistor (MCC). Here we give a brief overview of this model. A detailed description of MCC can be found in [8].

In MCC, a MOS transistor and the current it can drive is characterized by 3 regions and the following expressions:

Blocked mode ($v_{gs}<V_t$) $i_{ds} = 0$

Linear mode ($v_{ds}<V_{sat}$) $i_{ds} = \frac{v_{ds} I_{sat}}{V_{sat}}$

Saturated mode($v_{ds}>V_{sat}$) $i_{ds} = \frac{W}{L} \frac{A(v_{gs} - V_t)^2}{(1 + B(v_{gs} - V_t))}$

Saturation voltage $V_{sat} = K(V_{gs} - V_t)$

In the linear mode, the current is proportional with the v_{ds} voltage. In the saturation region, the drain current is constant and does not depend on v_{ds}.

In this model A and B are two constant parameters that depend on the process and characterize the drain current. K is a constant representing the saturation factor. These parameters have to be set through a set of electrical simulations to make the MCC model be fitted to a given process.

This simple model has been used to develop several verification tools inside the Alliance CAD System including a static timing analysis and a first version of crosstalk noise estimator. However, the discontinuity between the linear and the saturated modes make the evaluation of the peak value difficult when the peak exceeds the saturation voltage.

Thus, we propose a unified model of the drain current as a decreasing exponential function of v_{ds} :

$$i_{DS} = I_{sat}(1 - e^{\frac{-v_{DS}}{\alpha}})$$

where α is a parameter which depends on the process. Figure 7 shows the proposed current model compared to a Spice simulation for a 0.25µm technology. The different parameters of the model have been set to match the drain current for the high values of v_{gs}.

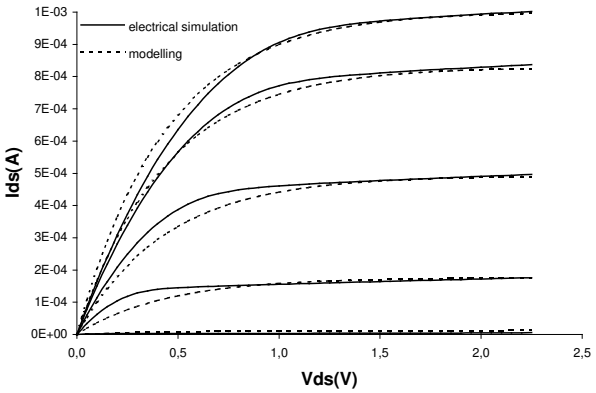

Fig. 7: Drain current vs. drain voltage given by electrical simulation and the proposed model

3.2. Discharge of a capacitance

Many current forms may be used to match the current driven by a transistor. Nevertheless, the model must respect some constraints. The particular form of the drain current has been chosen in such a way it allows to solve the differential equation describing a capacitance discharge thru a transistor. Let consider the case of Figure 8 where a capacitance is discharged through a transistor and where the grid has a constant voltage.

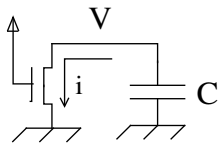

Fig. 8: Discharge of a capacitance in a transistor

The following first order non linear equation characterizes the circuit:

$$I_{sat}(1 - e^{\frac{-v_{DS}}{\alpha}}) + C.v'_{DS} = 0$$

The resolution is obtained by making a variable replacement:

$$v_{DS}(t) = \alpha.\log(f)$$

$$\frac{1}{f}(I_{sat}(f-1) + C.f') = 0$$

The expression of Vds can be stated given the initial value $v_{ds}(0) = V_0$

$$v_{DS}(t) = \alpha.\log(1 + (e^{\frac{V_0}{\alpha}} - 1).e^{\frac{-I_{sat}}{C.\alpha}t})$$

Figure 9 illustrates a comparison between our expression and a Spice simulation for the same 0.25µm process.

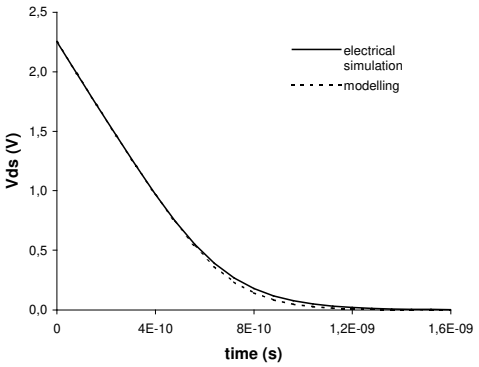

Fig. 9: Drain current versus drain voltage for electrical simulation and model

3.3. Current sources

Let now consider the case of the noise induced on a victim by a set of current sources. Each current source represents a switching aggressor and has the following form:

$$i_i = I_i.e^{-t/\tau_i}$$

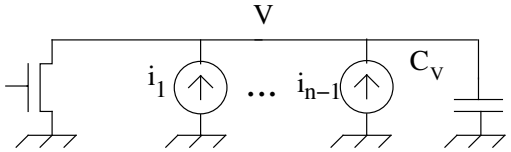

Fig. 10: Multiple current sources

The circuit is described by the equation

$$I_{sat}(1 - e^{\frac{-v_{DS}}{\alpha}}) + Cv'_{DS} - g(t) = 0$$

where $g(t) = \sum_{i=1}^{n-1} I_i.e^{-t/\tau_i}$

The same variable replacement technique can be used to simplify the equation:

$$v_{DS} = \alpha.\log(f)$$

$$\frac{1}{f}(I_{sat}f + C\alpha f' - fg - I_{sat}) = 0$$

Unfortunately the resulting equation is not linear and cannot be solved in a simple way. Therefore, several steps are needed to get into a resolution. Let's consider the following equation where I_{sat} has been suppressed:

$$I_{sat}f_0 + C\alpha f_0' - f_0 g = 0$$

A solution of this equation is given by:

$$f_0 = e^{\frac{-1}{C.\alpha}(I_{sat}.t - \int g(t)dt)}$$

Back to the original equation a second variable replacement is proposed:

$$f = f_0 h$$

$$h(I_{sat}f_0 + C\alpha f_0' - gf_0) + C\alpha h' f_0 - I_{sat} = 0$$

$$C\alpha h' f_0 - I_{sat} = 0$$

Then $f(t)$ can be expressed:

$$f(t) = \frac{I_{sat}}{C\alpha} f_0 \int e^{\frac{1}{C\alpha}(I_{sat}t - \int g(t)dt)} dt$$

Even if $g(t)$ can be easily integrated, $f(t)$ cannot be expressed because of the second primitive. Therefore, an approximation is needed to obtain the expression of $f(t)$. Let consider the following expression:

$$p(t) = e^{-\int \frac{1}{C\alpha} g(t)dt}$$

We propose to approximate $p(t)$ by $p_{eq}(t)$ such as:

$$p_{eq}(t) = \sum_{i=0}^{\infty} k_i.e^{-i.\frac{t}{\tau}}$$

The different k_i parameters are defined by forcing $p_{eq}(t)$ to respect the following conditions:

$$\lim_{t \to +\infty} p(t) = \lim_{t \to +\infty} p_{eq}(t)$$

and $$\forall j \in N,\ p(j.\tau) = p_{eq}(j.\tau)$$

Actually, limiting the number of parameters to 4 leads to a satisfying precision. Figure 11 shows the function $p(t)$ and its approximation $p_{eq}(t)$

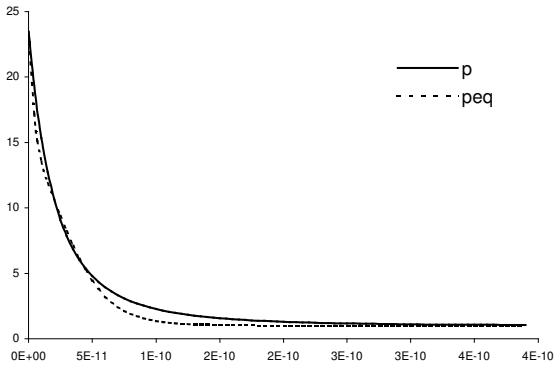

Fig. 11: Approximation of the function p(t) by the function $p_{eq}(t)$

The time constant τ is determined such as the slope of $p(t)$ and $p_{eq}(t)$ be the same at t=0.

$$\frac{dp}{dt}(0) = \frac{dp_{eq}}{dt}(0)$$

Thus,

$$\tau = \frac{C.\alpha}{\sum_{i=1}^{n} I_i}\left(1 - e^{-\frac{1}{C.\alpha}\sum_{i=1}^{n}\tau_i.I_i}\right)$$

Then, replacing *p(t)* by its equivalent gives the analytic expression of *f(t)*

$$f(t) = \frac{I_{sat}}{C\alpha} f_0 \int\left(e^{\frac{I_{sat}t}{C\alpha}} * \sum_{i=0}^{\infty} k_i.e^{-i\frac{t}{\tau}}\right)dt$$

Then, considering the initial condition: $v_{DS}(0)=0$, we obtain

$$v_{DS}(t) = \alpha.\log(I_{sat}\tau\sum_{j=0}^{\infty}\frac{k_j}{I_{sat}\tau - C\alpha j}(e^{-j\frac{t}{\tau}} - e^{\frac{I_{sat}}{C\alpha}t})$$

$$+ e^{\frac{1}{C.\alpha}(\sum_{i=1}^{n-1}\tau_i I_i - I_{sat}.t)}) - \frac{1}{C}\sum_{i=1}^{n-1}\tau_i I_i e^{\frac{-t}{\tau_i}}$$

Then, given the expression of $v_{DS}(t)$ peak value of the noise can be expressed. First, the peak time is calculated from:

$$\frac{dv_{DS}}{dt}(t_{peak}) = 0$$

An approximate solution of this implicit equation can be obtained using an iterative resolution technique (Newton-Raphson). Then, the peak voltage is calculated from:

$$v_{peak} = v_{DS}(t_{peak})$$

Figure 12 gives a comparison between the waveform obtained from an electrical simulation and the analytic expression of $v_{DS}(t)$ when the victim is aggressed by 3 aggressors.

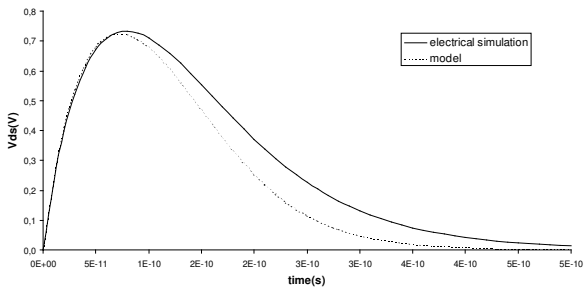

Fig. 12: Peak voltage for electrical simulation and model

4. Results

The implementation of this enhanced model in a prototype Crosstalk Noise Evaluation tool is currently under development.

However, a simple bench circuit can be used to check the relevance of the proposed transistor current model. The bench circuit is composed of a victim signal V surrounded by 3 active and 3 silent aggressors. Each aggressor is coupled to the signal V and to 3 other secondary victims via a coupling capacitance (Fig. 13).

Different set of coupling and ground capacitance have been experimented to produce different types of peak on the victim.

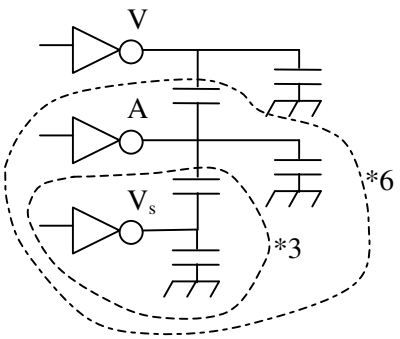

Fig. 13: Bench circuit

Tables 1 to 3 show the peak value and the corresponding relative error obtained on the signal V. The comparison between the previous model and the enhanced model is performed by replacing the active elements of the circuit by an equivalent resistor or by the proposed transistor model. The two first lines concern the replacement of the victim's and the active aggressors' drivers. The third shows the combined effect of these two replacements. Finally, in the two last lines, secondary victims and silent aggressors are replaced by an equivalent capacitance as explained in section 3.

The results are given for a 0.25µm process, where the supply voltage is 2,25V.

In the first situation, the peak value given by a Spice simulation is 0,38 V.

Modelling	Previous model (V)	Error (%)	Enhanced model (V)	Error (%)
Victime	0,397	-3,6	0,357	6,8
Agressors	0,341	11,0	0,361	5,8
Vict + Ag	0,357	6,8	0,331	13,5
Secondary victime	0,357	6,8	0,331	13,5
Silent Agressors	0,362	5,5	0,295	23,1

Table 1 : Previous vs. Enhanced model for a peak of 0,38V

The error obtained from the enhanced model is higher but remains reasonable excepted the approximation of silent aggressors. This error is mainly due to the fact that, the proposed current model is not accurate for low values of v_{DS} . Besides, the equivalent capacitance is calculated using the resistive model.

For the second example, the peak value is 0,61 V and is close to the saturation voltage. In this case, the error for the two models are comparable.

Modelling	Previous model (V)	Error (%)	Enhanced model (V)	Error (%)
Victime	0,584	4,1	0,594	2,3
Agressors	0,495	18,6	0,555	8,8
Vict + Ag	0,489	19,5	0,533	12,3
Secondary victime	0,490	19,5	0,534	12,3
Silent Agressors	0,504	17,1	0,508	16,6

Table 2 : Previous vs. Enhanced model for a peak of 0,61V

In the last case, a high peak (1,135 V) is produced on the victim.

Modelling	Previous model (V)	Error (%)	Enhanced model (V)	Error (%)
Victime	1,025	9,7	1,136	0,0
Agressors	0,960	15,4	1,136	0,0
Vict + Ag	0,888	21,8	1,135	0,0
Secondary victime	0,892	21,4	1,130	0,4
Silent Agressors	0,909	20,0	1,139	-0,3

Table 3 : Previous vs. Enhanced model for a peak of 1,135V

As expected, these first results show that the proposed improvement does not affect the error for the low values of the peak. Nevertheless, when the noise is such that the victim's driver enter in its saturation region, the error induced by the resistive model is largely reduced.

5. Conclusion and future works

An overview of several models currently used in our crosstalk noise analysis and an improvement of our previous model have been presented.

The preliminary results obtained from the application of the proposed transistor model to the victim's driver seem to confirm the expected gain in the peak voltage calculation and push to explore the application of the model in replacement of the aggressors' driver.

The proposed transistor drain current leads to a more complex peak expression and requires several additional computation steps. However, this increase of the complexity is compensate by a significant reduction of the error for the high peaks. Thus, to limit the overhead of computation time introduced by the enhanced model, a mixed approach may represent a suitable trade-off. In this configuration, the noise verification tools operates in two steps. In a first step, a rough estimation of the peak is performed using the resistive model. Then, in the second step, the peak evaluation is improved by using the enhanced model for those signals that show a high peak value.

Besides, the crosstalk model has to be extended to take into account the interaction between aggressors and the RC of the interconnects.

References:

[1] R. Saleh, D. Overhauser, S. Taylor, “Full-Chip of UDSM Designs”, ICCAD, IEEE/ACM, 1998, pp. 453-460.

[2] P. Chen, K. Keutzer, “True Crosstalk Noise Analysis”, DAC, IEEE/ACM, 1999, pp. 111-116.

[3] K.L. Shepard, V. Narayanan, “Noise in Deep Submicron Digital Design”, ICCAD, IEEE/ACM, 1996, pp. 524-531.

[4] B.N. Sheehan, “Predicting Coupled Noise in RC Circuits”, DATE, IEEE, 2000, pp. 517-521.

[5] B. Choi, D.M. H. Walker, “Timing Analysis of Combinational Circuits Including Capacitive Coupling and Statistical Process Variation”, DATE, IEEE, 2000, pp. 59-54.

[6] T. Xue, E.S. Kuh, D. Wang, “Post Global Routing Crosstalk Risk Estimation and reduction”, ICCAD, IEEE/ACM, 1996, pp. 302-309.

[7] H. Zhou, D.F. Wong, “An Optimal Algorithm for River Routing with Crosstalk Contraints”, ICCAD, IEEE/ACM, 1996, pp. 310-315.

[8] A. Hajjar, R. Marbot, A. Greiner, P. Kiani, “TAS: An Accurate Timing Analyser for CMOS VLSI”, EDAC, IEEE, 1991, pp. 261-265.

[9] P. Bazargan-Sabet, F. Ilponse, “Modeling Crosstalk Noise for Deep Submicron Verification Tools”, DATE, 2001.

[10] A.B. Kahng, S. Muddu, D. Vidhani, “Noise and delay uncertainly studies for coupled RC interconnects”, ASIC/SOC, IEEE, 1999, pp. 3.

[11] A.B. Kahng, S. Muddu, N. Pol, D. Vidhani, “Noise Model for Multiple Segmented Coupled RC Interconnects”, ISQED, 2001, pp. 145-150.

[12] P. Chen, K. Keutzer, “Towards True Crosstalk Noise Analysis”, ICCAD, 1999.

[13] P. B. Morton, W. Day, “An Efficient Sequential Quadratic Programming Formulation of Optimal Wire Spacing for Crosstalk Noise Avoidance Routing”, ISPD, 1999.

[14] A. Devgan, “Efficient Coupled Noise Estimation for On-Chip Interconnects”, ICCAD, 1997