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CONCEPTION EN VUE DE LA RÉUTILISATION DE CONVERTISSEURS ANALOGIQUE-NUMÉRIQUE $\Sigma\Delta$ TEMPS-CONTINU MODE-COURANT

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Le jury est composé de :

M. Franco MALOBERTI	Rapporteur
M. Georges GIELEN	Rapporteur
M. Ahmed SOLIMAN	Examinateur
M. Andreas KAISER	Examinateur
M. Carel DIJKMANS	Examinateur
M. Frédéric PAILLARDET	Examinateur
Mme Marie-Minerve LOUËRAT	Examinateur
M. Alain GREINER	Examinateur

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Presented by : **Hassan ABOUSHADY**

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DESIGN FOR REUSE OF CURRENT-MODE CONTINUOUS-TIME $\Sigma\Delta$ ANALOG-TO-DIGITAL CONVERTERS

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Committee in charge :

Franco MALOBERTI	University of Texas at Dallas
Georges GIELEN	Katholieke Universiteit Leuven
Ahmed SOLIMAN	Cairo University
Andreas KAISER	Institut Supérieur d'Électronique du Nord
Carel DIJKMANS	Philips Research Laboratories
Frédéric PAILLARDET	STMicroelectronics R&D
Marie-Minerve LOUËRAT	University of Paris VI
Alain GREINER	University of Paris VI

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Chapter 1

Introduction

Oversampled Sigma-Delta ($\Sigma\Delta$) modulation is widely used in Analog-to-Digital (A/D) conversion of narrow-band signals. Unlike Nyquist rate A/D converters, which need high-precision building blocks, $\Sigma\Delta$ A/D converters show low sensitivity to circuit imperfections. This technique is then well-suited for standard low-cost CMOS technologies dedicated to digital VLSI circuits. Discrete-time (DT) switched-capacitor (SC) technique has been the preferred technique for the implementation of $\Sigma\Delta$ A/D converters.

The recent high demand for wideband, high resolution A/D converters for telecommunication applications requires very high sampling frequencies. The continuously decreasing supply voltage of recent CMOS technologies is causing important limitations to the performances of SC circuits. High switch resistance limits the signal range and limits the sampling frequency. Some circuit techniques, like bootstrapping switch and switched-opamp, have been developed to overcome this problem. These techniques are rather complex and still limit the sampling frequency. Continuous-time (CT) circuits do not suffer from these limitations and are therefore capable of achieving higher performances in recent low-voltage CMOS processes. Input-signal sampling errors, like settling-time errors and charge injection, are other discrete-time (DT) problems that do not exist in CT circuits.

On the other hand, the mixed (CT-DT) nature of CT $\Sigma\Delta$ modulators makes them more difficult to design and simulate. Design techniques for CT $\Sigma\Delta$ modulators are not mature and well-established as it is the case for DT $\Sigma\Delta$ modulators [Candy92] [Norsworthy97].

Furthermore, simulation and design automation tools for DT $\Sigma\Delta$ are widely available:

- Design automation tools for the calculation of the coefficients of stable high order DT $\Sigma\Delta$ modulators are available [Schreier99].
- Circuit synthesis tools for DT SC $\Sigma\Delta$ modulators have also been developed [Medeiro99].
- Tools for rapid simulation of DT $\Sigma\Delta$ taking into account the non-idealities of SC circuits have also been presented [Liberali93][Brigati99].

The lack of a systematic design approaches, in addition to the absence of simulation and design automation tools renders the design of CT $\Sigma\Delta$ modulators difficult and time-consuming. That is the main reason why designers have been reluctant to design CT $\Sigma\Delta$ modulators despite their possible advantages compared to DT techniques.

In this work, we mainly focus on identifying the major design difficulties and finding systematic design approaches suitable for design automation in order render the design of CT $\Sigma\Delta$ easier and faster.

The main contributions of this work can be summarized in the following five points:

- A Discrete-Time to Continuous-Time $\Sigma\Delta$ transformation method using the modified-z-transform technique.
- Low-power low-voltage circuit design of current-mode integrators.
- Multi-technology design automation tool for current-mode continuous-time $\Sigma\Delta$ modulators, from system specifications to transistors sizes.
- Fabrication and measurement of a 5mW, 100kHz bandwidth, current-mode continuous-time $\Sigma\Delta$ modulator with 84dB dynamic range.
- Low-power architecture for comb decimation filters using polyphase decomposition.

Outline

This section gives a brief overview of the contents of the following chapters: After a brief introduction in chapter 1, chapter 2 defines the context of the thesis. Motivations are introduced and the main objectives are stated.

Chapter 3 is a brief state of the art of CT $\Sigma\Delta$ modulators design together with the main strategies used for analog design automation.

In chapter 4 a method, based on the modified z transform technique, to perform equivalence between DT and CT modulators is presented The method is general and systematic. Several lowpass and bandpass design examples are given to illustrate the effectiveness of the transformation method.

Chapter 5 discusses the design of the Low-Power Continuous-Time Current-Mode Integrators for the modulator at the circuit level and analyzes possible sources of harmonic distortion.

Chapter 6 discusses the design of the Digital-to-Analog (DAC) converter of the modulator and analyzes the impact of the clock jitter.

Chapter 7 presents the design methodology used to design a reusable CT $\Sigma\Delta$ converter. First, high level synthesis is performed, based on the DT to CT transformation, to determine system-level parameters from the required specifications. Then, mapping of system requirements to building block specifications is performed. Finally low-level synthesis of each block is done.

Chapter 8 presents the implementation of the $\Sigma\Delta$ modulator. Measurement results from the fabricated modulator are presented and comparison with other recently reported implementations is performed.

In chapter 9 we propose a low-power architecture for the Comb filter of $\Sigma\Delta$ A/D converters.

Finally chapter 10 concludes the thesis with possible direction for future work.

Chapter 2

Problem Definition and Motivation

2.1 Introduction

In order to comprehend the main reasons for our interest in CT $\Sigma\Delta$ modulators, we first present the main advantages and drawbacks of CT $\Sigma\Delta$ modulators compared to their DT counterparts. Then the main issues and difficulties of designing reusable CT $\Sigma\Delta$ modulators are discussed. Finally, we present the main contributions of this thesis towards a more systematic top-down design approach for CT $\Sigma\Delta$ modulators.

2.2 Continuous-Time Versus Discrete-Time $\Sigma\Delta$ Modulators

The general structures of DT and CT $\Sigma\Delta$ modulators are shown in Figures 2.1 and 2.2 respectively. In the following we will discuss the main advantages of CT $\Sigma\Delta$ modulators over their DT counterparts.

- **Low Voltage Operation:**
  The continuously decreasing supply voltage of recent CMOS technologies is causing important limitations to the performances of switched-capacitor circuits. Switch-bootstrapping [Dessouky01] or switched-opamp [Peluso97] circuit techniques are now necessary in order to obtain sufficiently low on-resistances.

- **Sampling Frequency:**
  In switched-capacitor circuits several errors occur while sampling the input signal. These

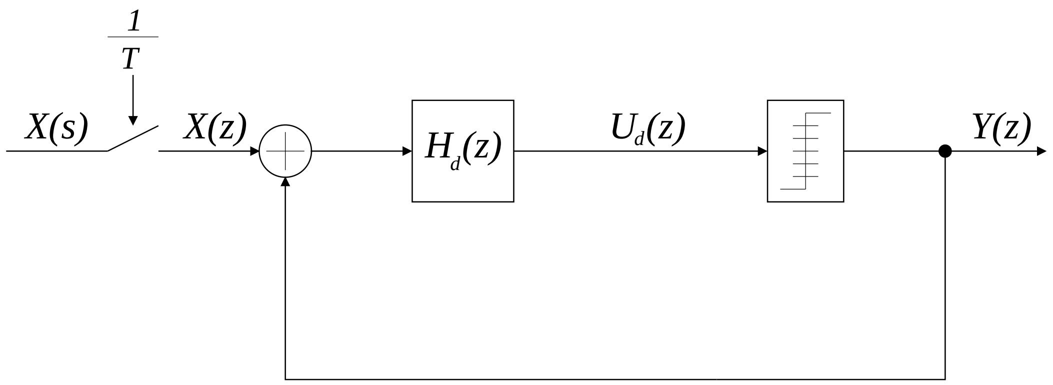

Figure 2.1: *Discrete-time* $\Sigma\Delta$ *modulator*.

errors are due to the switch non-linearity, charge injection, clock feedthrough and finite settling time. Sampling errors in switched-capacitor circuits limit the sampling frequency, f_s, of DT $\Sigma\Delta$ modulators.
In CT modulators sampling occurs inside the $\Sigma\Delta$ loop, therefore sampling errors are shaped out of the frequency band of interest just like quantization noise [Zwan96].

- **Power Consumption:**
  In switched-capacitor circuits the unity gain frequency of operational amplifiers must be at least five times the sample rate [Gregorian86]. High quiescent current is then required to achieve high bandwith. On the other hand, unity gain frequencies of the integrators in the CT $\Sigma\Delta$ are usually lower than the sampling frequency.
  Furthermore, since sampling occurs inside the $\Sigma\Delta$ loop, this strongly reduces:

  – Thermal noise aliasing in the frequency band of interest [Dias92].

  – Aliasing of out of band signals, so that the antialiasing filter may be eliminated [Candy85][Shoaei97].

  It is then expected that for the same specifications, CT $\Sigma\Delta$ modulators will have lower power consumption than their DT counterparts.

It has also been shown, in [Zwan97], that CT $\Sigma\Delta$ modulators are less sensitive to asynchronous substrate interference from neighbouring digital circuitry than DT $\Sigma\Delta$ modulators. This will be an important issue for future SoC (System on Chip) design.

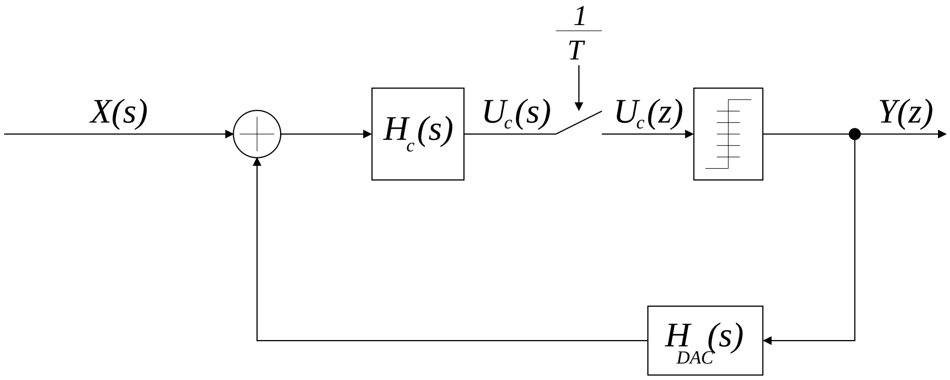

Figure 2.2: *Continuous-time* ΣΔ *modulator*.

While DT ΣΔ modulators are insensitive to the shape of the feedback signal as long as full settling occurs, the main disadvantages of CT ΣΔ modulators are related to switching charateristics of the feedback signal:

- **Excess Loop Delay:**
  The delay in the feedback signal is mainly due to the non-zero comparator response-time. This delay has been found to alter the frequency response and degrade the signal-to-noise ratio (SNR) of the CT ΣΔ modulators [Cherry99]. Using a Return-to-Zero (RZ) feedback signal gives enough time for the comparator output to settle and thus eliminates any influence of the comparator delay on the SNR [Aboushady99a].

- **DAC Output Rise and Fall Time Asymmetry:**
  Unequal rise and fall times of the DAC output current introduces harmonic distortion [Zwan96]. The effect of this waveform asymmetry can also be highly attenuated by the use of a RZ feedback DAC.

- **Clock Jitter:**
  Clock jitter in feedback signal increases the noise level in the signal band. Unlike excess loop delay and DAC waveform asymmetry, clock jitter influence on the CT modulators cannot be attenuated by a RZ feedback signal. In fact, as we will see later in chapter 6, using a RZ feedback signal slightly increases the clock jitter effect on SNR. Other solutions to tackle this problem will then be discussed.

Table 2.1: *Main advantages of Continuous-time $\Sigma\Delta$ modulators over DT $\Sigma\Delta$ modulators.*

	DISCRETE-TIME $\Sigma\Delta$	CONTINUOUS-TIME $\Sigma\Delta$
Input Switch Resistance	$r_{ds} = \frac{1}{\beta(V_{gs}-V_t)}$	No input switches
Sampling Errors	Critical	Shaped out of band
Unity Gain Frequency	$f_T = 5 * f_s$	$f_T \leq f_s$
Thermal Noise Aliasing	Increases noise level	Highly attenuated
Anti-Aliasing Filter	Essential	May be discarded

Table 2.2: *Main disadvantages of Continuous-time $\Sigma\Delta$ modulators compared to DT $\Sigma\Delta$ modulators.*

	DISCRETE-TIME $\Sigma\Delta$	CONTINUOUS-TIME $\Sigma\Delta$
Excess Loop Delay	Low sensitivity	SNR degradation
Rise and Fall Time Asymmetry	Low sensitivity	Introduces harmonic distortion
Clock Jitter	Low sensitivity	Increases noise level

After this discussion on the advantages and disadvantages of CT $\Sigma\Delta$ modulators compared to the DT $\Sigma\Delta$ modulators (summarized in tables 2.1 and 2.2), we believe that CT modulators will play an important role in recent and future CMOS technologies. This is mainly because of their advantages concerning low voltage, low power and high sampling frequency.

In the following, we will discuss the main difficulties and the different issues associated with the design and implementation of CT $\Sigma\Delta$ modulators.

2.3 Continuous-Time $\Sigma\Delta$ Design Issues

2.3.1 System Design

In fact, CT $\Sigma\Delta$ are mixed CT-DT systems. While the input signal is continuous and the loop filter is composed of CT integrators, the output signal is sampled. The feedback DAC signal can either have a constant output during each clock cycle (NRZ case), or have its output change during the clock cycle (RZ case). This makes the calculation of the CT $\Sigma\Delta$ modulator coefficients, in order to obtain the required Noise Transfer Function (NTF), a mathematically difficult task.

In a low power design, the NTF should designed in such a way that the in-band quantization noise is sufficiently low to be neglected compared to the circuit transistors noise. After the calculations of the proper CT ΣΔ coefficients required to obtain the desired NTF, these coefficients should be scaled for maximum output swing of the integrators. Nevertheless, these coefficients may appear to degrade the modulator circuit performances when realized in the transistor level. In this case, the modulator coefficients are scaled according to the first integrator gain which was found to give the desired circuit performances.

Note also that compared to DT ΣΔ simulations, CT ΣΔ modulators simulations are very lengthy. Moreover, DAC circuit imperfections are particularly difficult to model in a system level simulation.

2.3.2 Circuit Design

Continuous-time ΣΔ modulators are composed of CT integrators, comparators and feedback DACs.

Integrator Circuit

For proper operation of the CT ΣΔ modulator, integrator circuit frequency response must satisfy a specific transfer function. In fact, each integrator has a gain which is determined during system level design. This gain is also dependent on the sampling frequency of the modulator. Furthermore, the first integrator, along with the first feedback DAC, determines the circuit noise (thermal and 1/f noise) level of the modulator [Signore90]. Therefore the integrating capacitance and the biasing current of the first integrator have to be calculated carefully in order to satisfy the desired signal-to-noise ratio while having the correct frequency response to insure proper operation of the ΣΔ modulator.

Note however, that if the desired specifications cannot be met, the first integrator gain can be modified. In this case, it is necessary to go back to the system level design to scale the rest of the coefficients accordingly.

The transistor lengths must be chosen in such a way that the area of the transistors is large enough to reduce the 1/f noise to the desired level.

Satisfying all the above requirements while keeping the power consumption as low as possible, is indeed a challenging task in the circuit design of CT $\Sigma\Delta$ integrators.

DAC Circuit and Digital control

As described in section 2.2, CT $\Sigma\Delta$ modulators are sensitive to the DAC output waveform characteristics. Any delay, rise and fall time asymmetry or jittered transitions can significantly degrade the signal-to-noise ratio of the modulator. The DAC circuit and its digital control circuitry have then to be designed carefully in order to reduce all possible switching errors. In feedback $\Sigma\Delta$ topologies the feedback coefficients determined on the system level design, along with the biasing current of the integrators, fix the current that should be drawn from the DACs.
Moreover, since the first DAC transistors contribute thermal and 1/f noise to the modulator, transistors dimensions must be chosen carefully.

2.3.3 Design Automation

From the previous discussions on the system and circuit design levels, we can see that there is strong interaction between the two design levels. It is obvious that any modification in the system level coefficients would require a complete redesign of all components at the transistor circuit design level. Furthermore, any modifications in the specifications of the modulator, or in the CMOS technology process would require a complete redesign at both the system and the circuit level. If hand-calculations are used for system and circuit design, this rapidly becomes a very tiresome task.
With the current high demand on mixed-signal systems (digital and analog) for SoC (Sytem on Chip) design, it has become necessary to develop design automation tools for the analog circuits in order to cope with the already mature and well-established digital circuits design automation tools [Gielen00].

2.3.4 Decimation Filter

The complete decimation filter of $\Sigma\Delta$ A/D converters, with an OSR of M is often divided into 4 subfilters, Figure 2.3:

- 1 Comb filter decimating by M_1 (where $M/M_1 = 4$).
- 2 Half-Band filters, each decimating by 2.

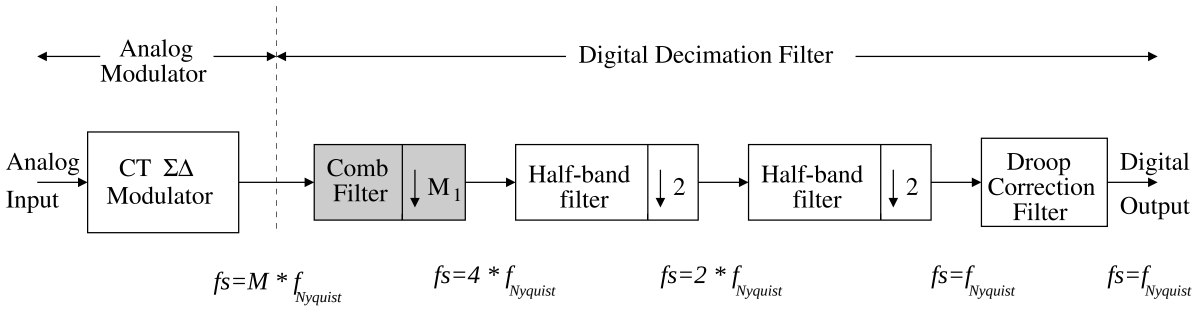

Figure 2.3: *The 4 subfilters of a* $\Sigma\Delta$ *A/D decimation filter*.

- 1 FIR filter for droop correction.

Due to its high operating frequency, the Comb filter dissipates most of the power consumption of the complete decimation filter [Barrett97]. With CT $\Sigma\Delta$ modulators, it is now possible to achieve very high sampling frequencies [Jensen95] [Cherry00] [Maurino00] [Raghavan01].
It is then necessary to find design techniques for the comb filter in order to reduce its power consumption.

After introducing the different design issues, we will now present the major contributions of this thesis in the design and implementation of CT $\Sigma\Delta$ A/D converters.

2.4 Major Contributions

While studying the design of reusable CT $\Sigma\Delta$ A/D converters, the main contributions can be summarized in the following five paragraphs:

2.4.1 Continuous-Time Sigma-Delta System Design

Since DT $\Sigma\Delta$ modulators are easier to design and simulate, we have chosen to start from the coefficients of a well-known DT $\Sigma\Delta$ modulator, and then use a transformation method to get the equivalent CT $\Sigma\Delta$. A DT to CT transformation method, based on the modified z transform technique, has been introduced in [Aboushady99a] and [Aboushady99b]. Using this transformation method, we can get the CT $\Sigma\Delta$ coefficients taking into account the RZ feedback signal. This transformation method has been succesfully applied to different architectures and orders of lowpass and bandpass $\Sigma\Delta$ modulators [Aboushady02a].

2.4.2 Low-power Low-Voltage Current-Mode Circuit Design

Current-mirror based circuits have been used to design the CT integrators. A design method is used to obtain the maximum modulation index (the ratio of the input signal over the biasing current). It is shown, by theoretical analysis and simulations, that maximum modulation index is obtained for supply voltages significantly lower than the maximum supply voltage of a given technology. It is found that there exists an optimum supply voltage for minimum power consumption [Aboushady01b]. This interesting result indicates that current-mode circuits may have interesting performances in recent and future low-voltage CMOS technologies. Furthermore, the regularity and the simplicity of current-mirror-based circuits make these circuits particularly well-suited to design automation. The main source of harmonic distortion of the current integrator is transconductance variation with the input signal. It is shown that by properly choosing the gain of the first integrator, harmonic distortion can be significantly reduced [Aboushady01c].

2.4.3 Analog Design Automation

A top-down design method for CT $\Sigma\Delta$ is presented. Starting from the DT $\Sigma\Delta$ coefficients, the modulator specifications (signal-to-noise-ratio, harmonic distortion, bandwidth, oversampling ratio), and the technology informations including BSIM or MM9 MOS transistor models, we generate the netlists of the current-mode integrators, the feedback DACs and the comparator. First DT-to-CT transformation, using the modified-z-transform technique, is automated in a *Maple* program. The biasing current and the capacitance of the current-mode integrator are chosen to satisfy the thermal noise requirements and the bandwidth specifications of the modulator. Finally, a circuit sizing tool is implemented to calculate the dimensions of all transistors for a given CMOS process. This design procedure has been introduced in the COMDIAC environement [Porte99] using a C program, with a tcl-tk graphical interface for a third order CT modulator. This has allowed us to easily design and simulate several $\Sigma\Delta$ modulators with different specifications and different technologies.

2.4.4 Circuit Implementation and Measurements Results

In order to validate the design procedure described in the previous section, a fully differential third order $\Sigma\Delta$ modulator has been implemented in 0.18 μm CMOS process with polysilicon-

nwell capacitors. The modulator achieves 84 dB dynamic range and occupies 1.56 mm2. With a sampling frequency of 26 MHz, the modulator consumes 5mW at 1.8V. The peak SNR is 79dB in 100kHz bandwidth. The total harmonic distortion is -79dB for 25 kHz input signal.
This circuit is the first implementation of a current-mode CT $\Sigma\Delta$ modulator.

2.4.5 Decimation Filter

In order to reduce its power consumption, we propose to use a multi-rate multi-stage Comb decimation filter. Polyphase decomposition in all stages, with high decimation factor in the first stage, is used to significantly reduce the sampling frequency. It is shown, by theoretical analysis and simulations, that proper choice of the first stage decimation factor can considerably improve power consumption, area and maximum sampling frequency. Both mono-bit and multi-bit $\Sigma\Delta$ have been studied. In multi-bit A/D, the optimum first stage decimation factor is function of the input wordlength [Aboushady01a].

2.5 Conclusion

In this chapter, it has been shown that due to their advantages concerning low-voltage, low-power and high sampling frequency, CT $\Sigma\Delta$ modulators may outperform conventional DT $\Sigma\Delta$ modulators, especially in recent and future low-voltage CMOS technologies.
However CT $\Sigma\Delta$ modulators are mathematically more complex to design, there is strong interaction between system and circuit design levels, and special care must be taken while designing the feedback signal. Furthermore simulation of CT $\Sigma\Delta$ modulators is much more time consuming than DT $\Sigma\Delta$ simulation.
Design reuse through design automation is the best way to profit from CT $\Sigma\Delta$ advantages without spending too much effort and time in the design.
The main contributions of this thesis mainly focus on identifying major design difficulties and finding systematic design approaches, suitable for design automation, in order to render the design of CT $\Sigma\Delta$ easier and faster.

Chapter 3

State of the Art

3.1 Introduction

In this chapter we present the state of the art in the field of CT $\Sigma\Delta$ modulators.
Previous work on the system level design of CT $\Sigma\Delta$ modulators with NRZ and RZ feedback signal is presented in section 3.2.
An overview of the different CT $\Sigma\Delta$ circuit implementations is given in section 3.3.
The different design automation approaches used for DT and CT $\Sigma\Delta$ modulators and analog circuit synthesis are given in section 3.4.
Finally filter architectures used to implement the $\Sigma\Delta$ Comb decimation filter are described in section 3.5.

3.2 Continuous-Time $\Sigma\Delta$ System Design

In order to overcome problems associated with the design and analysis of mixed CT-DT systems, CT $\Sigma\Delta$ modulators can be designed entirely in the DT domain. A DT-to-CT transformation method can then be applied in order to obtain the equivalent CT $\Sigma\Delta$ modulator.

Previous work on $\Sigma\Delta$ DT-to-CT transformation, has usually performed this transformation in the time domain. The complicated mathematics involved in the computation of time-domain convolution renders this method not adapted to design automation and has usually been used for specific cases [Candy85] [Thurston91] [Shoaei95].

A more general transformation method using state-space representation has been presented in

[Schreier96]. Heavy use of matrix notation, singularity problems and the use of special control and optimization MATLAB functions [Schreier99] make the use this transformation technique rather difficult.

In this work we propose to perform the DT-CT equivalence directly in the z domain using the *modified-z-transform* technique [Jury64]. While avoiding the complex mathematics necessary to perform time-domain convolution, this technique enables us to get the z-transform of signals having variations between two sampling instants.

In this thesis we present a general method for an n^{th} order CT modulator. This method is valid for the different lowpass and bandpass $\Sigma\Delta$ topologies. The feedback DAC can be RZ or NRZ and the shape of the feedback signal can either be rectangular or non-rectangular.
The proposed method is also well-suited for design automation.

3.3 Continuous-Time $\Sigma\Delta$ Circuit Implementations

3.3.1 Bipolar Transistors

Continuous-time $\Sigma\Delta$ modulators have received increasing attention in Heterojunction Bipolar Transistor (HBT) technologies which cannot easily accomodate switched-capacitor (SC) circuits. Many CT $\Sigma\Delta$ with very high sampling frequency have been implemented in these technologies. Bandpass modulators having sampling frequencies in the GHz range have been reported [Cherry00][Maurino00][Raghavan01].

In this thesis we will mainly focus on CT $\Sigma\Delta$ modulators in standard low-cost digital CMOS technologies.

3.3.2 MOS Transistors

Different techniques have been used to implement integrators for CT $\Sigma\Delta$ modulators in CMOS technology:

- **RC Integrators:** RC integrators have been used to implement a low-voltage second order lowpass CT modulator [Matsuya94][1] and a sixth order CT bandpass $\Sigma\Delta$ for digital radio IF [Engelen99].

[1]MTCMOS: Multi-Threshold CMOS technology process.

- **Gm-C Integrators:** A first order current steering $\Sigma\Delta$ modulator has been presented in [Comino91] and a low-power forth order $\Sigma\Delta$ modulator with 80 dB dynamic range for speech coding has been presented in [Zwan96].

- **RC/Gm-C Integrators:** The best performances of lowpass CT $\Sigma\Delta$ modulators have been achieved using an RC integrator in the first stage and Gm-C integrators for the subsequent stages. This architecture has been used for high resolution audio applications in [Zwan97] and for telecommunications applications in [Breems00] [Zwan00].

- **Current-Mirror based Integrators:** Low-power low-voltage implementations of CT current-mode filters have been reported [Zele96]. A study on a first-order CT $\Sigma\Delta$ modulator using CT current-mode integrator has been presented in [Mittal95].

In this work we have implemented a 79 dB SNR, 100 kHz bandwidth, third-order CT $\Sigma\Delta$ modulator for telecommunication applications with current-mode integrators [Aboushady02b]. The circuit consumes 5 mW at 1.8V in a standard digital 0.18 μm CMOS process.
It will be shown later in chapter 8 that, when compared to other recently published $\Sigma\Delta$ modulators having similar bandwidth specifications, the proposed current-mode CT $\Sigma\Delta$ modulator have a better Figure of Merit than all the DT SC implementations and most of other CT implementations.

3.4 Design automation of $\Sigma\Delta$ modulators

3.4.1 System Level Design Automation

The Delta-Sigma Toolbox [Schreier99] contains many useful MATLAB functions that can be used for the design of single-bit DT $\Sigma\Delta$ modulators. The design method for multi-bit DT $\Sigma\Delta$ modulators proposed in [Kenney93] is also included in *The Delta-Sigma Toolbox*.
Using the state-space method mentioned in section 3.2, it is possible to design CT LC-bandpass modulators with RZ feedback.

In this work a general design procedure for RZ CT $\Sigma\Delta$ starting from a DT $\Sigma\Delta$, using the modified-z-transform technique, is implemented in a symbolic mathematical tool *MAPLE* [Wat97]. The advantage of using a symbolic tool is that the resulting CT coefficients are expressed in function of the DT coefficients and the CT feedback signal characteristics. This means that for a given ΣΔ topology and order, the design procedure is performed only once using *MAPLE*. Simple substitutions are then required to get the numerical values of the CT coefficients.

3.4.2 Circuit Level Design Automation

Two main approaches exist for analog circuit synthesis [Carley96] [Gielen00]:

- **Optimzation-based approach:**
  Either symbolic models or SPICE-like circuit simulations are used to evaluate the circuit performances. Optimization routines are then used to modify the design parameters (transistors dimensions, biasing currents and voltages, ...) until the desired specifications are reached [Nye88][Koh90][Gielen93][Medeiro94].

- **Knowledge-based approach:**
  Analog design knowledge is exploited to perform circuit sizing. This includes topological and analytical knowledge, rules of thumb, heuristics and simplified models [Degrauwe87][Harjani89][Porte99].

In this work only the knowledge-based approach will be discussed.

COMDIAC [Porte99] is a circuit sizing environment mainly dedicated to opamp synthesis. COMDIAC is based on a powerful transistor sizing tool. In fact, the two most popular MOS transistor simulation models: BSIM [Berkeley00] and MM9 [Philips00], are implemented in this tool and are used to accurately calculate the transistor dimensions. This is an important feature that considerably reduces the number of iterations in a top-down design flow. In addition, the transistor sizing tool in COMDIAC can also calculate DC and small-signal parameters of each transistor.

In chapter 7 of this thesis, we present a knowledge-based CT ΣΔ modulator circuit sizing tool. This tool has been implemented in the COMDIAC environment and uses its transistor sizing tool.

3.5 Decimation Filter

Power consumption of decimation filters in ΣΔ A/D converters is receiving increasing attention [Pan00][Maulik00][Gao00]. Comb filters are widely used in the decimation filter of ΣΔ A/D converters. These filters are usually implemented using the IIR-FIR technique [Dijkstra88].

Although the output of a $\Sigma\Delta$ modulator is coded on a very small number of bits, the wordlength of the IIR filter has to be large to avoid any register overflow [Hogenauer81]. The major drawback of this architecture is that the IIR filter is operating at maximum sampling frequency and with a large wordlength. This considerably increases the power consumption of Comb filters [Aboushady97] [Barrett97].
Recently, lower power consumption has been achieved using the FIR2 [Gao00] and the POLY-FIR2 [Gao99] implementations. These FIR architectures have the advantage of having a limited wordlength.

In this work we present a different FIR architecture of the Comb filter. This architecture allows us to exploit the Polyphase decomposition in order to perform higher decimation factors at the input of the first stage. It is shown that the proper choice of the first stage decimation factor can significantly improve power consumption, area and maximum sampling frequency [Aboushady01a].

3.6 Conclusion

After analyzing the current CT $\Sigma\Delta$ modulator design techniques, we can deduce the following conclusions:

- DT-to-CT $\Sigma\Delta$ transformation techniques based on time-domain convolution are not well-suited for design automation.
- Despite their simplicity and good performances in filters, current-mirror based integrators have never been used to implement a CT $\Sigma\Delta$ modulator.
- *The Delta-Sigma Toolbox* offers one function to design CT LC-bandpass $\Sigma\Delta$ modulators, but a general DT-to-CT transformation tool is not available.
- COMDIAC, with its powerful transistor sizing tool, offers a favorable environment to implement a top-down circuit synthesis design automation tool for current-mode CT $\Sigma\Delta$ modulators.
- New filter architectures are needed to reduce high power consumption of Comb decimation filters.

Chapter 4

Discrete-Time to Continuous-Time Transformation

4.1 Introduction

In this chapter we present a systematic approach for DT-to-CT transformation of $\Sigma\Delta$ modulators. First a brief review of the current techniques used to perform DT-CT equivalence of $\Sigma\Delta$ modulators is given in section 4.2.

In section 4.3, the modified-z-transform technique is used to calculate the z-transform the loop gain of CT $\Sigma\Delta$ with RZ feedback signals.

Based on this technique, a systematic design approach for the most common $\Sigma\Delta$ topologies is described in section 4.5.

Finally several design examples of high order lowpass and bandpass CT $\Sigma\Delta$ modulators with RZ and NRZ are given in order to validate the proposed design approach.

4.2 Equivalence between Discrete-Time and Continuous-Time $\Sigma\Delta$ modulators

CT $\Sigma\Delta$ modulators are mixed CT-DT systems. While the input signal is continuous and the loop filter is composed of CT integrators, the output signal is sampled. The feedback DAC signal can either have a constant output during each clock cycle (NRZ case), or have its output change during the clock cycle (RZ case). This makes the calculation of the CT $\Sigma\Delta$ Noise Transfer Function (NTF),

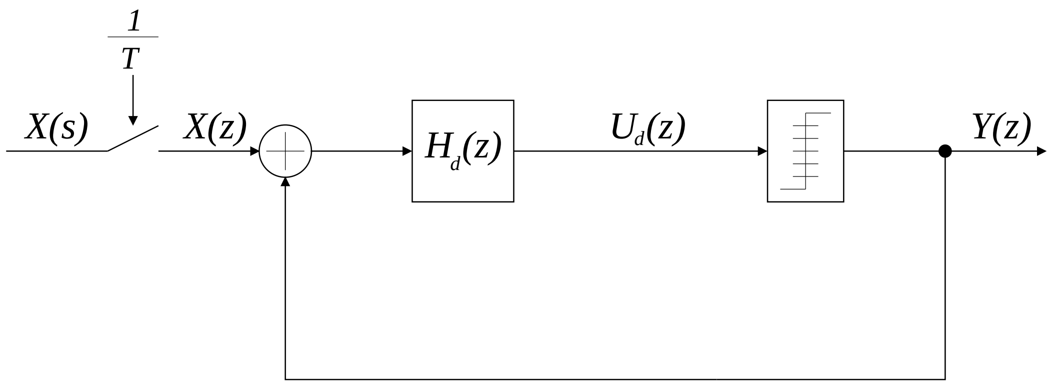

Figure 4.1: *Discrete-time* $\Sigma\Delta$ *modulator*.

a mathematically difficult task.

A general DT $\Sigma\Delta$ modulator is shown in Figure 4.1, where $H_d(z)$ is the DT loop filter. A general CT $\Sigma\Delta$ modulator is shown in Figure 4.2, where $H_c(s)$ is the CT loop filter and $H_{DAC}(s)$ the CT feedback DAC transfer function.

Note that the output $Y(z)$ and the input of the comparator $U(z)$ are DT signals in both DT and CT systems shown in Figures 4.1 and 4.2.

The objective is to design, for a given feedback DAC transfer function $H_{DAC}(s)$, the CT loop filter $H_c(s)$ so that the CT $\Sigma\Delta$ loop gain $G_c(z)$ is equal to the DT $\Sigma\Delta$ loop gain $G_d(z)$. This can be expressed by

$$\begin{aligned} G_d(z) &= G_c(z) \\ \frac{U_d(z)}{Y_d(z)} &= \frac{U_c(z)}{Y_c(z)} \\ G_d(z) &= \mathcal{Z}\left[H_c(s)\ \ H_{DAC}(s)\right] \end{aligned} \tag{4.1}$$

where $G_d(z) = H_d(s)$.

Previous work on $\Sigma\Delta$ DT-CT equivalence has usually solved equation (4.1) in the time domain using the following relation

$$\mathcal{Z}^{-1}\left[G_d(z)\right] \;=\; \mathcal{L}^{-1}\left[H_c(s)\ \ H_{DAC}(s)\right] \tag{4.2}$$

Due to the complicated mathematics involved in the computation of time-domain convolution, solving equation (4.2) is not well-suited for design automation and has usually been used for specific cases:

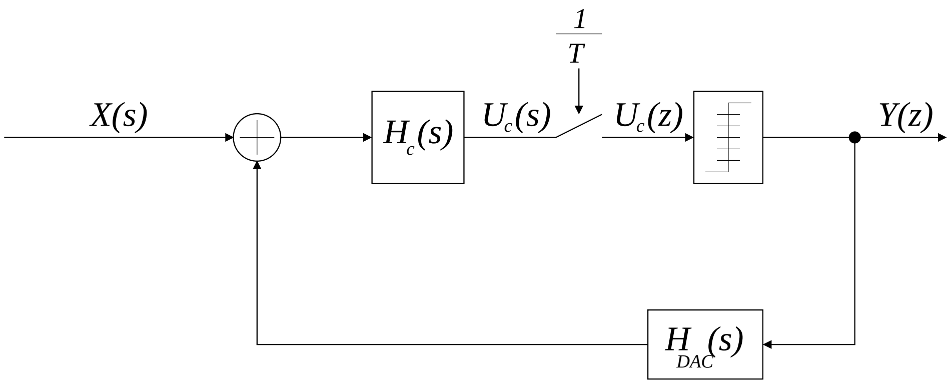

Figure 4.2: *Continuous-time* ΣΔ *modulator*.

- [Candy85]: second order low-pass CT ΣΔ modulator with NRZ feedback signal.

- [Thurston91]: cascade of Resonators bandpass CT ΣΔ modulator with NRZ feedback signal.

- [Shoaei95]: second and fourth order bandpass CT ΣΔ modulators with NRZ and RZ feedback signal.

A more general transformation method, using state-space representation has been presented in [Schreier96]. Heavy use of matrix notation, singularity problems and the use of special control and optimization MATLAB functions [Schreier99] make the use this transformation technique rather difficult.

In this work, we propose to solve equation (4.1) directly in the z domain using the *modified-z-transform* technique [Jury64]. While avoiding the complex mathematics necessary to perform time-domain convolution, this technique enables us to get the z-transform of signals having variations between two sampling instants.

In the following, we present a general method for an n^{th} order CT modulator. This method is valid for the different lowpass and bandpass ΣΔ topologies. The feedback DAC can be RZ or NRZ and the shape of the feedback signal can either be rectangular or non-rectangular.

4.3 z-Transform of Continuous-Time $\Sigma\Delta$ Loop Gain

4.3.1 Rectangular Feedback Signal

During a period T, the rectangular feedback signal, shown in Fig.4.3, can be described in the time domain by the following relationship:

$$h_{dac}(t) = u(t - t_d) - u(t - t_d - \tau) \tag{4.3}$$

where $u(t)$ is unit step function. Applying the *Laplace* transform, we get

$$H_{DAC}(s) = \frac{e^{-t_d s} - e^{-(t_d+\tau)s}}{s} \tag{4.4}$$

The z-transform of the CT $\Sigma\Delta$ loop gain can be expressed by

$$\mathcal{Z}\left[G_c(s)\right] \quad = \quad \mathcal{Z}\left[H_c(s) \;\; H_{DAC}(s)\right] \tag{4.5}$$

by substitution from equation (4.4) into equation (4.5), we have

$$G_c(z) = \mathcal{Z}\left[\frac{H_c(s)\; e^{-t_d s}}{s}\right] - \mathcal{Z}\left[\frac{H_c(s)\; e^{-(t_d+\tau)s}}{s}\right] \tag{4.6}$$

The conventional z-transform cannot be used to represent any variations occuring between two consecutive sampling instants. Since $0 \leq t_d < T$ and $0 < t_d + \tau \leq T$, another mathematical approach has to be used to represent equation (4.6) in the discrete-time z domain.
The modified-z-transform method is a modification of the z-transform method so that the output at any time between two consecutive sampling instants can be obtained [Jury64].
Equation (4.6) is rewritten in the following form:

$$G_c(z) \quad = \quad \mathcal{Z}_{m_1}\left[\frac{H_c(s)}{s}\right] - \mathcal{Z}_{m_2}\left[\frac{H_c(s)}{s}\right] \tag{4.7}$$

where $m_1 = 1 - \frac{t_d}{T}$ and $m_2 = 1 - \frac{(t_d+\tau)}{T}$. Equation (4.7) is a general expression that can be used to obtain the loop gain $G_c(z)$ of CT $\Sigma\Delta$ with rectangular RZ or NRZ feedback signals. Now, in

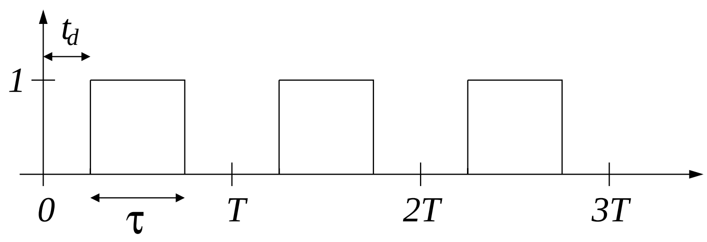

Figure 4.3: *Continuous-time rectangular feedback signal.*

order to design a CT $\Sigma\Delta$ modulator which is equivalent to a well-known DT $\Sigma\Delta$ modulator, we use equations (4.7) and (4.1) to get the general expression for DT-CT equivalence.

Conversion tables from the *Laplace* domain to the z domain exists for the modified-z-transform as it is the case for the conventional z-transform [Jury64][Sévely73]. Another method to calculate the modified-z-transform starting from the *Laplace* representation is the *Residue* theorem [Ogata87]. This method is systematic and much more convenient for design automation. Equation (4.7) can then be written in the following form

$$\begin{aligned} G_c(z) = & \sum_{p_i=\text{poles of } \frac{H_c(s)}{s}} \text{Residues of } \left. \frac{H_c(s)}{s} \frac{e^{m_1 Ts}}{z - e^{Ts}} \right|_{\text{at } p_i} \\ - & \sum_{p_i=\text{poles of } \frac{H_c(s)}{s}} \text{Residues of } \left. \frac{H_c(s)}{s} \frac{e^{m_2 Ts}}{z - e^{Ts}} \right|_{\text{at } p_i} \end{aligned} \tag{4.8}$$

Using equation (4.8), the loop gain of the CT $\Sigma\Delta$ $G_c(z)$ signal can be expressed in the DT z domain. Comparing the coefficients of the numerator and the denominator of $G_c(z)$ with those of the DT loop gain $G_d(z)$, we can deduce the coefficients of the CT loop filter $H_c(s)$. This will be explained in detail, for the different $\Sigma\Delta$ topologies, in the section 4.5

Note that equation (4.8) is a general relation valid for both RZ and NRZ rectangular feedback signal. In the special case of a NRZ feedback signal, with $t_d = 0$ and $\tau = T$, and by substitution in equation (4.4), we have the well-known zero-order hold relation:

$$H_{DAC}(s) = \frac{1 - e^{-Ts}}{s} \tag{4.9}$$

In this case equation(4.6) will give the common relation:

$$G_c(z) = (1 - z^{-1})\mathcal{Z}\left[\frac{H_c(s)}{s}\right] \tag{4.10}$$

4.3.2 Non-Rectangular Feedback Signals

There are two main reasons which makes it useful to be able to design CT $\Sigma\Delta$ modulators with non-rectangular feedback signals. First, it can be used to model non-idealities in the rectangular feedback, e.g. non-zero rise and fall time. The second reason is that it is theoretically possible to use different feedback shapes to reduce the modulator sensitivity to clock jitter noise (chapter 6).

In this section we will show that the proposed DT-to-CT transformation method can be used for CT $\Sigma\Delta$ modulators with non-rectangular feedback signals. A decaying Ramp and a decaying RC signal are taken as examples.

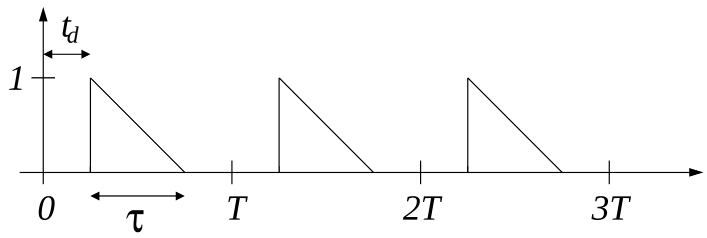

Figure 4.4: *Continuous-time decaying ramp feedback signal.*

4.3.2.1 Decaying Ramp Feedback Signal

Following the same procedure described in section 4.3.1, the decaying ramp feedback signal, shown in Figure 4.4, can be described in the time domain by the following relationship:

$$h_{dac_{ramp}}(t) = (1 - \frac{t-t_d}{\tau})[u(t-t_d) - u(t-t_d-\tau)] \tag{4.11}$$

Applying the Laplace transform, we get

$$H_{DAC_{RAMP}}(s) = \frac{e^{-(t_d+\tau)s}}{\tau s^2} - \frac{e^{-t_d s}}{\tau s^2} + \frac{e^{-t_d s}}{s} \tag{4.12}$$

The z transform of the CT $\Sigma\Delta$ loop gain can be expressed by

$$\mathcal{Z}(G_c(s)) \quad = \quad \mathcal{Z}(H_c(s) \;\; H_{DAC_{RAMP}}(s)) \tag{4.13}$$

by substitution from equation (4.12) into equation (4.13), we have

$$\mathcal{Z}\left[G_c(s)\right] \quad = \quad \frac{1}{\tau}\mathcal{Z}\left[\frac{H_c(s) \;\; e^{-(t_d+\tau)s}}{s^2}\right] - \frac{1}{\tau}\mathcal{Z}\left[\frac{H_c(s) \;\; e^{-t_d s}}{s^2}\right] + \mathcal{Z}\left[\frac{H_c(s) \;\; e^{-t_d s}}{s}\right] \tag{4.14}$$

Using the modified z transform representation, we can express equation (4.14) in the following form:

$$G_c(z) \quad = \quad \frac{1}{\tau}\mathcal{Z}_{m2}\left[\frac{H_c(s)}{s^2}\right] - \frac{1}{\tau}\mathcal{Z}_{m1}\left[\frac{H_c(s)}{s^2}\right] + \mathcal{Z}_{m1}\left[\frac{H_c(s)}{s}\right] \tag{4.15}$$

where $m_1 = 1 - \frac{t_d}{T}$ and $m_2 = 1 - \frac{(t_d+\tau)}{T}$. The modified z transform can be calculated using the residues method as described in equation (4.8).

4.3.2.2 Decaying RC Feedback Signal

Another more realistic and easier-to-implement feedback signal is the decaying RC signal, shown in Figure 4.5. Following the same procedure described in section 4.3.2, the decaying RC feedback

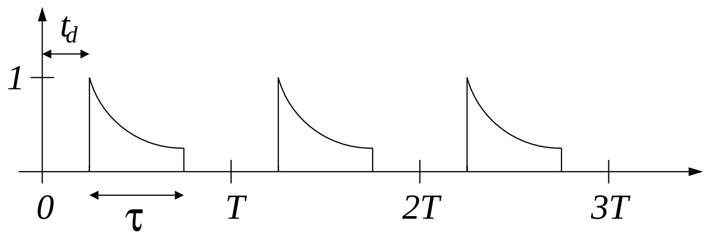

Figure 4.5: *Continuous-time decaying RC feedback signal.*

signal can be described in the time domain by the following relationship:

$$h_{dac_{rc}}(t) = e^{-\frac{1}{RC}(t-t_d)}[u(t-t_d) - u(t-t_d-\tau)] \tag{4.16}$$

Applying the Laplace transform, we get

$$H_{DAC_{RC}}(s) = \frac{e^{-t_d s} - e^{-(t_d+\tau)s}e^{\frac{-\tau}{RC}}}{s + \frac{1}{RC}} \tag{4.17}$$

The z transform of the CT ΣΔ loop gain can be expressed by

$$\mathcal{Z}[G_c(s)] \quad = \quad \mathcal{Z}\left[H_c(s) \;\; H_{DAC_{RC}}(s)\right] \tag{4.18}$$

by substitution from equation (4.17) into equation (4.18), we have

$$\mathcal{Z}\left[G_c(s)\right] \quad = \quad \mathcal{Z}\left[\frac{H_c(s) \;\; e^{-t_d s}}{s + \frac{1}{RC}}\right] - \mathcal{Z}\left[\frac{H_c(s) \;\; e^{-(t_d+\tau)s}}{s + \frac{1}{RC}}\right] e^{\frac{-\tau}{RC}} \tag{4.19}$$

Using the modified z transform representation, we can express equation (4.19) in the following form:

$$G_c(z) \quad = \quad \mathcal{Z}_{m1}\left[\frac{H_c(s)}{s + \frac{1}{RC}}\right] - e^{-\frac{\tau}{RC}}\mathcal{Z}_{m2}\left[\frac{H_c(s)}{s + \frac{1}{RC}}\right] \tag{4.20}$$

where $m_1 = 1 - \frac{t_d}{T}$ and $m_2 = 1 - \frac{(t_d+\tau)}{T}$. The modified z transform can be calculated using the residues method as described in equation (4.8).

4.4 Continuous-Time ΣΔ Signal Transfer Function

The CT loop filter $H_c(s)$ design procedure described in the previous sections ensures that the Noise Transfer Function (NTF) of the CT modulator is the same as the NTF of the DT modulator. On the other hand, this design procedure does not guarantee that the Signal Transfer Function

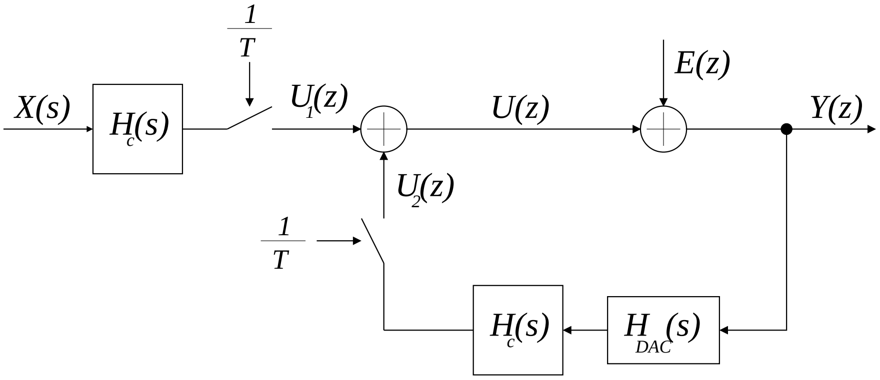

Figure 4.6: *Another representation of the CT $\Sigma\Delta$ shown in Figure 4.2, used to calculate the STF and the NTF.*

(STF) of the CT modulator is the same as the STF of the DT modulator. This stems from the fact that it is not possible to describe the STF of the CT modulator in the DT z domain as it is possible for the NTF.

In Figure (4.7), we show another representation of the general CT $\Sigma\Delta$ modulator of Figure (4.2). Note that the comparator is replaced by its linear model [Candy92], where $E(z)$ is the quantization error. The CT $\Sigma\Delta$ output signal, $Y(z)$, can be described in function of the CT input signal, $X(s)$, and the DT error signal, $E(z)$, by the following relation:

$$Y(z) \quad = \quad \frac{\mathcal{Z}\left[X(s)\;\; H_c(s)\right]}{1-\mathcal{Z}\left[H_c(s)\;\; H_{DAC}(s)\right]}+\frac{E(z)}{1-\mathcal{Z}\left[H_c(s)\;\; H_{DAC}(s)\right]} \tag{4.21}$$

From the previous section, we know that $H_d(z) = \mathcal{Z}\left[H_c(s)\;\; H_{DAC}(s)\right]$. Substituting in equation (4.21), we get

$$Y(z) \quad = \quad \frac{\mathcal{Z}\left[X(s)\;\; H_c(s)\right]}{1-H_d(z)}+\frac{E(z)}{1-H_d(z)} \tag{4.22}$$

From equation (4.22), we see that the CT NTF is identical to the DT NTF, and can be described by

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1-H_d(z)} \tag{4.23}$$

On the other hand, knowing that

$$\mathcal{Z}\left[X(s)\; H_c(s)\right] \neq \mathcal{Z}[X(s)]\; \mathcal{Z}[H_c(s)] \tag{4.24}$$

the STF cannot be represented in the DT z domain. Therefore, we will express the STF in the frequency domain using the Fourier Transform

$$STF(jw) = \frac{Y(e^{jw})}{X(jw)} = \frac{H_c(jw)}{1-H_d(e^{jw})} \tag{4.25}$$

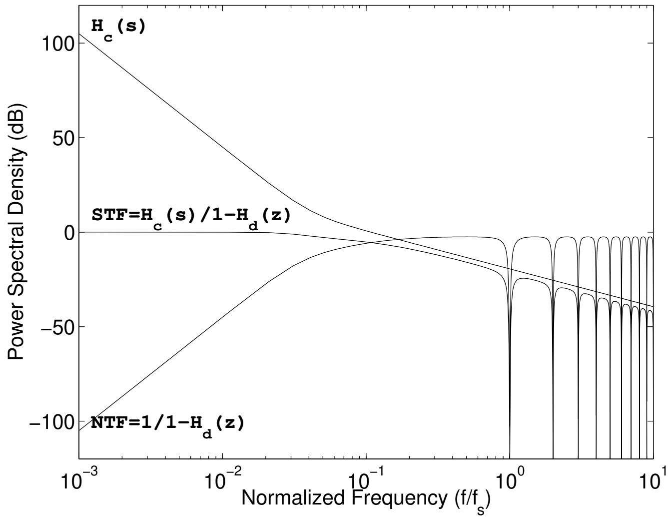

Figure 4.7: *$STF(jw)$, $NTF(e^{jw})$ and the CT loop filter $H_c(jw)$ of a 3^{rd} order feedforward structure $\Sigma\Delta$ modulator.*

Figure 4.4, shows the $STF(jw)$, $NTF(e^{jw})$ and the CT loop filter $H_c(jw)$ of a 3^{rd} order feedforward structure $\Sigma\Delta$ modulator. It is important to note that the STF has a flat frequency response in the band of interest.

4.5 Systematic Design Approach

In this section we present a systematic design approach for the most common DT and CT $\Sigma\Delta$ modulator topologies. The two main topologies are cascade of integrators and cascade of resonators [Norsworthy97] [Schreier99]. Both of these topologies can be implemented either in feedforward or a feedback form. In the following we will study, without loss of generality, 3 main topologies:

- CIFF: Cascade of Integrators Feedforward Form, Figures 4.8 and 4.9
- even CRFF: even order Cascade of Resonators Feedforward Form, Figures 4.10 and 4.11
- odd CRFF: odd order Cascade of Resonators Feedforward Form, Figures 4.12 and 4.11

The feedback forms, CIFB and CRFB, can be directly deduced from the feedforward form and vice-versa.

The DT and CT loop filters of the CIFF, even CRFF and odd CRFF topology are listed in tables

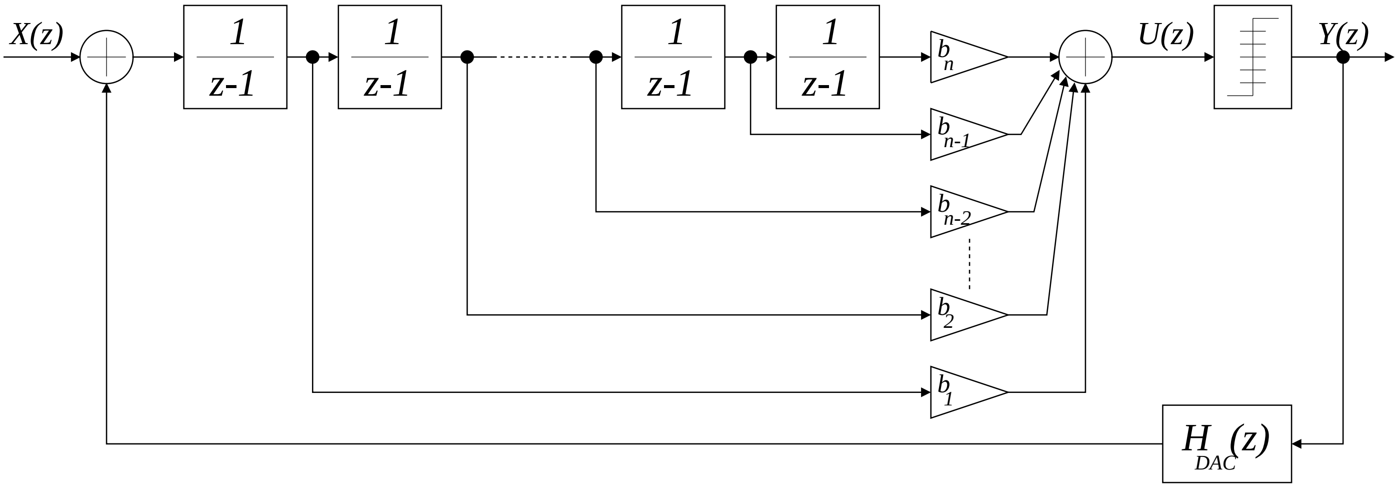

Figure 4.8: *Discrete-Time CIFF*.

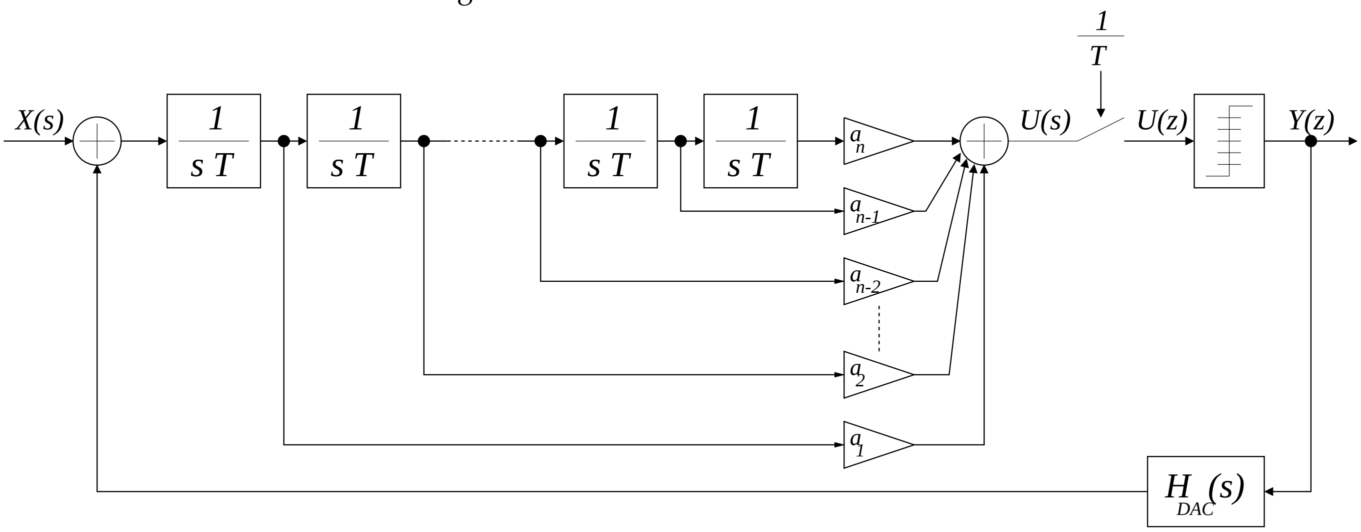

Figure 4.9: *Continuous-time CIFF*.

Table 4.1: *Loop filter of CIFF $\Sigma\Delta$ modulators*.

n^{th} order CIFF		
DT	$H_d(z)$	$\sum_{i=1}^{n} \frac{b_i}{(z-1)^i}$
CT	$H_c(s)$	$\sum_{i=1}^{n} \frac{a_i}{(sT)^i}$

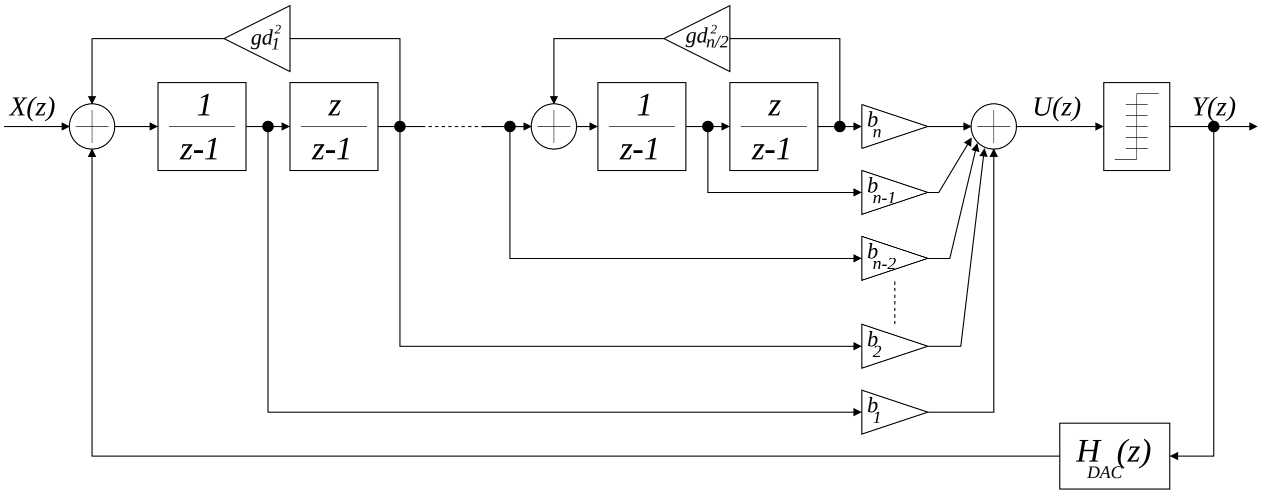

Figure 4.10: *Discrete-time even CRFF*.

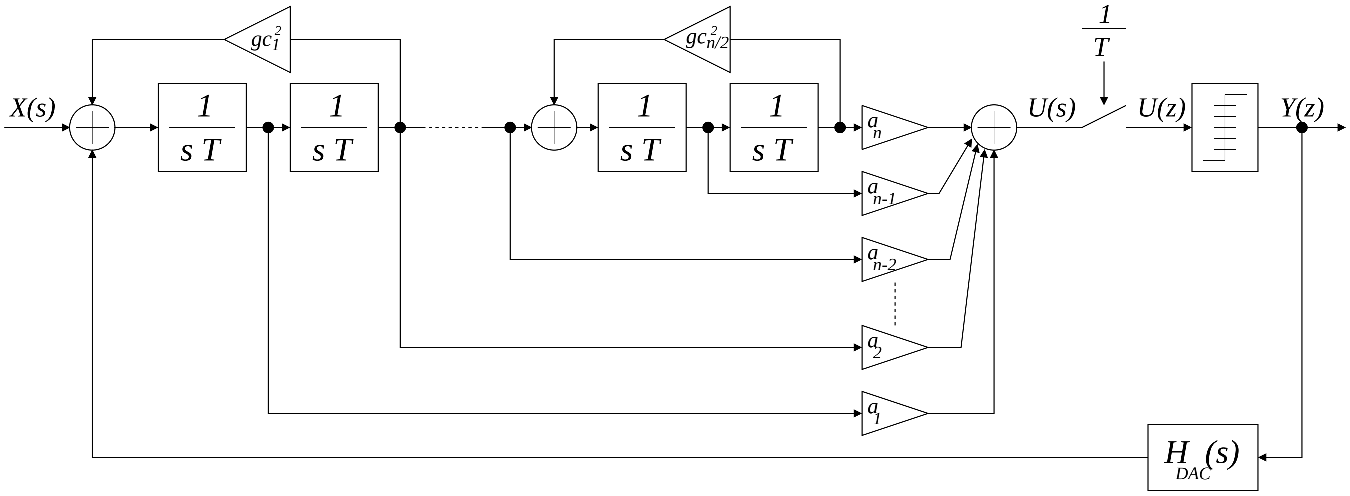

Figure 4.11: *Continuous-time even CRFF*.

Table 4.2: *Loop filter of even CRFF* $\Sigma\Delta$ *modulators*.

n^{th} order even CRFF		
DT	$H_d(z)$	$\sum_{i\ odd}^{n} \frac{b_i \quad z^{\frac{i-1}{2}}(z-1)}{\prod_{j=1}^{\frac{i+1}{2}}(z^2-(2-{g_{d_j}}^2)+1)} + \sum_{i\ even}^{n} \frac{b_i \quad z^{\frac{i}{2}}}{\prod_{j=1}^{\frac{i}{2}}(z^2-(2-{g_{d_j}}^2)+1)}$
CT	$H_c(s)$	$\sum_{i\ odd}^{n} \frac{a_i \quad (Ts)}{\prod_{j=1}^{\frac{i+1}{2}}[(Ts)^2-{g_{c_j}}^2]} + \sum_{i\ even}^{n} \frac{a_i}{\prod_{j=1}^{\frac{i}{2}}[(Ts)^2-{g_{c_j}}^2]}$

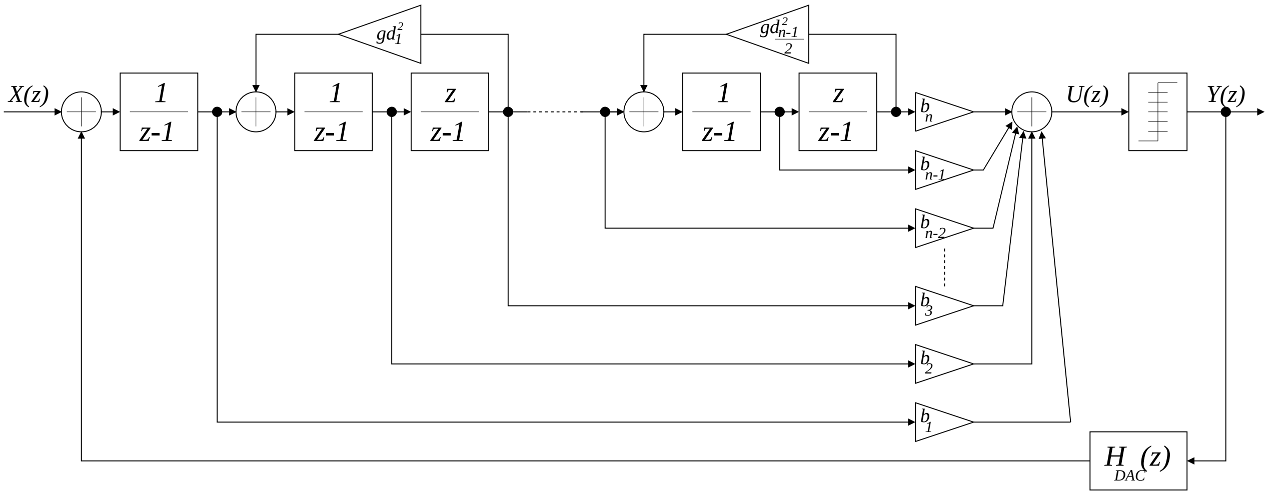

Figure 4.12: *Discrete-time odd CRFF*.

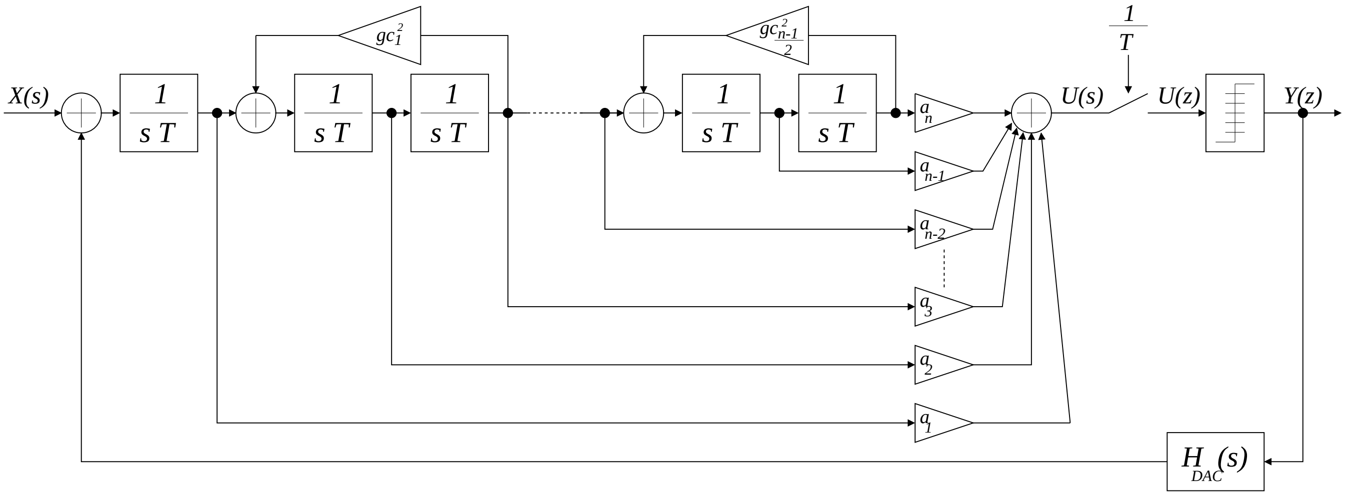

Figure 4.13: *Continuous-time odd CRFF*.

Table 4.3: *Loop filter of odd CRFF $\Sigma\Delta$ modulators*.

n^{th} order odd CRFF		
DT	$H_d(z)$	$\sum_{i\ odd}^{n} \frac{b_i\ z^{\frac{i-1}{2}}}{(z-1)\prod_{j=1}^{\frac{i-1}{2}}(z^2-(2-{g_{d_j}}^2)+1)} + \sum_{i\ even}^{n} \frac{b_i\ z^{\frac{i}{2}}}{\prod_{j=1}^{\frac{i}{2}}(z^2-(2-{g_{d_j}}^2)+1)}$
CT	$H_c(s)$	$\sum_{i\ odd}^{n} \frac{a_i}{(Ts)\prod_{j=1}^{\frac{i-1}{2}}[(Ts)^2-{g_{c_j}}^2]} + \sum_{i\ even}^{n} \frac{a_i}{\prod_{j=1}^{\frac{i}{2}}[(Ts)^2-{g_{c_j}}^2]}$

Table 4.4: *Loop gain of CIFF $\Sigma\Delta$ modulators.*

n^{th} order CIFF		
DT	$G_d(z)$	$\frac{\alpha_{d_{n-1}} z^{n-1}+\alpha_{d_{n-2}} z^{n-2}+\cdots+\alpha_{d_1} z+\alpha_{d_0}}{\beta_{d_n} z^n+\beta_{d_{n-1}} z^{n-1}+\cdots+\beta_{d_1} z+\beta_{d_0}}$
CT	$G_c(z)$	$\frac{\alpha_{c_{n-1}} z^{n-1}+\alpha_{c_{n-2}} z^{n-2}+\cdots+\alpha_{c_1} z+\alpha_{c_0}}{\beta_{c_n} z^n+\beta_{c_{n-1}} z^{n-1}+\cdots+\beta_{c_1} z+\beta_{c_0}}$

Table 4.5: *Loop gain of even CRFF $\Sigma\Delta$ modulators.*

n^{th} order even CRFF		
DT	$G_d(z)$	$\frac{\alpha_{d_{n-1}} z^{n-1}+\alpha_{d_{n-2}} z^{n-2}+\cdots+\alpha_{d_1} z+\alpha_{d_0}}{(z^2-(2-g_{d_1}{}^2)+1)(z^2-(2-g_{d_2}{}^2)z+1)...(z^2-(2-g_{d_{\frac{n}{2}}}{}^2)z+1)}$
CT	$G_c(z)$	$\frac{\alpha_{c_{n-1}} z^{n-1}+\alpha_{c_{n-2}} z^{n-2}+\cdots+\alpha_{c_1} z+\alpha_{c_0}}{(z^2-2\ cos(g_{c_1})+1)(z^2-2\ cos(g_{c_2})+1)...(z^2-2\ cos(g_{c_{\frac{n}{2}}})+1)}$

Table 4.6: *Loop gain of odd CRFF $\Sigma\Delta$ modulators.*

n^{th} order odd CRFF		
DT	$G_d(z)$	$\frac{\alpha_{d_{n-1}} z^{n-1}+\alpha_{d_{n-2}} z^{n-2}+\cdots+\alpha_{d_1} z+\alpha_{d_0}}{(z-1)(z^2-(2-g_{d_1}{}^2)+1)(z^2-(2-g_{d_2}{}^2)z+1)...(z^2-(2-g_{d_{\frac{n-1}{2}}}{}^2)z+1)}$
CT	$G_c(s)$	$\frac{\alpha_{c_{n-1}} z^{n-1}+\alpha_{c_{n-2}} z^{n-2}+\cdots+\alpha_{c_1} z+\alpha_{c_0}}{(z-1)(z^2-2\ cos(g_{c_1})+1)(z^2-2\ cos(g_{c_2})+1)...(z^2-2\ cos(g_{c_{\frac{n-1}{2}}})+1)}$

4.1, 4.2 and 4.3 respectively. Using these loop filter relations, we can calculate general expressions for the loop gain for each topology. DT loop gain calulations are straightforward. The modified-z-transform-based technique, described in sections 4.3, is used to get the CT loop gain. The DT and CT loop gains of the CIFF, even CRFF and odd CRFF topology are listed in tables 4.4, 4.5 and 4.6 respectively. Comparing the CIFF loop gain denominators of table 4.4, we find that the DT denominator coefficients $\beta_{d_n}, \beta_{d_{n-1}}, \ldots, \beta_{d_1}, \beta_{d_0}$ and the CT denominator coefficients $\beta_{c_n}, \beta_{c_{n-1}}, \ldots, \beta_{c_1}, \beta_{c_0}$ are identical. In fact, these coefficients are independent from the loop filter coefficients $b_n, b_{n-1}, \ldots, b_2, b_1$ and $a_n, a_{n-1}, \ldots, a_2, a_1$. They are only dependent on the loop filter order, n. For the CRFF topologies, the CT resonator feedback coefficient, g_{c_i}, can be described as a function of its DT counterpart, g_{d_i}, using the following relation

$$g_{c_i} = cos^{-1}(1 - g_{d_i}{}^2) \tag{4.26}$$

Comparing the numerators of the DT and CT loop gains described in tables 4.1, 4.2 and 4.3, we find that the DT numerator coefficients $\alpha_{d_{n-1}}, \alpha_{d_{n-2}}, \ldots, \alpha_{d_1}, \alpha_{d_0}$ are function of the DT loop filter coefficients $b_n, b_{n-1}, \ldots, b_2, b_1$ and that the CT numerator coefficients $\alpha_{c_{n-1}}, \alpha_{c_{n-2}}, \ldots, \alpha_{c_1}, \alpha_{c_0}$ are function of the CT loop filter coefficients $a_n, a_{n-1}, \ldots, a_2, a_1$ and the characteristics of the DAC feedback signals t_d and τ. For the CT modulator to be equivalent to the DT modulator, the following set of equation must be satisfied:

$$\begin{aligned}
\alpha_{c_{n-1}}(a_1, a_2, \ldots, a_{n-1}, a_n, t_d, \tau) &= \alpha_{d_{n-1}}(b1, b2, \ldots, b_{n-1}, b_n) \\
\alpha_{c_{n-2}}(a_1, a_2, \ldots, a_{n-1}, a_n, t_d, \tau) &= \alpha_{d_{n-2}}(b1, b2, \ldots, b_{n-1}, b_n) \\
&\vdots \\
\alpha_{c_1}(a_1, a_2, \ldots, a_{n-1}, a_n, t_d, \tau) &= \alpha_{d_1}(b1, b2, \ldots, b_{n-1}, b_n) \\
\alpha_{c_0}(a_1, a_2, \ldots, a_{n-1}, a_n, t_d, \tau) &= \alpha_{d_0}(b1, b2, \ldots, b_{n-1}, b_n)
\end{aligned} \tag{4.27}$$

Equation(4.27), can be written in the following form:

$$\begin{pmatrix} c_{11}(t_d,\tau) & c_{12}(t_d,\tau) & \ldots & c_{1n}(t_d,\tau) \\ c_{21}(t_d,\tau) & c_{22}(t_d,\tau) & \ldots & c_{2n}(t_d,\tau) \\ \vdots & \vdots & \ddots & \vdots \\ c_{n1}(t_d,\tau) & c_{n2}(t_d,\tau) & \ldots & c_{nn}(t_d,\tau) \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \\ \vdots \\ a_n \end{pmatrix} = \begin{pmatrix} d_{11} & d_{12} & \ldots & d_{1n} \\ d_{21} & d_{22} & \ldots & d_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ d_{n1} & d_{n2} & \ldots & d_{nn} \end{pmatrix} \begin{pmatrix} b_1 \\ b_2 \\ \vdots \\ b_n \end{pmatrix}$$

which can be expressed as

$$C\ A = D\ B \tag{4.28}$$

In order to get the CT vector coefficients A, we need the inverse of matrix C,

$$A = C^{-1}\ D\ B \tag{4.29}$$

The complete design procedure for RZ CT $\Sigma\Delta$ starting from a DT $\Sigma\Delta$, using the modified-z-transform technique, is summarized in Figure 4.14. This design procedure has been implemented using the symbolic mathematical tool *MAPLE* [Wat97]. This mathematical tool has mainly been used to calculate the residues of equation (4.8) and the matrix inversion of equation (4.29). The advantage of using a symbolic tool is that the resulting CT coefficients $(a_1, \ldots, a_n)$ are expressed in function of the DT coefficients $(b_1, \ldots, b_n)$ and the feedback signal characteristics $(t_d, \tau, \ldots)$. This means that for a given $\Sigma\Delta$ topology and order, the design procedure of Figure 4.14 is performed only once. Simple substitutions are then required to get the numerical values of the CT coefficients.

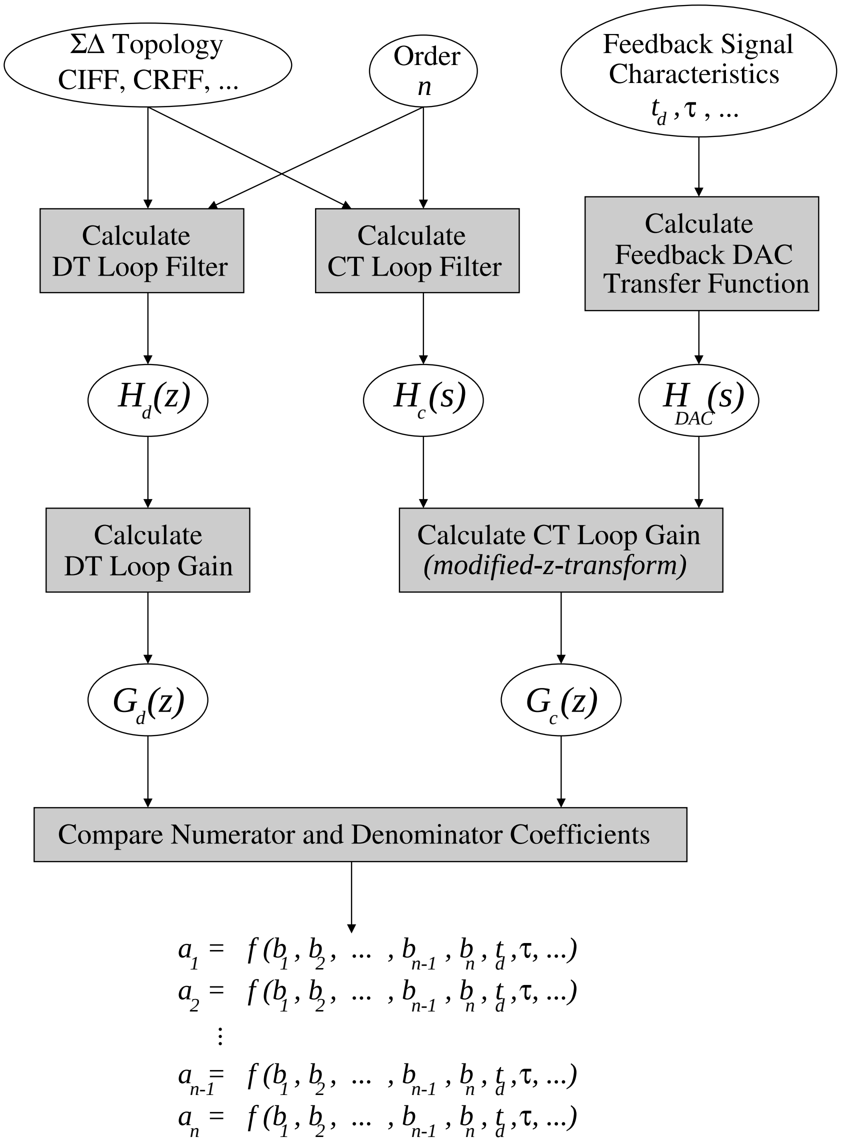

Figure 4.14: *Design Procedure to find CT ΣΔ coefficients* $(a_1, a_2, \ldots, a_{n-1}, a_n)$ *in function of DT ΣΔ coefficients* $(b_1, b_2, \ldots, b_{n-1}, b_n)$ *and the feedback signal characteristics* $(t_d, \tau, \ldots)$.

4.6 Design Examples

The CT ΣΔ design technique, described in this chapter, is used to design three different CT ΣΔ modulators:

- The third order CIFF shown in Figure 4.15.
- The fifth order CRFF shown in Figure 4.17.

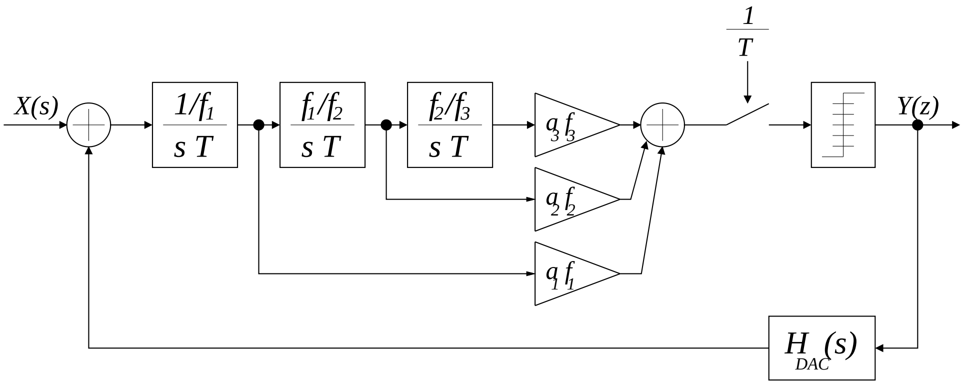

Figure 4.15: *3rd order CIFF*.

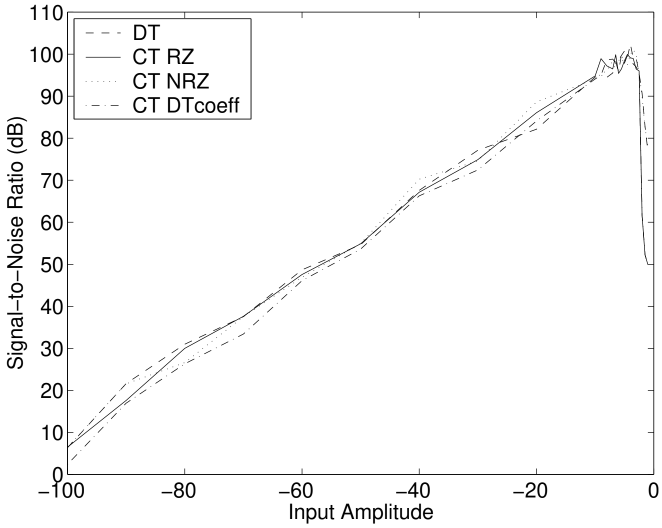

Figure 4.16: 3^{rd} *order CIFF (OSR=128)*.

- The sixth order bandpass CRFF shown in Figure 4.19.

The DT $\Sigma\Delta$ coefficients have been obtained using Richard Schreier's $\Sigma\Delta$ Toolbox [Schreier99] which uses the design method described in [Schreier93]. Using the design procedure illustrated in Fig.4.14, the CT $\Sigma\Delta$ coefficients were obtained for both RZ and NRZ rectangular feedback signals. The RZ feedback signal had $t_d = \frac{T}{4}$ and $\tau = \frac{3T}{4}$.
The coefficients of the DT $\Sigma\Delta$ as well those of the resulting CT $\Sigma\Delta$ are scaled in order to obtain maximum swing at the output of the each integrator. These coefficients are listed in tables A.1, A.2 and A.3 of Appendix A.

In order to study the behavior of the resulting CT $\Sigma\Delta$ modulator, several MATLAB/SIMULINK simulations have been performed to compare it with its DT counterpart.

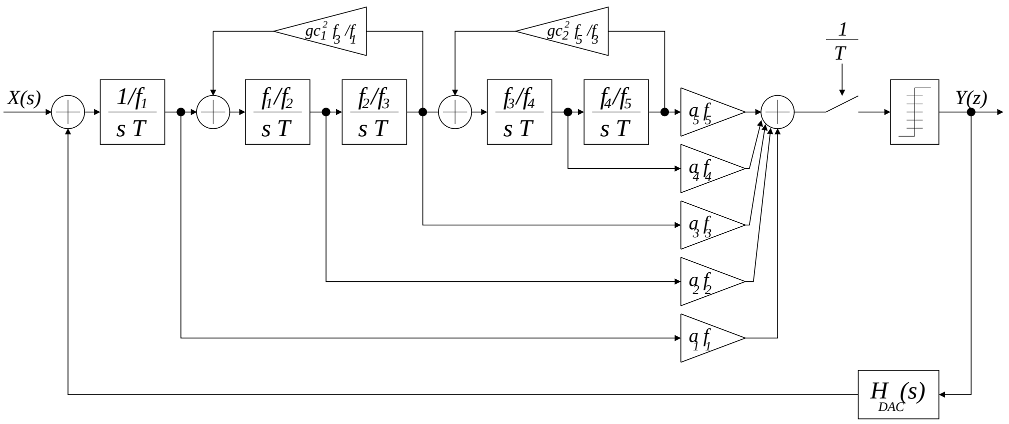

Figure 4.17: 5^{th} *order CRFF (OSR=64)*.

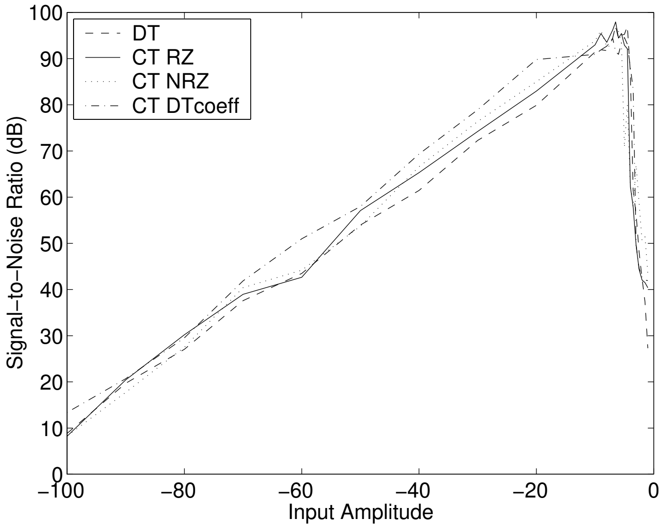

Figure 4.18: 5^{th} *order lowpass CRFF (OSR=64)*.

Figures 4.16, 4.18 and 4.20 show the Signal-to-Noise Ratio (SNR) resulting from the simulation of the DT modulator (DT), the RZ CT modulator (CT RZ), the NRZ CT modulator (CT NRZ), and a RZ CT modulator simulated with the DT coefficients (CT DTcoeff).
We can see in Figures 4.16 and 4.18 that in the case of the 5^{th} order lowpass CRFF, there is very little difference between the performance of the DT modulator (DT), the calculated CT modulators (CT RZ and CT NRZ), and the CT modulator using the DT coefficients (CT DTcoeff).

On the other hand, it is clear from Figure 4.20, that in the case of the bandpass $\Sigma\Delta$ modulators, the CT modulator with DT coefficients has a very poor performance. Only the CT $\Sigma\Delta$ modulators using the coefficients calculated using the DT-to-CT transformation method are equivalent to the original DT $\Sigma\Delta$ modulator.

Figure 4.21 shows the power spectral density of the 6^{th} order $\Sigma\Delta$ of the calculated CT modulator and the CT modulator with the DT coefficients. It is obvious that the center frequency of the CT DTcoeff modulator is shifted from the required center frequency $\frac{f_s}{4}$.

4.7 Conclusion

A systematic DT-to-CT transformation method to design CT $\Sigma\Delta$ modulators has been presented. The method is general and can be used for rectangular and non-rectangular feedback signals with or without RZ. Implementing this method in a symbolic mathematical tool, has permitted us to design high-order lowpass and bandpass $\Sigma\Delta$ modulators with different topologies. It has been found that DT-to-CT transformation is particularly important in bandpass modulators.

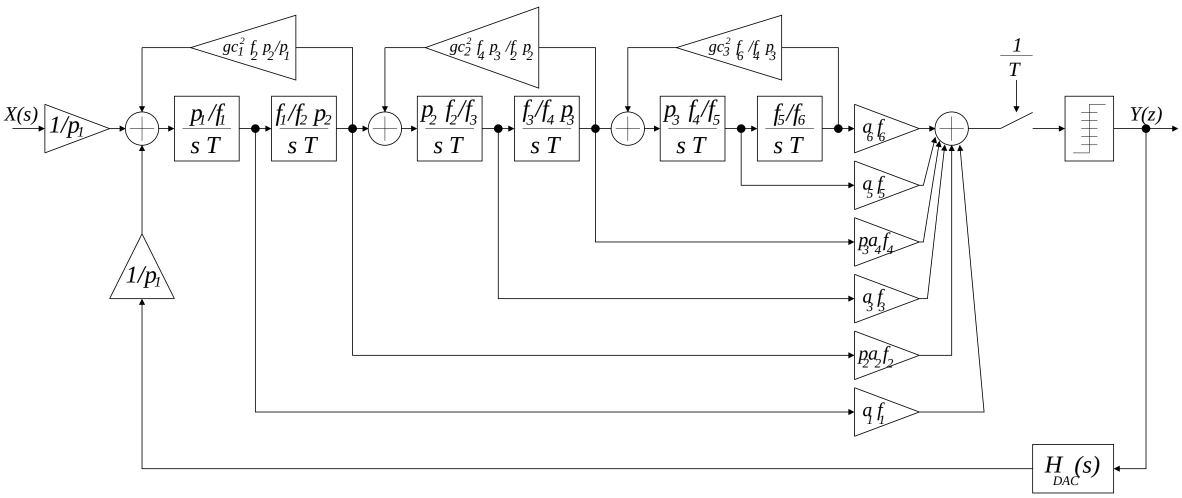

Figure 4.19: 6^{th} *order CRFF*.

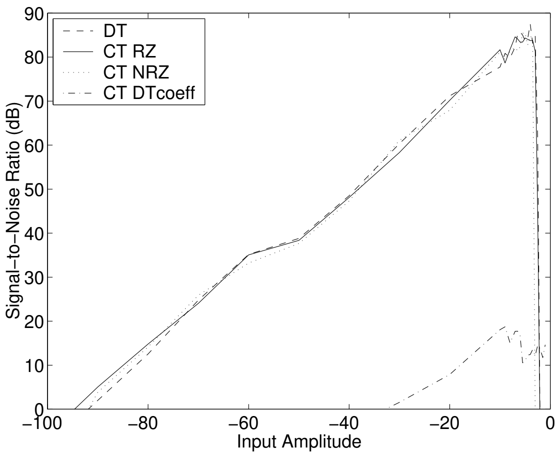

Figure 4.20: 6^{th} *order bandpass CRFF (OSR=64)*.

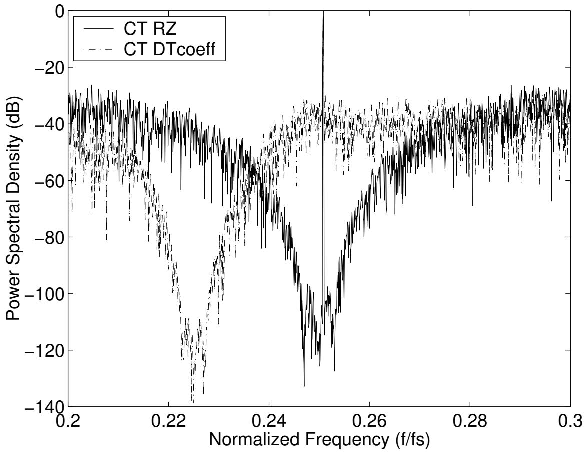

Figure 4.21: 6^{th} *order bandpass CRFF (input signal=-10dB, 16384 pts FFT)*.

Chapter 5

Low-Power Design of Continuous-Time Current-Mode Integrators

5.1 Introduction

In this chapter we present the current-mode continuous-time integrator used for the implementation of the continuous-time $\Sigma\Delta$ modulator.

First we start, in section 5.2, by explaining how current-mirrors are used to realize continuous-time integrators. Then a method to maximize the modulation index of cascode current-mirrors is presented in section 5.3.

In section 5.4 we show the frequency response requirements of continuous-time integrators for $\Sigma\Delta$ modulators. The different design parameters affecting the signal-to-thermal-noise power are discussed in section 5.5.

Finally, harmonic distortion due to transconductance variation is discussed in section 5.6.

5.2 Continuous-Time Current-Mode Integrator

Continuous-time current-mode integrators are based on the current-mirror circuit shown in Figure 5.1. Neglecting output conductances and parasitic capacitances and assuming identical transistors, we can derive the transfer function of the current-mirror circuit from the small-signal equivalent circuit,

$$H_{mir}(s) = \frac{i_{out}(s)}{i_{in}(s)} = \frac{-\frac{g_{m_{11}}}{C}}{s + \frac{g_{m_1}}{C}} \tag{5.1}$$

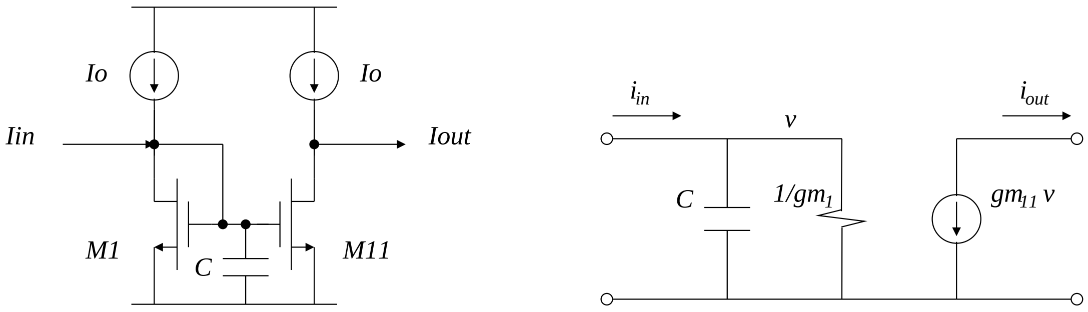

Figure 5.1: *The simple current-mirror and its small-signal equivalent circuit.*

The differential current-mode integrator, shown in Figure 5.2, has been proposed in [Zele96] and [Smith96]. The circuit is composed of two cross-coupled current-mirrors and two output stages. In order to analyze this differential current-mode integrator, we will use the mathematical model described in Figure 5.3, where $H_1(s)$ and $H_2(s)$ are the transfer functions of the two cross-coupled current-mirrors. Assuming that the aspect ratio of all mirror transistors is equal to 1, the two output stages are omitted from the representation shown in Figure 5.3. The differential output current can then be described by

$$i_{outp}(s) - i_{outn}(s) = \left[\frac{H_1(s)H_2(s) - H_1(s)}{1 - H_1(s)H_2(s)}\right] i_{inp}(s) - \left[\frac{H_1(s)H_2(s) - H_2(s)}{1 - H_1(s)H_2(s)}\right] i_{inn}(s) \tag{5.2}$$

Assuming $i_{in}(s) = i_{inp}(s) = -i_{inn}(s)$, the input-output relation is found to be

$$\frac{i_{outp}(s) - i_{outn}(s)}{i_{in}(s)} = \frac{2H_1(s)H_2(s) - H_1(s) - H_2(s)}{1 - H_1(s)H_2(s)} \tag{5.3}$$

by substitution from equation (5.1) into equation (5.3), we get

$$\frac{i_{outp}(s) - i_{outn}(s)}{i_{in}(s)} = \frac{s\frac{g_{m_{11}} + g_{m_{22}}}{C} + \frac{\left(g_{m_1}g_{m_{22}} + g_{m_2}g_{m_{11}} + 2g_{m_{11}}g_{m_{22}}\right)}{C^2}}{s^2 + s\frac{\left(g_{m_1} + g_{m_2}\right)}{C} + \frac{\left(g_{m_1}g_{m_2} - g_{m_{11}}g_{m_{22}}\right)}{C^2}} \tag{5.4}$$

In the case of all mirror transistors having the same transconductance g_m, the transfer function of the differential circuit shown in Figure 5.2 becomes

$$\frac{i_{outp}(s) - i_{outn}(s)}{i_{inp}(s) - i_{inn}(s)} = \frac{g_m}{s\,C} \tag{5.5}$$

It is obvious from equation (5.4), that this current-mode integrator is sensitive to the g_m matching. Thus, it is important to study the effect of g_m mismatch on the transfer function of the integrator. We also have to identify which transistors should be matched in order to achieve the best performances. Equation 5.4 is plotted in Figure 5.4 for 3 different cases:

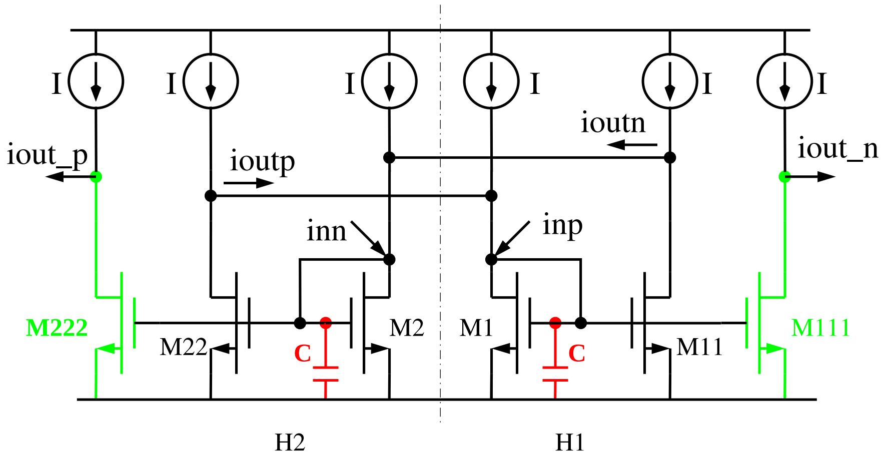

Figure 5.2: *Differential current-mode integrator.*

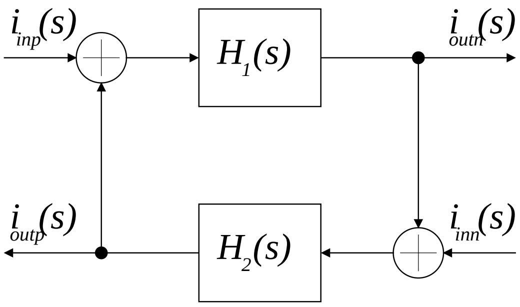

Figure 5.3: *Mathematical model of the current-mode integrator of Figure 5.2.*

- all transistors g_m are identical ($g_{m_1} = g_{m_{11}} = g_{m_2} = g_{m_{22}}$).
- all transistors in the same current-mirror are matched, but there is 1% g_m mismatch between the transistors of different current-mirrors ($g_{m_1} = g_{m_{11}} \neq g_{m_2} = g_{m_{22}}$).
- transistors of the same current-mirror have 1% g_m mismatch ($g_{m_1} \neq g_{m_{11}}$).

From Figure 5.4 we can see that mismatch between transistors of different current-mirrors have very little effect on the frequency response of the integrator. Mismatch between transistors of the same current-mirror has very little effect on the unity gain frequency of the integrator, but has a considerable effect on the DC gain.

In order to improve g_m matching between the different transistors of the integrator, common-centroid layout should be used to realize each mirror transistor pair (M_1, M_{11}) and (M_2, M_{22})

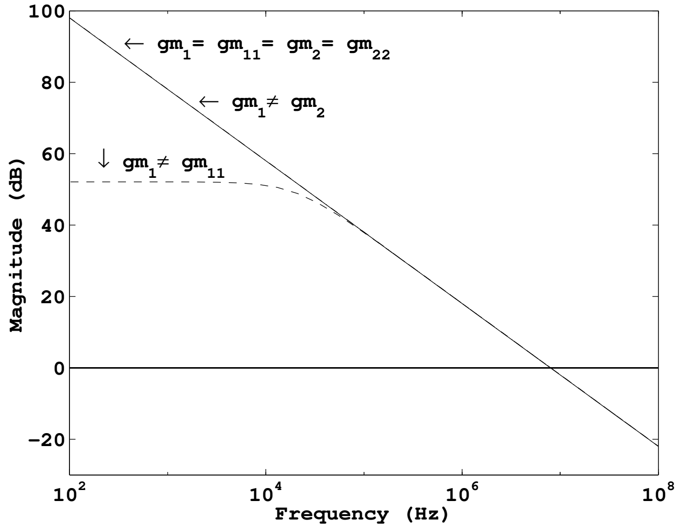

Figure 5.4: *The effect of* 1% g_m *mismatch in mirror transistors on the frequency response of the current-mode integrator described by equation5.4.*

[Maloberti94].

In the derivation of equations 5.4, the output conductance g_{ds} of the mirror transistors has been neglected. If it is taken into account, the differential current-mode integrator will have the following transfer function

$$\frac{i_{outp}(s) - i_{outn}(s)}{i_{inp}(s) - i_{inn}(s)} = \frac{\frac{g_m}{C}}{s + \frac{g_{ds}}{C}} \tag{5.6}$$

The DC gain of the integrator is then determined by the ratio $\frac{g_m}{g_{ds}}$. In order to have a sufficiently low output conductance, a cascode current-mirror configuration is used. In Figure 5.5 we illustrate the cascode current-mirror-based integrator. In the next section we will present a design method for the high swing cascode current-mirror [Crawley92] shown in Figure 5.6. This method is used to obtain the maximum modulation index $m = \frac{I_{in}}{I_0}$, where I_{in} is the input current and I_0 is the biasing current. In the next section it will be shown, by theoretical analysis and simulations, that the maximum modulation index is obtained for supply voltages significantly lower than the maximum supply voltage of a given technology.

5.3 Cascode Current-Mirror Modulation Index

In this section we will describe a method to bias the cascode current-mirror shown in Figure 5.6. This method gives maximum modulation index m for a given V_{EG1_0} and V_{EG3_0}, the effective

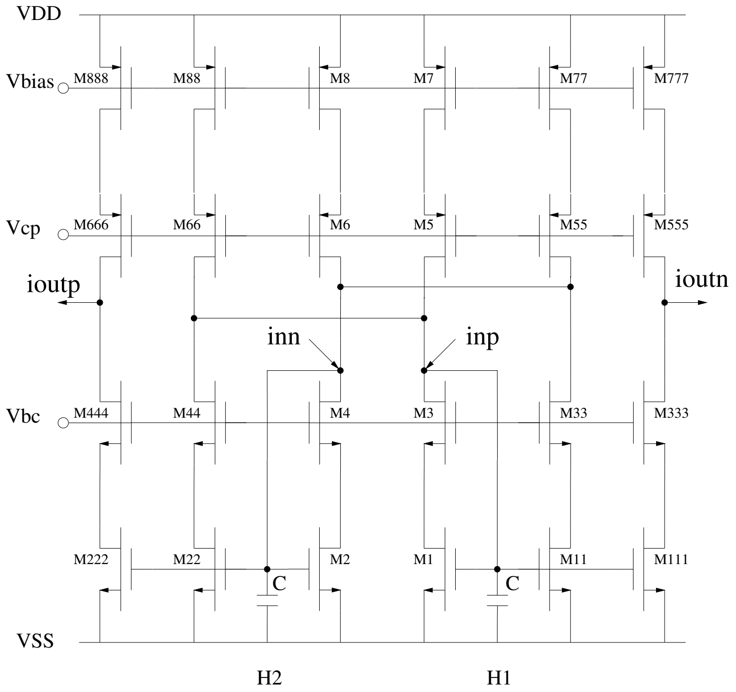

Figure 5.5: *Cascode current-mirror-based integrator.*

gate voltage $(V_{GS} - V_{TH})$ for $I_{in} = 0$, of the mirror transistor M_1, and the cascode transistor M_3 respectively. This method also gives the optimum value for the cascode transistor biasing voltage V_{BC}, in order to obtain maximum modulation index.

Starting from the simple square model of a MOS transistor in the saturation region:

$$I = \frac{\beta}{2}(V_{GS} - V_{TH})^2 \tag{5.7}$$

The effective gate voltage, $V_{EG} = (V_{GS} - V_{TH})$, can be written in function of the modulation index, $m = \frac{I_{in}}{I_0}$, as described in the following:

$$\begin{aligned}
V_{EG} &= \sqrt{\frac{2I}{\beta}} = \sqrt{\frac{2(I_0 \pm I_{in})}{\beta}} \\
V_{EG} &= \sqrt{1 \pm m}\ \sqrt{\frac{2I_0}{\beta}} \\
V_{EG} &= \sqrt{1 \pm m}\ V_{EG_0}
\end{aligned} \tag{5.8}$$

where $0 \leq m \leq 1$.

The condition for the mirror transistor M_1 to be operating in the saturation region:

$$\begin{aligned} V_{DS_1} &\geq V_{GS_1} - V_{TH_1} \\ V_{BC} - V_{GS_3} &\geq V_{GS_1} - V_{TH_1} \\ V_{BC} &\geq V_{EG_1} + V_{EG_3} + V_{TH_3}. \end{aligned} \tag{5.9}$$

Note that this condition must be considered for high input current, i.e. when $V_{EG_1} = \sqrt{1+m}\ V_{EG_0}$. In this case, the input-node voltage rises, consequently V_{GS_1} increases and transistor M_1 could be driven out of the saturation region.

The condition for the cascode transistor M_3 to be operating in the saturation region:

$$\begin{aligned} V_{DS_3} &\geq V_{GS_3} - V_{TH_3} \\ V_{GS_1} - V_{DS_1} &\geq V_{GS_3} - V_{TH_3} \\ V_{GS_1} - V_{BC} + V_{GS_3} &\geq V_{GS_3} - V_{TH_3} \end{aligned}$$

$$V_{BC} \leq V_{EG_1} + V_{TH_1} + V_{TH_3}. \tag{5.10}$$

Note that this condition must be considered for low input current, i.e. when $V_{EG_1} = \sqrt{1-m}\ V_{EG_0}$. In this case, the input-node voltage diminishes, consequently V_{DS_3} decreases and transistor M_3 could be driven out of the saturation region.

By substitution, from equation (5.7) in equation (5.9) and equation (5.10) we get

$$V_{BC_{min}} = \sqrt{1+m}\ (V_{EG_{1_0}} + V_{EG_{3_0}}) + V_{TH_3} \tag{5.11}$$

$$V_{BC_{max}} = \sqrt{1-m}\ V_{EG_{1_0}} + V_{TH_1} + V_{TH_3} \tag{5.12}$$

In order to get maximum modulation index m we equate these two equations. By equating equation (5.11) and equation (5.12), we get

$$\sqrt{1+m}\,(V_{EG_{1_0}} + V_{EG_{3_0}}) - \sqrt{1-m}\,V_{EG_{1_0}} - V_{TH_1} = 0 \tag{5.13}$$

Since $V_{BC} = V_{GS_{3_0}} + V_{DS_{1_0}}$, and by substitution in equation (5.12), we can deduce the value of V_{DS_1}

$$V_{DS_{1_0}} = \sqrt{1-m}\ V_{EG_{1_0}} - V_{EG_{3_0}} + V_{TH_1} \tag{5.14}$$

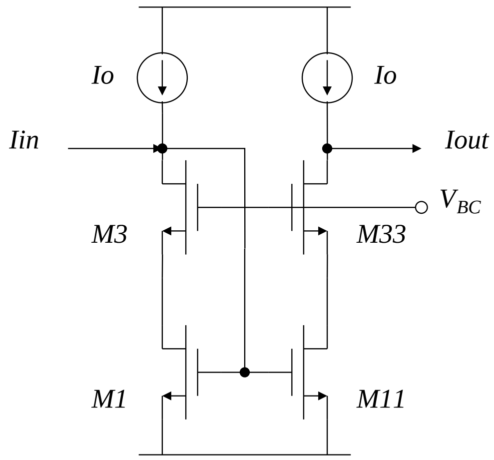

Figure 5.6: *Cascode current-mirror.*

Knowing $V_{DS_{1_0}}$, we can get V_{BS_3}, the Bulk-Substrate voltage of M_3, and then calculate V_{TH_3} from the transistor model equations. From the values of $V_{EG_{3_0}}$ and V_{TH_3} we can easily deduce the cascode biasing voltage V_{BC}.

Using equation (5.13), the modulation index m can be calculated in function of $V_{EG_{1_0}}$ and $V_{EG_{3_0}}$. This is illustrated in Figure 5.7 for $0.6\mu m$ CMOS process, with $V_{TH_1} = 0.83V$ and in Figure 5.8 for $0.25\mu m$ CMOS process, with $V_{TH_1} = 0.566V$. From these figures, we can see that very high values of the modulation index m can be obtained for small values of $V_{EG_{1_0}}$ and $V_{EG_{3_0}}$. This is an interesting result which supports the claims, already made in [Toumazou90] and [Hughes00], that current-mode circuits are adapted to operate at low voltage supply.

With $V_{EG_{1_0}}$ biased to $\frac{1}{2}V_{DD} - V_{TH}$ and $V_{EG_{3_0}}$ fixed to $0.15V$, equation (5.13) is used to calculate the modulation index in function of the supply voltage V_{DD}, for the $0.25\mu m$ process. The result of these calculations, using equation (5.13), are illustrated in Figure 5.9 along with the simulation results performed using the MM9 MOS transistor model [Philips00]. Although equation (5.13) was derived from the simple square model of the MOS transistor, the simulation results of the modulation index, shown in Figure 5.9, are very close to the values predicted by the equation.

In the following sections we will develop relations for the biasing current, I_0, of a $\Sigma\Delta$ integrator. We will see that there exists an optimum supply voltage, V_{DD}, where minimum power consumption is obtained.

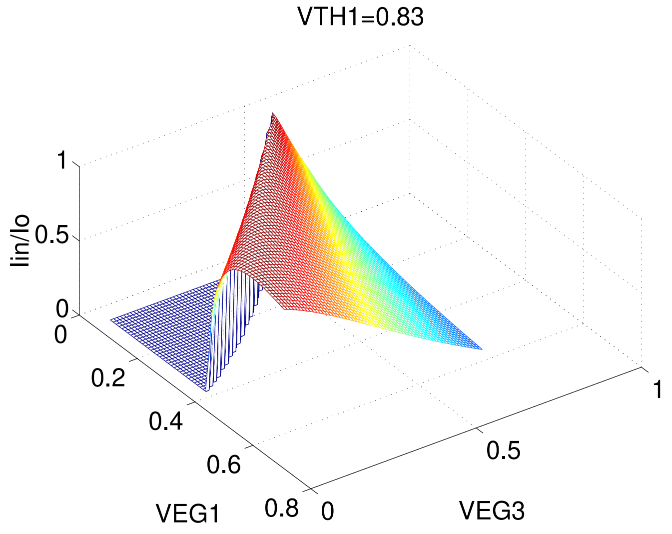

Figure 5.7: *The modulation index, m, in function of V_{EG1_0} and V_{EG3_0} for 0.6μ CMOS process with $V_{TH} = 0.83$, equation (5.13).*

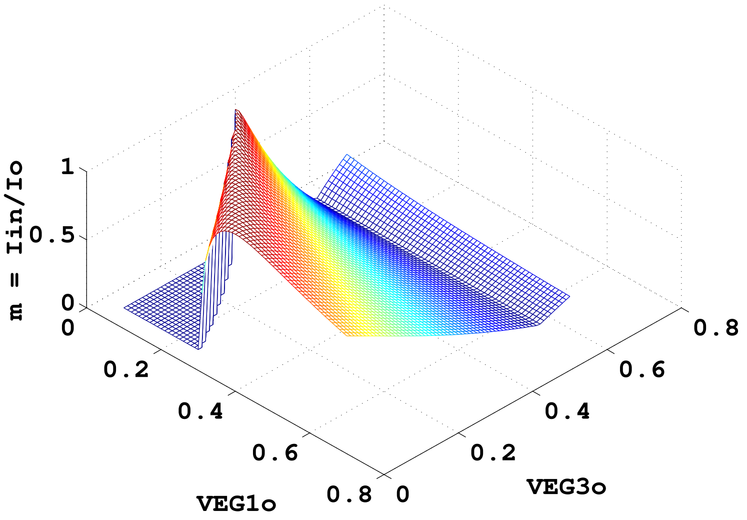

Figure 5.8: *The modulation index, m, in function of V_{EG1_0} and V_{EG3_0} for 0.25μ CMOS process with $V_{TH} = 0.566$, equation (5.13).*

5.4 Continuous-time Integrator for $\Sigma\Delta$ modulators

A differential current-mode n^{th} order continuous-time $\Sigma\Delta$ modulator is shown in Figure 5.10. The transfer function of each integrator in the $\Sigma\Delta$ modulator is determined during the system level

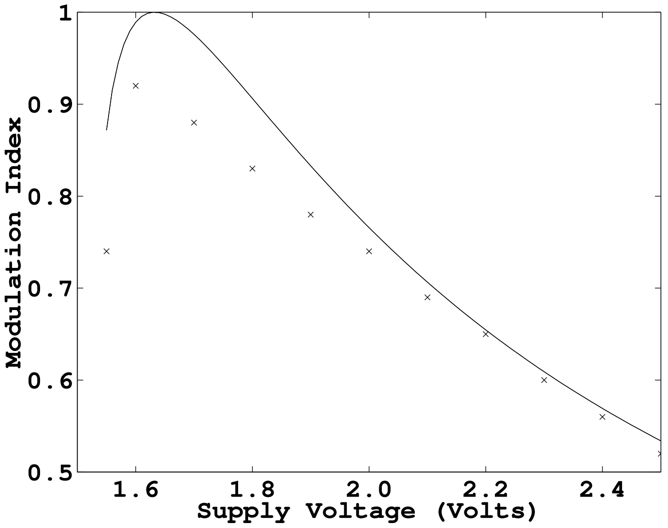

Figure 5.9: *The modulation index m in function of the supply voltage V_{DD}, $V_{EG3_0} = 0.15V$ and $V_{GS1_0} = \frac{V_{DD}}{2}$ (0.25μ CMOS process), (-) Calculated using equation (5.13), (x) measured by simulation.*

design described in chapter 4. This transfer function can be written in the following form

$$H_{system}(s) = \frac{A_{int}}{s\,T} \tag{5.15}$$

where A_{int} is the gain of the integrator and T is the sampling period. The circuit realizing the integrator is a Gm-C circuit whose transfer function can be described by

$$H_{circuit}(s) = \frac{g_m}{s\,C} \tag{5.16}$$

where g_m is the MOS transistor transconductance and C is the integrating capacitance. Comparing (5.15) and (5.16), it is obvious that for proper operation of the modulator the following relation

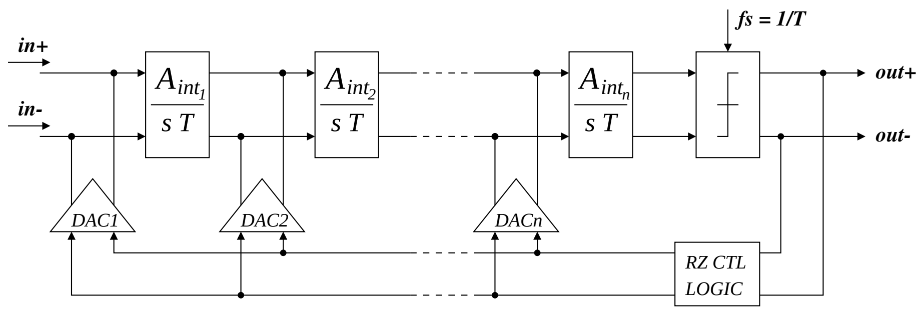

Figure 5.10: *Differential continuous-time ΣΔ modulator.*

must be satisfied:

$$A_{int}\ f_s = \frac{g_m}{C} \tag{5.17}$$

where $f_s = \frac{1}{T}$ is the sampling frequency of the modulator. The transconductance g_m can also be written in the following form

$$g_m = \frac{2\ I_0}{V_{EG}} \tag{5.18}$$

By substitution from equation (5.18) into equation (5.17) we find that

$$A_{int}\ f_s = \frac{2\ I_0}{V_{EG}\ C} \tag{5.19}$$

In order to reduce power consumption and area of the $\Sigma\Delta$ modulator, we would like the biasing current, I_0, and the integrating capacitance, C, to be as small as possible. However, these values must be carefully chosen to satisfy the signal-to-thermal-noise-ratio (SNR_{TH}) requirements of the $\Sigma\Delta$ modulator.

In the following, we will develop a design procedure to find the minimum biasing current, I_0, and integrating capacitance, C, required to achieve a given SNR_{TH}.

5.5 Signal-to-Thermal-Noise Ratio

In this section, we will define the design equations of a current-mirror based integrator for continuous-time $\Sigma\Delta$ modulator. The biasing current and the capacitance of this integrator are chosen to satisfy the thermal noise requirements and the bandwidth specifications of the modulator. It is found that there exists an optimum operating supply voltage for minimum power consumption of the integrator. Two design examples of continuous-time $\Sigma\Delta$ integrators are given, in section 5.5.3, to validate the design procedure.

The power spectral density of thermal noise at the $\Sigma\Delta$ modulator input can be expressed by [Gray93]:

$$S_i = \frac{2}{3}\ g_m\ 4KT\ N_{tr} \tag{5.20}$$

where N_{tr} is the number of transistors adding noise to the signal, K is Boltzman constant and T is the temperature. The input referred noise power is equal to:

$$\overline{i_{in}^2} = \frac{2}{3}\ g_m\ 4KT\ N_{tr}\ BW \tag{5.21}$$

where BW is the bandwidth of the $\Sigma\Delta$ modulator. On the other hand, the power of a sinusoidal input signal can be defined as:

$$\text{Signal Power} = \frac{1}{2}\, A_{\Sigma\Delta}^2\, m^2\, I_0^2 \tag{5.22}$$

where $A_{\Sigma\Delta}$ is the gain of the input signal which gives maximum signal-to-quantization-noise ratio, usually $A_{\Sigma\Delta}$ is equal to 0.5. From equation (5.21) and equation (5.22) we can define the Signal-to-Thermal-Noise Ratio as:

$$SNR_{TH} = \frac{\frac{1}{2}\, A_{\Sigma\Delta}^2\, m^2\, I_0^2}{\frac{2}{3}\, g_m\, 4KT\, N_{tr}\, BW} \tag{5.23}$$

The bandwidth of a $\Sigma\Delta$ modulator can be written in function of the sampling frequency, f_s, and the oversampling ratio, OSR

$$BW = \frac{f_s}{2\, OSR} \tag{5.24}$$

From equation (5.24) and equation (5.19) the bandwith of the continuous-time $\Sigma\Delta$ modulator can be expressed by

$$BW = \frac{I_0}{V_{EG}\, C\, A_{int}\, OSR} \tag{5.25}$$

Assuming that all transistors adding noise to the signal have the same transconductance g_m, and by substitution from equation (5.25) and equation (5.18) into equation (5.23), we get the following expression for the signal-to-thermal-noise ratio

$$SNR_{TH} = \frac{3}{8}\, (A_{\Sigma\Delta}^2\, OSR\, A_{int})\, \frac{m^2\, V_{EG_{1_0}}^2\, C}{N_{tr}\, 4KT} \tag{5.26}$$

From equation (5.26) we can see the different parameters that affect the signal-to-thermal-noise ratio. We can see that SNR_{TH} depends on both system design parameters ($A_{\Sigma\Delta}$, OSR, A_{int}) and circuit design parameters (m, $V_{EG_{1_0}}$, C, N_{tr}).

In the following, we will have a discussion about equation (5.26) and the different design parameters:

System Level Design Parameters:

- Oversampling Ratio OSR:

  Along with the order of the $\Sigma\Delta$ modulator, the oversampling ratio, OSR, is chosen in such a way that the quantization noise is sufficiently low compared to the circuit thermal noise.

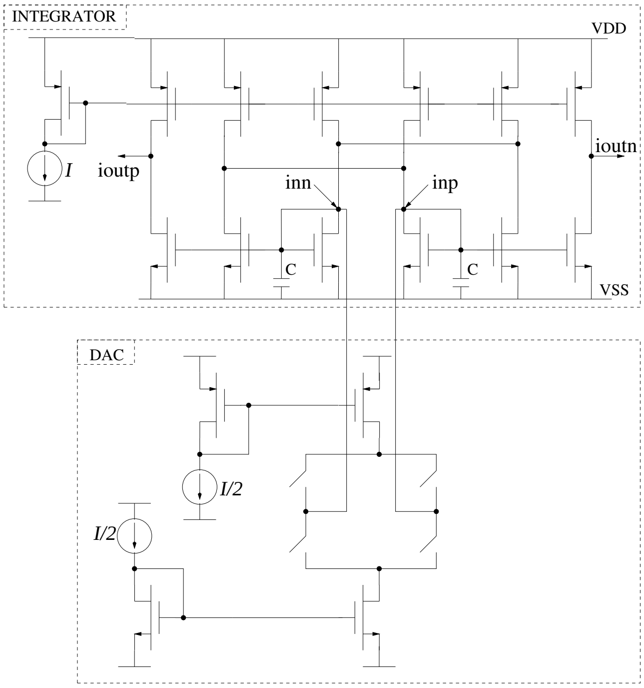

Figure 5.11: *Transistors affecting the signal-to-thermal-noise ratio at the $\Sigma\Delta$ modulator input.*

- $A_{\Sigma\Delta}$:

  $A_{\Sigma\Delta}$ is the gain of the input signal which gives maximum signal-to-quantization-noise ratio. In $\Sigma\Delta$ modulator peak signal-to-noise ratio is usually obtained for a signal input amplitude lower than the maximum allowable input signal. The maximum allowable input signal of the integrator is usually given the notation I_{ref}. The modulation index calculated in section 5.3 determines this amplitude $I_{ref} = m\ I_0$. $A_{\Sigma\Delta}$ is determined by simulation and is usually equal to 0.5.

- A_{int}:

  Although the integrator gain, A_{int}, is also determined during system level design, we will see, in the next sections, that this value can be modified during circuit design. This is due to the considerable impact of the first integrator's gain on the linearity of the $\Sigma\Delta$ modulator. The gain of the other integrators will have to be scaled accordingly in order to keep the modulator transfer function unaltered.

Circuit Level Design Parameters:

- N_{tr}:

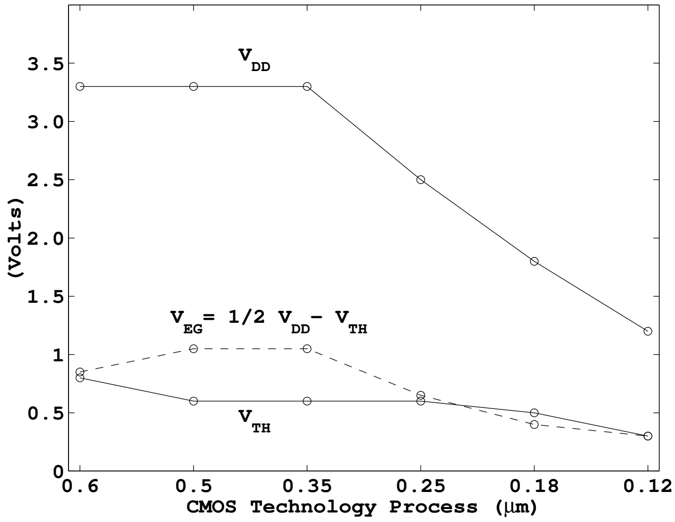

Figure 5.12: *The evolution of the supply voltage V_{DD}, the threshold voltage V_{TH} and the effective gate voltage $V_{EG} = \frac{1}{2}V_{DD} - V_{TH}$ in recent CMOS technologies.*

N_{tr} is the number of transistors adding noise to the signal at the input node. This number is determined by the structure of the integrator, the feedback DAC and their biasing circuits. In Figure 5.11, all transistors contributing noise to the input signal are shown. The cascode transistors have been removed from Figure 5.11 due to their negligible effect on the input referred thermal noise power.

All the transistors ($NMOS$ and $PMOS$) represented in Figure 5.11 have the same effective gate voltage, V_{EG}. The transistors representing the feedback current sources of the DAC and their biasing transistors draw half the biasing current of the integrator. We can then consider that their transconductance is half the transconductance of the integrator transistors. The number of transistors contributing noise to the input signal can then be estimated by

$$N_{tr} = (7\ PMOS + 6\ NMOS)_{int} + \frac{1}{2}(2\ PMOS + 2\ NMOS)_{dac} = 15 \tag{5.27}$$

- The effective gate voltage V_{EG}:

  From equation (5.26) we can see that increasing V_{EG} improves the signal-to-noise ratio. The effective gate voltage V_{EG} is dependent on the supply voltage V_{DD}. In this design all transistors depicted in Figure 5.11 are biased such that their effective gate voltage $V_{EG} = \frac{1}{2}V_{DD} - V_{TH}$. Due to the continuously decreasing supply voltages of the new CMOS technologies, it is expected that the effective gate voltage will decrease in future technologies.

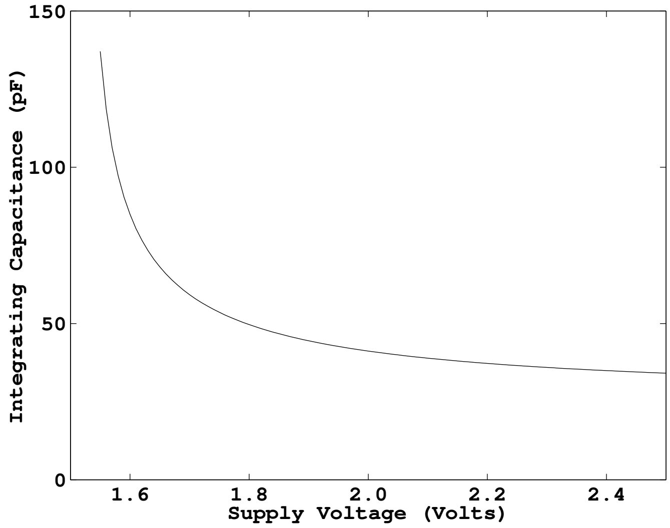

Figure 5.13: *The integrating Capacitance, C, in function of the supply voltage V_{DD}, equation (5.28), $V_{EG_{3_0}} = 0.15V$ and $V_{EG_{1_0}} = \frac{1}{2}V_{DD} - V_{TH}$.*

Figure 5.12 shows the evolution of the effective gate voltage in recent CMOS technologies.

- The modulation index, m:
  Maximizing the modulation index, m, can significantly increase the signal-to-noise ratio. Calculations and simulations of the modulation index of cascode current-mirror has been presented in section 5.3. It has been shown that by proper biasing, modulation index close to the maximum, 1, can be obtained even for low voltage supply.

- The Integrating Capacitance, C:
  The integrating capacitance, C, can be increased to compensate for any reduction in the effective gate voltage due to the low supply voltage of recent and future technologies.

The effect of reducing the supply voltage,V_{DD}, on the integrating capacitance, C, and the biasing current, I_0, is studied in the following.

5.5.1 Integrating Capacitance

Equation (5.26) can be written in the following form

$$C = \frac{8}{3} \frac{SNR_{TH}}{A_{\Sigma\Delta}^2 \; OSR \; A_{int}} \frac{N_{tr} \; 4KT}{m^2 \; V_{EG_{1_0}}^2} \tag{5.28}$$

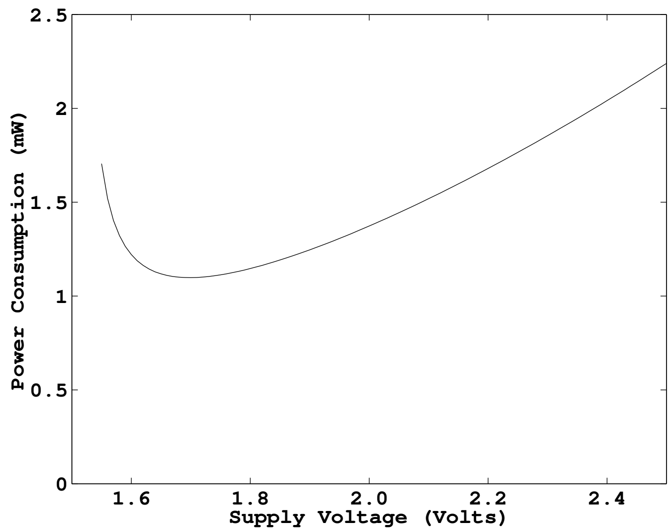

Figure 5.14: *The power consumption of the integrator,* $P = 6\ I_0\ V_{DD}$*, in function of the supply voltage* V_{DD}*, equation (5.29),* $V_{EG_{3_0}} = 0.15V$ *and* $V_{EG_{1_0}} = \frac{1}{2}V_{DD} - V_{TH}$.

Using equation (5.28), we can calculate the minimum integrating capacitance, C, necessary to achieve a required signal-to-thermal noise ratio SNR_{TH}. For the second order $\Sigma\Delta$ modulator specifications listed in table 5.1, we have calculated the integrating capacitance variation with the supply voltage in $0.25\mu m$ technology with a maximum supply voltage of $2.5V$. The results of these calculations are shown in Figure 5.13. We can see that reducing the supply voltage significantly increases the integrating capacitance. This is due to the fact that, as can be see from equation (5.28), the integrating capacitance, C, is inversely proportional to the square of the effective gate voltage V_{EG}.

Table 5.1: *Specifications of the* 2^{nd} *order* $\Sigma\Delta$ *modulator.*

SNR_{TH}	BW	OSR	f_s	A_{int}	$A_{\Sigma\Delta}$
80 dB	100 kHz	128	25.6 MHz	0.5	0.5

5.5.2 Biasing Current

By substitution, from equation (5.18) into equation (5.23), we get the following relation for the biasing current:

$$I_0 = \frac{8}{3} \frac{SNR_{TH}\ BW}{A_{\Sigma\Delta}^2} \frac{N_{tr}\ 4kT}{m^2\ V_{EG_{1_0}}} \tag{5.29}$$

Using equation (5.28), we can calculate the minimum integrating capacitance, C, necessary to achieve a required signal-to-thermal noise ratio SNR_{TH}. For the second order $\Sigma\Delta$ modulator specifications listed in table 5.1, we have calculated the power consumption variation with the supply voltage. From Figure 5.14, we can see that there exists an optimum supply voltage where power consumption is minimum. This is the same supply voltage where maximum modulation index was obtained, Figure 5.9.

In this section, we have developed relations for the integrating capacitance, C, and the biasing current, I_0, in function of the modulation index and the effective gate voltage, $V_{EG_{1_0}}$, of the mirror transistor. In the next section, we will use these equations to design two integrators with different supply voltages.

5.5.3 Design Examples

In order to verify the performances predicted by equations (5.13), (5.28) and (5.29) developed in the previous section, we will design two second-order continuous-time $\Sigma\Delta$ modulators. The two modulators have the same specifications, described in table 5.1, but are operating at different supply voltages. The two values chosen for the supply voltage are $V_{DD} = 1.7$V and $V_{DD} = 2.5$V. The first is the supply voltage at which minimum power consumption was obtained, Figure 5.14, and the latter is the maximum supply voltage for the available $0.25\mu m$ process.

The integrator circuit characteristics of each modulator are as described in table 5.2. As predicted in the previous sections, biasing current and power consumption are lower in the low-voltage design than in the maximum supply voltage design. From table 5.2, we can see that the biasing current has been reduced by 12% and that the power consumption of the 1.7V design is 40% lower than the 2.5V design. This is mainly due to the high modulation index achieved in the 1.7V design. On the other hand, the integrating capacitance of the low-voltage design is 56% higher than the maximum power supply voltage design. Note however, that the values of the integrating capacitance are lower than those predicted by equation (5.28) in Figure 5.13. That is

Table 5.2: *Integrators circuit characteristics (0.25 μm CMOS process).*

	Design I	Design II
V_{DD}	1.7 V	2.5 V
V_{EG1_0}	0.34 V	0.69 V
V_{EG3_0}	0.15 V	0.15 V
m	0.87	0.53
C	27 pF	12 pF
I_0	133 μA	150 μA
Power Consumption	1.36 mW	2.25 mW

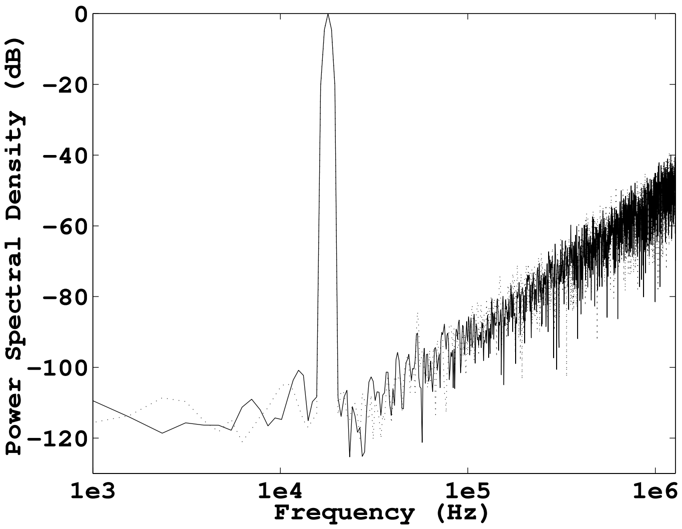

Figure 5.15: *The power spectral density of a second order $\Sigma\Delta$ modulator with ideal models for all elements except the integrators, (-) design I ($1.7V$), (:) design II ($2.5V$), (input signal = -6 dB, 32768 pts FFT).*

because the parasitic capacitances have been taken into account and substracted from the values of Figure 5.13.

The second order $\Sigma\Delta$ modulator was simulated using ideal models for all elements except the integrators. The power spectral density of the output from the 1.7V design is identical to the power spectral density of the output from the 2.5V design. Both power spectral densities are shown in Figure 5.15.

5.6 Harmonic Distortion

In this section, we discuss g_m non-linearity in current-mode continuous-time $\Sigma\Delta$ modulators.

5.6.1 Gm Variation

The main source of harmonic distortion in this current-mode integrator, shown in Figure 5.2, is the variation of the transconductance $g_{m_{11}}$ with the input current.

Starting from the simple square model of a MOS transistor in the saturation region, equation (5.7), the transconductance, g_m, can be expressed in the following form:

$$g_m = \sqrt{2\,\beta\,I}. \tag{5.30}$$

The current I_{11} flowing in transistor M_{11}, Figure 5.2, can be defined as:

$$I_{11} = I_0 + i_{out} \tag{5.31}$$

where I_0 is the biasing current and i_{out} is the output current of the integrator. By substitution from equation (5.31) into equation (5.30), we find that:

$$g_{m_{11}} = g_{m_0}\sqrt{1 + \frac{i_{out}}{I_0}} \tag{5.32}$$

where g_{m_0} is defined as the transistor transconductance for zero input signal. Assuming, for simplicity, that the output current of the current-mode integrator can be described by

$$i_{out}(t) = \frac{g_{m_0}}{C}\int_0^t i_{in}(t)\,dt \tag{5.33}$$

where the mirror transistor transconductance is assumed to be constant. By substitution, from equation (5.33) into equation (5.32), we get:

$$g_{m_{11}}(t) = g_{m_0}\sqrt{1 + \frac{g_{m_0}}{I_0\,C}\int_0^t i_{in}(t)\,dt} \tag{5.34}$$

By substitution, from equation (5.18) into equation (5.34), we get:

$$g_{m_{11}}(t) = g_{m_0}\sqrt{1 + \frac{2}{V_{EG}\,C}\int_0^t i_{in}(t)\,dt} \tag{5.35}$$

From equation (5.35), it is obvious that the non-linear term can only be reduced by increasing the effective gate voltage and the integrating capacitance. As we have seen in the previous section and from Figure 5.12, the effective gate voltage is small in recent technologies and will most likely get smaller in future technologies. Consequently, the only parameter that can be modified to improve the transconductance linearity, is the integrating capacitance C. On the other hand, as we have seen in section 5.5, we know that for proper operation of the continuous-time $\Sigma\Delta$ modulator, equation (5.19) must be satisfied. This means that any increase in the capacitance should be compensated by the same increase in the biasing current in order to keep the same $\frac{g_m}{C}$ ratio. Another alternative would be to compensate any increase in the integrating capacitance, C, by decreasing the integrator gain, A_{int}. This would, of course, require scaling all the $\Sigma\Delta$ integrators gains and feedback coefficients of in order to keep the transfer function unchanged.

In a low power design, it is preferable to decrease the integrator gain, A_{int}, than to increase the biasing current I_0.

5.6.2 Design Examples

The integrators gains and feedback DAC coefficients of two third order continuous-time $\Sigma\Delta$ modulators, $\Sigma\Delta_1$ and $\Sigma\Delta_2$, are listed in table 5.3. These modulators result from a discrete-time to continuous-time transformation method described in chapter 4. The modulator architecture is shown in Figure 5.16. Both modulators have the same noise transfer function. $\Sigma\Delta_1$ is scaled for low distortion according to the value of A_{int_1}. $\Sigma\Delta_2$ is scaled for maximum signal swing at the output of the integrators.

The circuits of the integrators have been designed in 0.18 μm technology and then used with ideal DACs and comparator models to simulate the complete $\Sigma\Delta$ modulators. The simulation results are shown in Figure 5.17, where we can see that the third harmonic of $\Sigma\Delta_1$ is significantly lower than that of $\Sigma\Delta_2$. Since the integrator structure is fully differential, even order harmonics are highly attenuated.

In Table 5.4, we list the different circuit characteristics of the first integrator in $\Sigma\Delta_1$ and $\Sigma\Delta_2$. Note that the biasing current is kept constant and only the integrating capacitance varies with the integrator gain A_{int_1}.

This way we can achieve low-distortion at low power consumption. It is obvious, that the major drawback of this design technique is the large surface area of the $\Sigma\Delta$ modulator.

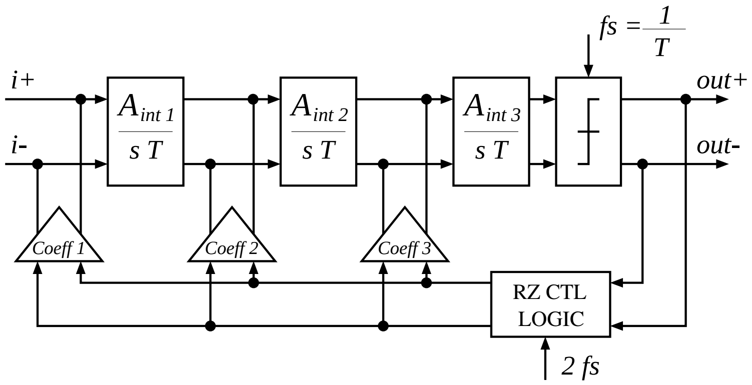

Figure 5.16: *Third order differential continuous-time $\Sigma\Delta$ modulator.*

Table 5.3: *Integrators gains and feedback DAC coefficients.*

	A_{int_1}	A_{int_2}	A_{int_3}	Coeff_1	Coeff_2	Coeff_3
$\Sigma\Delta_1$	0.03	0.50	2.00	0.50	0.10	0.11
$\Sigma\Delta_2$	0.18	0.38	2.00	0.50	0.54	0.45

Mismatch

Note that in the simulation results shown in Figure 5.17, the transistors were perfectly matched. Introducing mismatch into the simulation was done by adding an ideal current source in parallel with transistor M_1, Figure 5.5. The value of this current source is 1% of the current flowing in M_1. In Figure 5.18, we show the difference between a perfectly matched circuit and a circuit with 1% mismatch. We can notice the slight rise of the second harmonic and the presence of an offset component.

5.7 Conclusion

In this chapter we have presented a design method for the cascode current-mirror. It has been shown that by properly choosing the effective gate voltages of the cascode current-mirror transistors, very high modulation index can be achieved at low-voltage supply.

When used in a $\Sigma\Delta$ modulator, the optimum supply voltage of the current-mode integrator, where power consumption is minimum, is significantly lower than the maximum supply voltage.

Table 5.4: *First integrator circuit characteristics for $\Sigma\Delta_1$ and $\Sigma\Delta_2$ (0.18 μm CMOS process).*

	$\Sigma\Delta_2$	$\Sigma\Delta_1$
V_{DD}	1.8 V	1.8 V
V_{EG1_0}	0.4 V	0.4 V
V_{EG3_0}	0.15 V	0.15 V
m	0.7	0.7
A_{int_1}	0.18	0.03
C	138 pF	794 pF
I_0	150μA	150μA
Power Consumption	1.62 mW	1.62 mW

This makes current-mode circuits particularly well-suited to low-voltage operation.

It is shown that increasing the integrating capacitance can significantly reduce harmonic distortion. due to g_m variation. It is found that it is possible to obtain low-distortion continuous-time $\Sigma\Delta$ modulators at low-power consumption, this is done by compensating any increase in the integrating capacitance by decreasing the first integrator's gain and scaling the rest of $\Sigma\Delta$ coefficients accordingly.

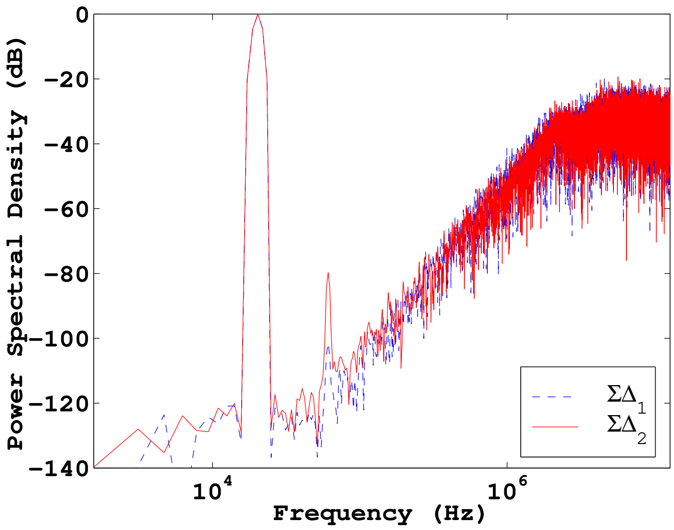

Figure 5.17: *The third harmonic of* $\Sigma\Delta_1$ *is* 20*dB lower than that of* $\Sigma\Delta_2$*, (input signal = -6 dB, 16384 pts FFT).*

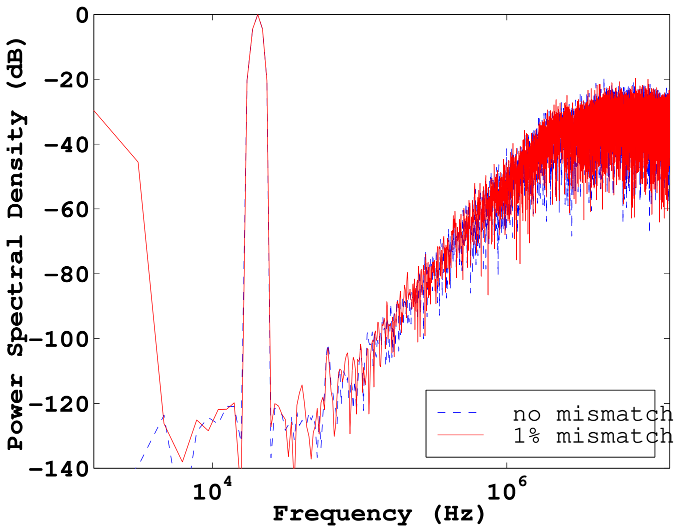

Figure 5.18: *Mismatch slightly increases the second harmonic and introduces an offset component, (input signal = -6 dB, 16384 pts FFT).*

Chapter 6

Continuous-Time Return-to-Zero Feedback DAC

6.1 Introduction

This chapter discusses the non-idealities of the DAC feedback signal and their effect on the performance of continuous-time $\Sigma\Delta$ modulators.
The sensitivity of continuous-time $\Sigma\Delta$ modulators with NRZ feedback to loop delay and waveform asymmetry is presented in section 6.2.
In section 6.3, clock jitter is analyzed for different shapes of the feedback signal.
Finally, in section 6.4, we present a RZ feedback DAC circuit with reduced switching errors. 6.4

6.2 Non-Return-to-Zero Feedback DAC

In the following, we will discuss the two main sources of errors in a continuous-time $\Sigma\Delta$ modulator with Non-Return-to-Zero (NRZ) feedback signal.

6.2.1 Loop Delay

Any extra delay in the modulator loop modifies the response of the continuous-time modulator [Shoaei95] [Benabes97]. The excess loop delay is mainly due to the comparator response-time and the latch propagation delay. It has been shown in [Cherry99] and [Maurino00], that excess loop delay can have a significant degrading effect on the SNR and may even affect the stability of

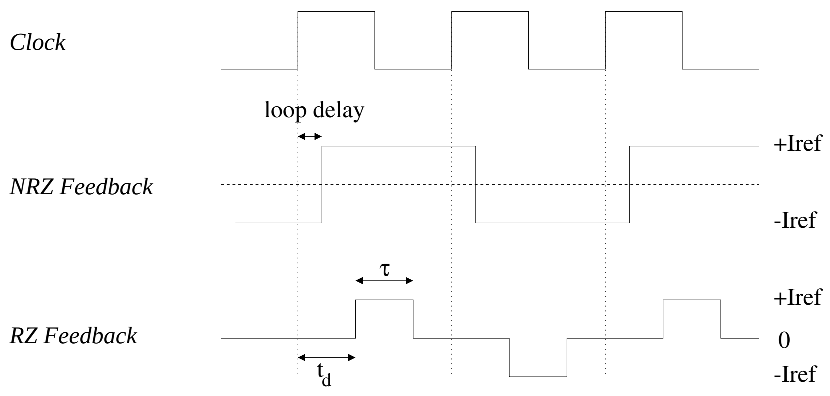

Figure 6.1: *Comparator delay*.

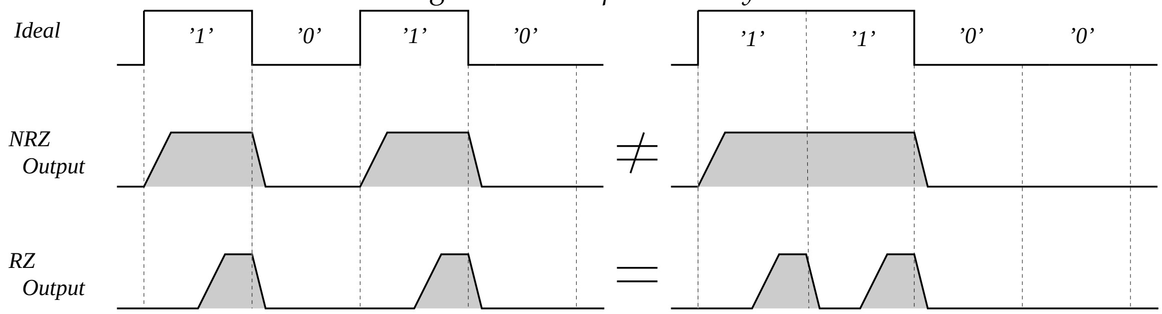

Figure 6.2: *Rise and fall time asymmetry*.

the modulator.

Note also that for small signal amplitudes, the comparator response-time becomes signal-dependent. This has the effect of jittering the edges of the NRZ feedback signal and consequently increasing the noise level in the signal band [Cherry97].

If a Return-to-Zero (RZ) feedback signal is used, signal-to-noise ratio degradation due to excess loop delay can be significantly reduced. As shown in Figure 6.1, the feedback signal is applied after a delay time, t_d, during which the feedback signal is zero. This delay should be sufficiently large to allow for a complete settling of the quantizer output.

6.2.2 Rise and Fall Time Asymmetry

When DAC output current pulses, having unequal rise and fall times, are integrated, the result of the integration depends on the DATA sequence. This DATA dependency produces harmonic distortion [Zwan96].

As shown in Figure 6.2, the effect of this feedback waveform asymmetry can be highly attenuated

Figure 6.3: *(a) Pulse-delay clock jitter (constant τ). (a) Pulse-width clock jitter (constant t_d).*

by using a RZ feedback signal [Zwan97].

In order to overcome problems related to loop delay and feedback waveform asymmetry, we have chosen to use a RZ feedback signal.

6.3 Clock Jitter

In the following, we will study the clock jitter effect on the performance of a continuous-time $\Sigma\Delta$ modulator with RZ feedback signal.

6.3.1 Pulse-Delay and Pulse-Width Jitter

Jitter is the intrinsic uncertainty in the time-instant of the clock transitions. In this analysis, we will assume that uncertainty in the time-instants of the RZ feedback signal causes two types of clock jitter. The random variation in the delay time t_d is called *pulse-delay* clock jitter and the random variation in pulse width τ is called *pulse-width* clock jitter. These two types of jitter are illustrated in Figure 6.3. Several simulations are performed in order to study separately the effect of each type of jitter on the overall performance of the $\Sigma\Delta$ modulator. A second-order $\Sigma\Delta$ modulator with RZ feedback signal, having $t_d = 0.5T$ and $\tau = 0.4T$, is simulated with a SPICE-like circuit simulator ELDO [Men00]. The simulations are performed with ideal integrator, DAC and comparator models. With an oversampling ratio of 128 the modulator has a signal-to-quantization noise SNR_Q of 82 dB when the input signal is -6dB. Jitter noise is introduced to the clock in the feedback signal. The two types of clock jitter are assumed to be white, uncorrelated and with Gaussian distribution. Note that these are very lengthy simulations, since the simulator time-slice has to be very small to take the jittered clock into account.

From Figure 6.4, we can see that that the pulse-width jitter has a much more degrading effect on

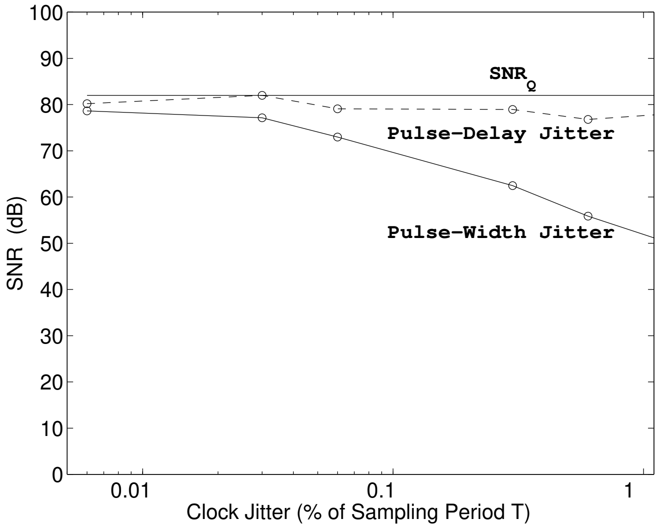

Figure 6.4: *Pulse-delay jitter and pulse-width jitter impact on SNR of a* 2^{nd} *order modulator with OSR=128 and input amplitude = -6dB.*

the signal-to-noise ratio than the pulse-delay jitter.

Therefor, in the following analysis, we will neglect the pulse-delay jitter and only the pulse-width jitter will be taken into account.

6.3.2 Jitter in Rectangular Feedback Signal

In order to calculate the noise power generated by the pulse-width clock jitter, let us look at the output of the first integrator of the modulator in the ideal case

$$\frac{1}{T}\int_{t_d}^{t_d+\tau} \frac{T}{\tau}\ dt = 1 \tag{6.1}$$

If the pulse-width has an error of $\delta\tau$, the output of the first integrator will be

$$\frac{1}{T}\int_{t_d}^{t_d+\tau+\delta\tau} \frac{T}{\tau}\ dt = 1 + \frac{\delta\tau}{\tau} \tag{6.2}$$

The error in the output of integration is then equal to $\frac{\delta\tau}{\tau}$. Assuming that the clock jitter causes timing errors $\delta\tau$ with variance ${\sigma_j}^2$, we can say that the jitter noise power in the signal band is equal to

$$\text{Jitter Noise Power} = \frac{{\sigma_j}^2}{\tau^2}\frac{f_s}{2\,OSR} \tag{6.3}$$

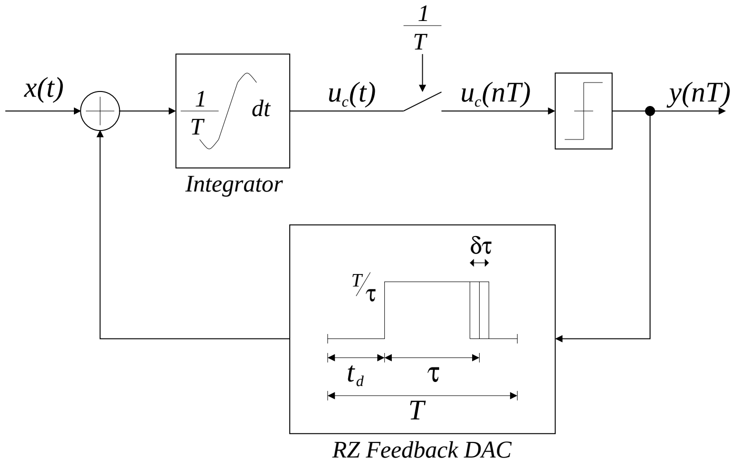

Figure 6.5: *Continuous-time* $\Sigma\Delta$ *modulator model used to derive the signal-to-jitter noise ratio* SNR_J *for a jittered rectangular RZ feedback signal.*

The signal-to-jitter noise ratio, SNR_J, can then be described by the following relation

$$SNR_J = \frac{\alpha^2\ \tau^2}{\sigma_j{}^2}\frac{OSR}{f_s} \tag{6.4}$$

where α is the amplitude of the sinusoidal input signal.

From equation (6.4), we can see that the signal-to-jitter noise ratio is directly proportional to τ. Since in the NRZ case, $\tau = T$, and in the RZ case, $\tau < T$, it is clear that continuous-time $\Sigma\Delta$ modulators with a RZ feedback signal are more sensitive to clock jitter than modulators with a NRZ feedback signal.

In order to verify equation (6.4), we have simulated the third order 1-bit 128x oversampling $\Sigma\Delta$ modulator, presented in section 5.6.2. The feedback signal has a pulse-delay $t_d = \frac{T}{4}$ and a pulse-width $\tau = \frac{3T}{4}$. In each clock cycle the error in the pulse-width is modeled by an error in the pulse amplitude instead of changing the edge timing [Adams98]. This allows us to perform rapid simulations using *MATLAB* instead of the lengthy simulations described in the previous section.

The results of these simulations, along with calculations using equation (6.4), are illustrated in Figure 6.6. In this Figure we can see the signal-to-noise ratio in function of the clock jitter represented in percentage of the clock period T. Note that the SNR values obtained by simulation are very close to the values predicted by equation (6.4). It is clear that, for the third order modulator with an OSR of 128, we need clock jitter to be less than $0.01\%T$ in order to obtain a SNR_J higher than the SNR_Q.

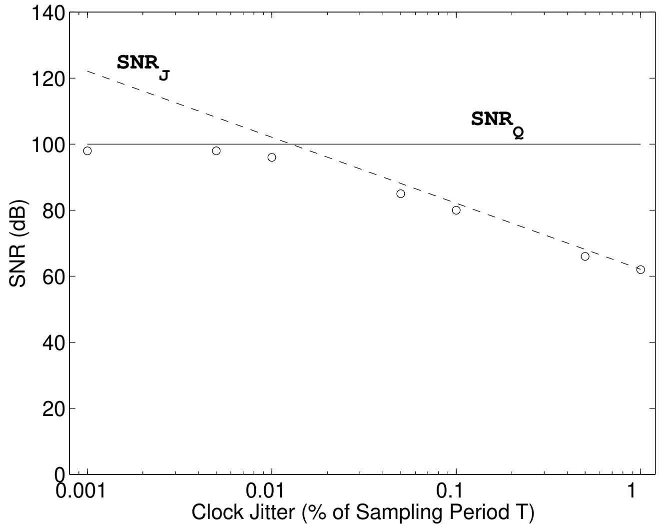

Figure 6.6: *Jitter sensitivity from simulation (circles) and calculations (dashed-line) for a third order 1-bit 128x oversampling $\Sigma\Delta$ modulator with white Gaussian clock jitter.*

Clock jitter can be a serious limitation to the performances of continuous-time $\Sigma\Delta$ especially at high sampling frequencies.

6.3.3 Jitter in Decaying Ramp Feedback Signal

In order to calculate the noise power generated by the pulse-width clock jitter, let us look at the output of the first integrator of the modulator in the ideal case

$$\frac{1}{T}\int_{t_d}^{t_d+\tau} \frac{2T}{\tau}[1+\frac{t_d}{\tau}-\frac{t}{\tau}]\ dt = 1 \tag{6.5}$$

If the pulse-width has an error of $\delta\tau$, the output of the first integrator will be

$$\frac{1}{T}\int_{t_d}^{t_d+\tau+\delta\tau} \frac{2T}{\tau}[1+\frac{t_d}{\tau}-\frac{t}{\tau}]\ dt = 1-\frac{\delta\tau^2}{\tau^2} \tag{6.6}$$

The error in the output of integration is then equal to $\frac{\delta\tau^2}{\tau^2}$. Assuming that the clock jitter causes timing errors $\delta\tau$ with variance ${\sigma_j}^2$, we can say that the jitter noise power in the signal band is equal to

$$\text{Jitter Noise Power} = \frac{{\sigma_j}^4}{\tau^4}\frac{f_s}{2\,OSR} \tag{6.7}$$

The signal-to-jitter noise ratio, SNR_J, can then be described by the following relation

$$SNR_J = \frac{\alpha^2\ \tau^4}{{\sigma_j}^4}\frac{OSR}{f_s} \tag{6.8}$$

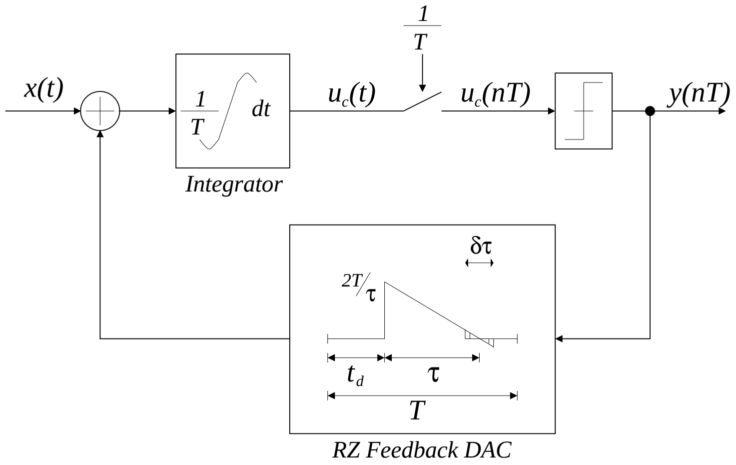

Figure 6.7: *Continuous-time $\Sigma\Delta$ modulator model used to derive the signal-to-jitter noise ratio, SNR_J, for a jittered decaying ramp RZ feedback signal.*

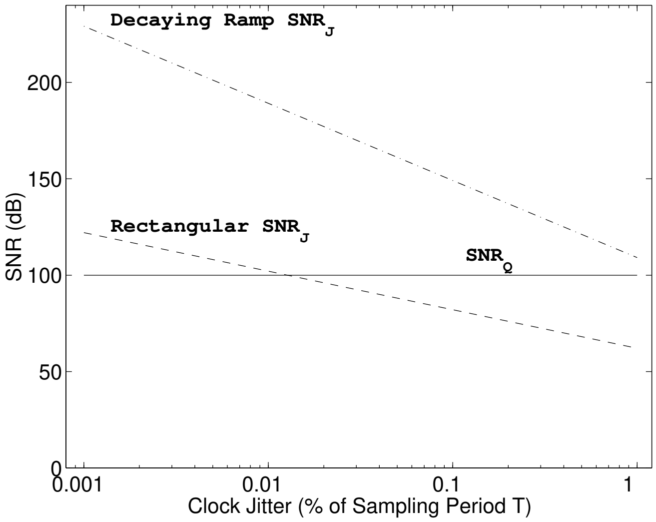

Figure 6.8: *Comparison between signal-to-jitter noise, SNR_J, of a CT $\Sigma\Delta$ modulator with rectangular RZ feedback signal, equation (6.4) (dashed), and decaying ramp RZ feedback signal, equation (6.8), (dash-point).*

In Figure 6.8 we compare the SNR_J of the rectangular pulse and the SNR_J of the decaying ramp feedback signal. The feedback signal has a pulse-delay $t_d = \frac{T}{4}$ and a pulse-width $\tau = \frac{3T}{4}$. It is obvious that continuous-time $\Sigma\Delta$ with decaying ramp feedback signal are much less sensitive to clock jitter than conventional rectangular feedback signals.

Similar performances are expected from the decaying RC feedback signal presented in chapter 4.

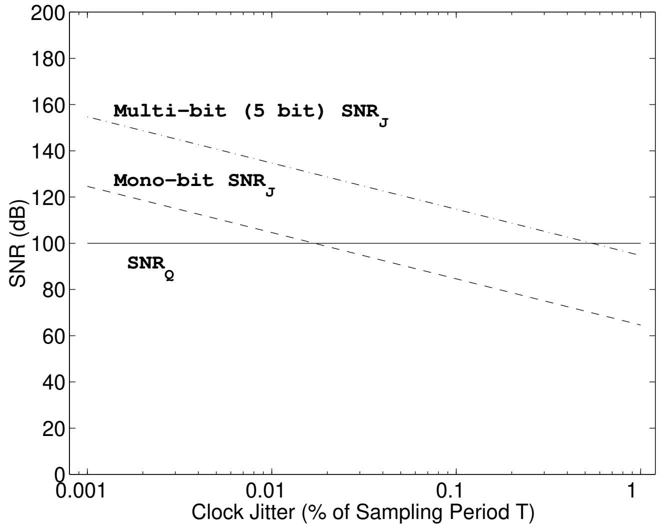

Figure 6.9: *Comparison between signal-to-jitter noise, SNR_J, of a mono-bit CT $\Sigma\Delta$ modulator with NRZ rectangular feedback signal (dashed), and multi-bit (5-bit) NRZ feedback signal (dash-point).*

Although these are interesting results, practical implementation of a such signals in the feedback of $\Sigma\Delta$ modulator is rather difficult and needs more investigation.

6.3.4 Jitter in Multi-bit $\Sigma\Delta$ Modulators

Another interesting solution to reduce continuous-time $\Sigma\Delta$ modulators sensitivity to clock jitter is to use a multi-bit quantizer [Adams98] [Aboushady99c]. The feedback DAC step size in a multi-bit modulator is significantly lower than in the 1-bit case and thus the jitter sensitivity is reduced proportionally. In fact we can say that:

$$\text{Multi-bit Jitter Noise Power} = \frac{\text{Single-bit Jitter Noise Power}}{(\text{Number of Quantization Steps})^2} \tag{6.9}$$

In Figure 6.9 we compare the SNR_J of the rectangular pulse and the SNR_J of a 5-bit DAC feedback signal. We can see that significant improvement in clock jitter sensitivity can be achieved using the multi-bit modulator. Pulse waveform asymmetry is also reduced by the same amount as clock jitter noise. Equation 6.9 is valid only for NRZ feedback signals. In a RZ feedback signal, large transitions occur at each clock cycle. This results in higher jitter and pulse waveform asymmetry similar to monobit modulators. If nonlinearity due feedback pulse asymmetry needs to be reduced, a dual RZ feedback signal could be used [Adams98] [Aboushady99c].

Note also that Data-Weighted-Averaging (DWA) techniques should be used to reduce harmonic distortion due to DAC elements mismatch [Baird95].

6.4 Return-to-Zero Feedback DAC Circuit

In the following, we will describe a RZ feedback DAC circuit with $t_d = \frac{T}{4}$ and $\tau = \frac{3T}{4}$. Special care was taken in the implementation of the digital control signal, in order to improve the switching characteristics of the DAC.

Figures 6.10 and 6.11 show the DAC circuit and the corresponding control signals respectively. An external clock frequency equal to twice the sampling frequency is required in order to get a $\frac{T}{4}$ RZ phase at the beginning of each cycle. The output current is directed either to $I_{DACOUT+}$ or $I_{DACOUT-}$ depending on the comparator output DATA.
During RZ phase, the positive and negative current sources are connected together through the DUMP node. In addition to reducing errors due to comparator delay and DAC output waveform asymmetry, connecting the current sources to the DUMP node at the beginning of each cycle has 2 other important features:

1. The switching sequence is DATA independent. This renders charge injection DATA independent and then no harmonic distortion is produced.

2. The drain of the current source transistor is always charged to the same potential before the new data signal connects the current source to one of the outputs. This reduces the error current due to residual charges on this node from the previous output connections.

The purpose of cascoding the switch transistor is to:

1. reduce the capacitance seen by the output node (the input of the integrator). This reduces error current due to charging of the drain of the current source transistor to the potential of the output node.

2. prevent any voltage variations at the output from reaching the drain of the current source transistor.

3. increase the output resistance of the current source.

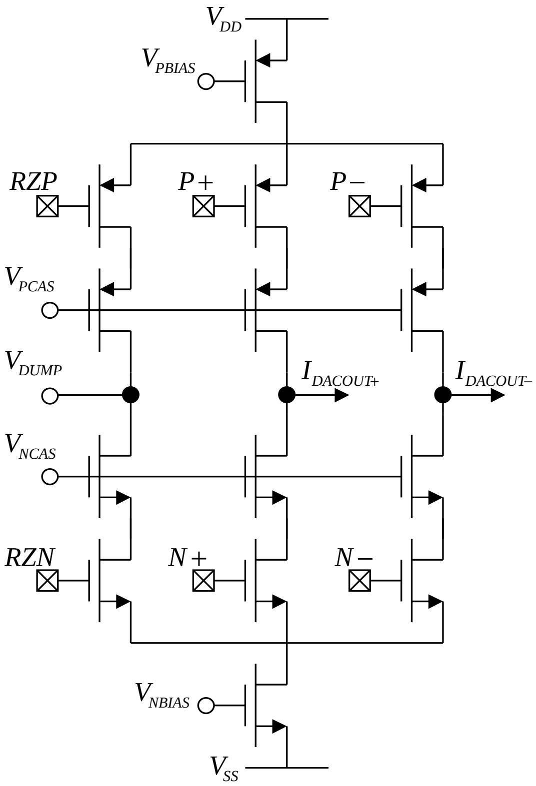

Figure 6.10: *DAC Circuit*.

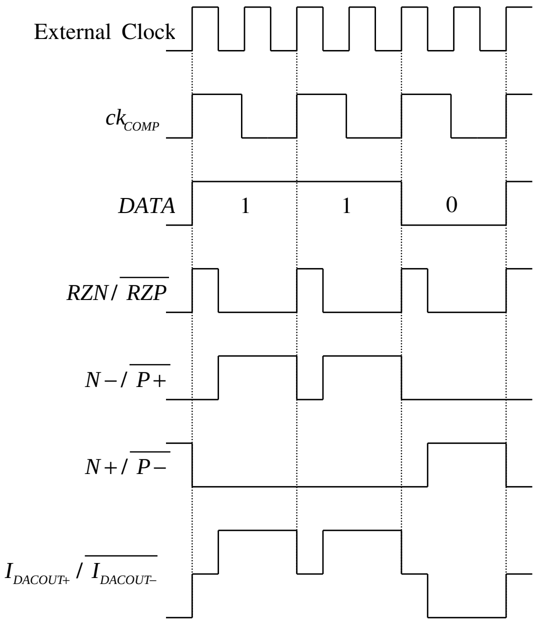

Figure 6.11: *DAC Control Signals*.

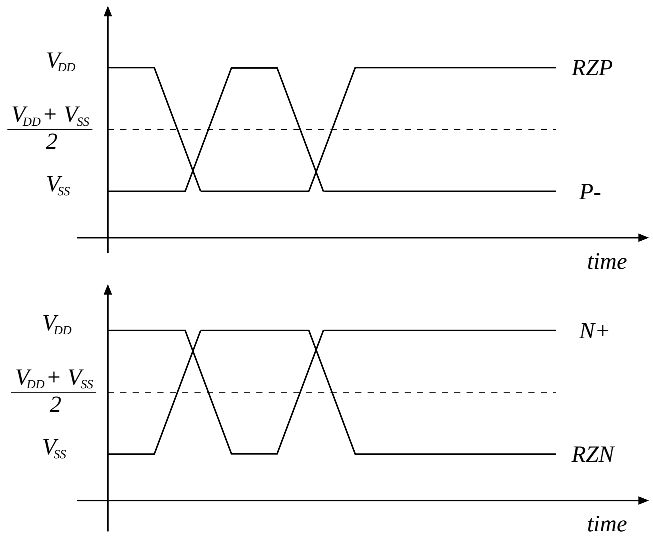

Figure 6.12: *Timing diagram of high-crossing NMOS-switch control signals and low-crossing PMOS-switch control signals.*

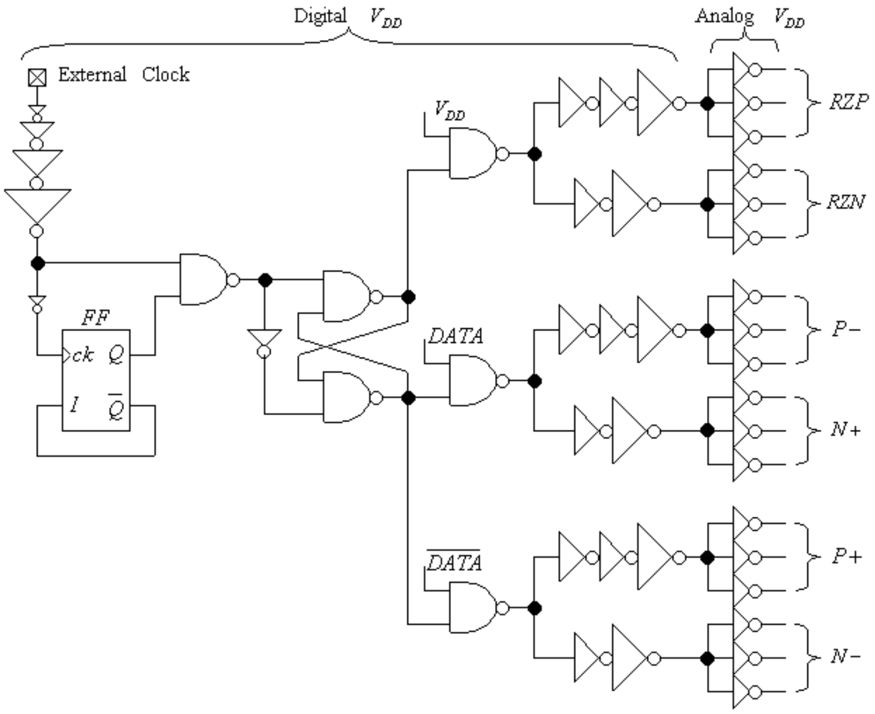

Figure 6.13: *DAC control signals for a third order ΣΔ modulator having 3 RZ DACs in the feedback loop.*

4. prevent glitches that occur during switching from reaching the output through C_{gd} of the switch transistor [Takakura91].

Current source transistors must always keep constant current flow. If the switching transistors are simultaneously turned OFF, the current transistor drain rapidly discharges and will need much time to recharge.
To ensure that the current from the current source can flow to either one of the outputs, the signals controlling the NMOS switches (RZN, N+, and N-) have a high crossing point. In the same way, the PMOS switches control signals (RZP, P+ and P-) have a low crossing point. A timing diagram of the switching control signals is illustrated in Figure 6.12.

The digital circuit generating the DAC control signals of Figure 6.11 with high-crossing and low-crossing points, as shown in Figure 6.12, is illustrated in Figure 6.13.

Note that in order to reduce the clock jitter on the control signals, the inverters driving the DAC switches are supplied from the analog V_{DD}[1].

6.5 Conclusion

In this chapter, it has been shown that RZ feedback signal can reduce errors due to loop delay and waveform asymmetry.
Clock jitter can be a serious limitation to the performances of continuous-time $\Sigma\Delta$ especially at high sampling frequencies. Using a decaying ramp feedback signal or a multi-bit DAC can significantly reduce signal-to-noise ratio degradation due to clock jitter.
A RZ current-source DAC has been presented. Cascode switches and careful design of the digital control circuit have been used to reduce any switching errors.

[1] Large transitions in these inverters might polute the analog V_{DD}. In [Gielen01], it is proposed to use a third supply voltage for these inverters.

Chapter 7

Analog Design Automation

7.1 Introduction

In this chapter we present a design automation tool for current-mode continuous-time $\Sigma\Delta$ modulators. First, the design methodology is proposed in section 7.2. Circuit synthesis and validation are presented in sections 7.3 and 7.4. Design examples are given in section 7.5, and the layout generation method is explained in section 7.6.
Finally, the main features of the presented design automation tool are discussed in section 7.7.

7.2 Design Methodology of Continuous-Time Current-Mode $\Sigma\Delta$ Modulator

Continuous-time current-mode $\Sigma\Delta$ modulator design methodology is illustrated in Figure 7.1. In this figure, we can see the design procedure of the $\Sigma\Delta$ modulator from system specifications to layout. The design process can be divided into four main levels:

- System level design
- Circuit level design with simplified MOS transistor models
- Circuit level design with advanced MOS transistor models
- Layout level design

7.2.1 System Level Design

When designing a continuous-time $\Sigma\Delta$ modulator, the first step is to select the modulator topology $(CIFF, CIFB, CRFF, ...)$, order (n) and oversampling ratio (OSR). These parameters should be chosen in such a way that the modulator achieves the desired Signal-to-Noise Ratio (SNR). This is first done for a discrete-time $\Sigma\Delta$. That is because design techniques for discrete-time $\Sigma\Delta$ modulators have been well established [Candy92] [Norsworthy97]. Moreover, the simulation of discrete-time $\Sigma\Delta$ modulators is much faster than continuous-time $\Sigma\Delta$ modulators. In chapter 4, a discrete-time to continuous-time tranformation technique for $\Sigma\Delta$ modulators has been proposed. This technique based on the modified-z-transform has been implemented in a symbolic mathematical tool *MAPLE* [Wat97]. We have also seen that, using this tool, it is possible to generate symbolic correspondance tables between DT and CT modulators with return-to-zero (RZ) feedback signal for the different $\Sigma\Delta$ topologies. The CT modulator coefficients are given in these tables in function of the DT coefficients and the RZ feedback signal characteristics. As shown in Figure 7.1, the final CT coefficients are obtained by scaling the coefficients resulting from the DT-to-CT transformation. Scaling is performed either:

- to obtain maximum swing at the output of each integrator of the modulator

or

- to fix the gain of the first integrator A_{int_1} to a certain value that achieves the required linearity. the rest of the coefficients must be scaled in order to maintain the same noise transfer function.

When the final CT $\Sigma\Delta$ coefficients are scaled, it is necessary to simulate the modulator in order to validate its performances. This simulation are performed using MATLAB [Mat97].

7.2.2 Circuit level design with simplified MOS transistor models

As shown in Figure 7.1, the next step after finding the CT $\Sigma\Delta$ modulator is to design the continuous-time cascode current-mirror based integrator, Figure 5.5. From the input circuit characteristics, the supply voltage, V_{DD}, and the effective gate voltage of transistor M_3, $V_{EG_{3_0}}$, we can calculate the modulation index of the cascode current mirror, using equation (5.13), repeated

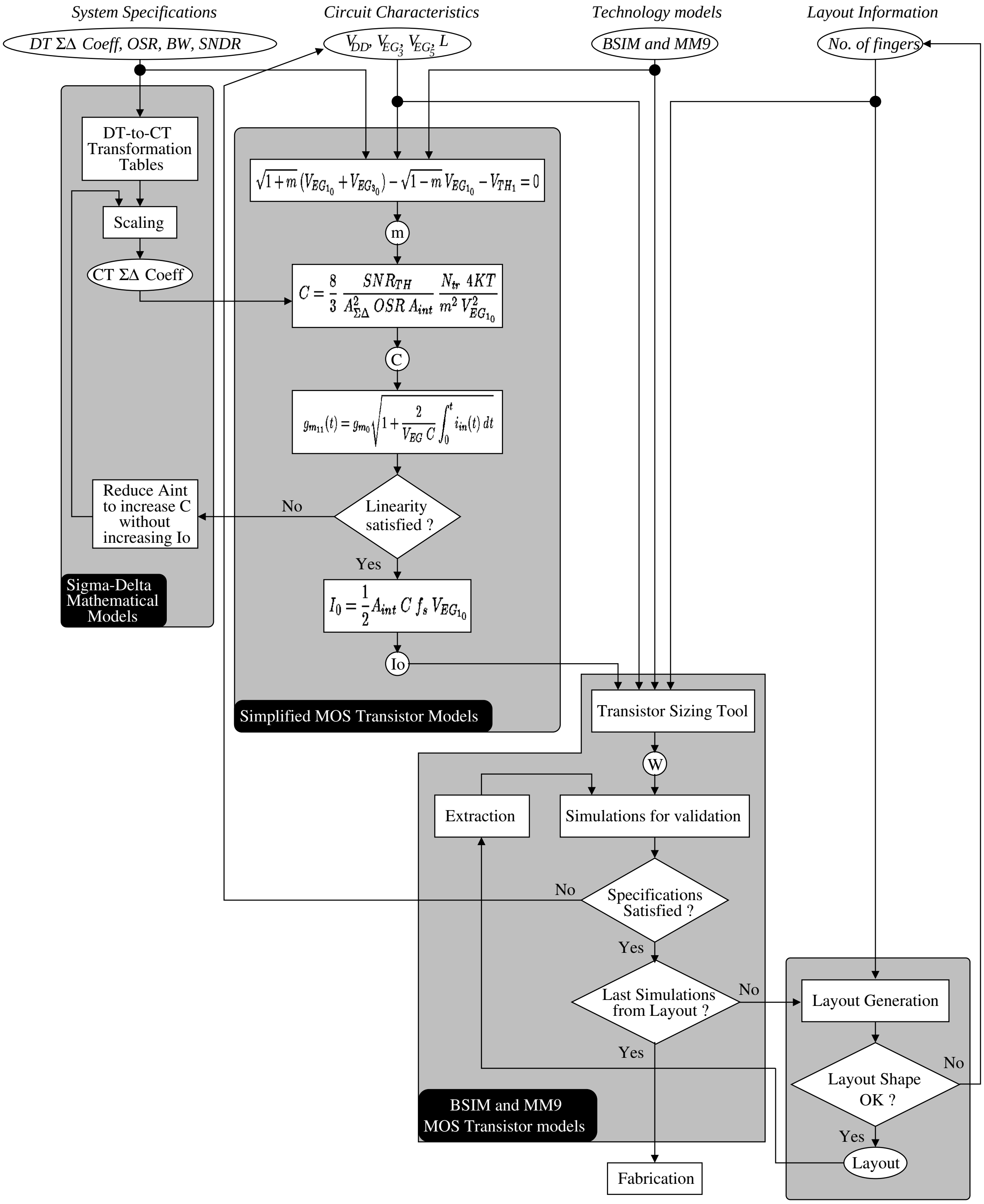

Figure 7.1: *Continuous-time current-mode ΣΔ modulator design methodology.*

here for convenience:

$$\sqrt{1+m}\,(V_{EG_{1_0}} + V_{EG_{3_0}}) - \sqrt{1-m}\,V_{EG_{1_0}} - V_{TH_1} = 0 \tag{7.1}$$

Since the Bulk-Source voltage of transistor M_1 is equal to zero, we can make the approximation that $V_{TH_1} = V_{TH_0}$, where V_{TH_0} is the MOS transistor threshold voltage given by the technology models. We also choose to bias the input node to half the supply voltage, the effective gate voltage of transistor M_1 is then equal to $\frac{1}{2}V_{DD} - V_{TH_0}$. In the case of transistor M_3, the effective gate voltage V_{EG_3} is given as an input parameter of the circuit characteristics.

The modulation index, m, resulting from equation (7.1), is used in equation (5.28), to calculate the minimum integrating capacitance, C, necessary to achieve the desired SNR. Equation (5.28) is repeated here for convenience:

$$C = \frac{8}{3}\,\frac{SNR_{TH}}{A^2_{\Sigma\Delta}\;OSR\;A_{int}}\,\frac{N_{tr}\;4KT}{m^2\;V^2_{EG_{1_0}}} \tag{7.2}$$

the first integrator gain, A_{int_1}, and the input signal gain for maximum SNR, $A_{\Sigma\Delta}$, are parameters calculated during the system level design.

From equation (5.35), we know that the integrating capacitance not only influence the circuit thermal noise but also has an important impact on the linearity of the integrator. Equation (5.35) is repeated here for convenience:

$$g_{m_{11}}(t) = g_{m_0}\sqrt{1 + \frac{2}{V_{EG}\;C}\int_0^t i_{in}(t)\;dt} \tag{7.3}$$

That is why at this stage of the design we should verify that the integrating capacitance obtained form equation (7.2) satisfies the linearity requirements of $\Sigma\Delta$ modulator. If the harmonic distortion is higher than desired, the value of the C should be increase to improve linearity. From equation (5.19),

$$I_0 = \frac{1}{2}\,A_{int_1}\;C\;f_s\;V_{EG_{1_0}} \tag{7.4}$$

it is obvious that increasing C would directly lead to increasing the biasing current I_0. Another low-power alternative would be to reduce A_{int_1} to compensate for any increase in C. In this case all the modulator coefficients should be scaled in order to keep the transfer function unchanged. This low-power solution requires that all the modulator coefficients be scaled in order to keep the transfer function unchanged. After several iterations, we finaly find the integrating capacitance

C that achieves the desired linearity and thermal noise. Equation (7.4) is then used to find the biasing current I_0.

In addition to the integrating capacitance, C, and the biasing current, I_0, the transistor biasing voltages, (V_{DS}, V_{BS}, V_{EG}), of the different transistors are also calculated using the simplified MOS transistor models presented chapter 5.

7.2.3 Circuit level design with advanced MOS transistor models

At this step of the design, all transistors DC parameters (bias voltages and drain-source current) have been calculated using the simplified MOS transistor models. The next step consists in calculating the transistors sizes using the accurate transistor models implemented in COMDIAC [Porte99]. This tool offers a set of functions for transistor sizing in order to calculate DC parameters as well as small signal parameters using the same models used by SPICE-like circuit simulators. The most widely used transistor models, BSIM [Berkeley00] and MM9 [Philips00], are implemented in this sizing tool. For example, given transistor bias voltages, drain-source current and channel length, COMDIAC calculates the width of the transistor and its small-signal parameters.

After sizing all the transistors we can now generate the SPICE-netlists of the different subcircuits of the $\Sigma\Delta$ modulator. A set of SPICE simulations, using the advanced MOS models (BSIM and MM9), is performed to validate the performance of the generated $\Sigma\Delta$ modulator. These simulations will be detailed in the next section.

If simulation results reveal that the modulator specifications have not been satisfied, it is possible to modify the circuit characteristics and to repeat the circuit design procedure. Since the 1/f noise has not been taken into account in the design procedure, it is expected that several iterations will be required in order to find the appropriate transistor length that gives a sufficiently low 1/f noise.

When the modulator specifications are satisfied, it is now possible to start the layout.

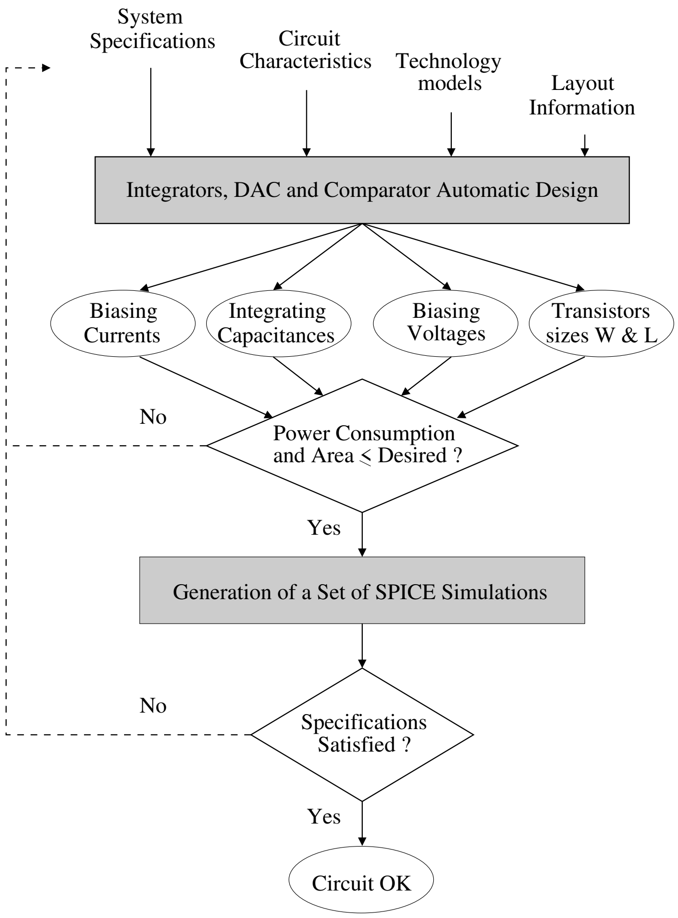

Figure 7.2: $\Sigma\Delta$ *design automation*.

7.2.4 Layout level design

The layout of the complete $\Sigma\Delta$ modulator is described hierarchically using a Layout language CAIRO[1] [Dessouky00a] [Dessouky00b]. CAIRO is composed of a superset of C functions. This offers indenpendence from any CAD vendor and takes advantage of the C language sophisticated constructs. The code written with CAIRO is independent from devices dimensions and fabrication process. In fact, either we change the specifications of the $\Sigma\Delta$ modulator, the fabrication process or both the layout can be generated without modifying the CAIRO code.

As seen in Figure 7.1, the generated layout should be extracted and simulated as a final validation step before sending the circuit for fabrication.

[1]CAIRO stands for ”Circuits Analogiques Intégrés Réutilisables et Optimisés”

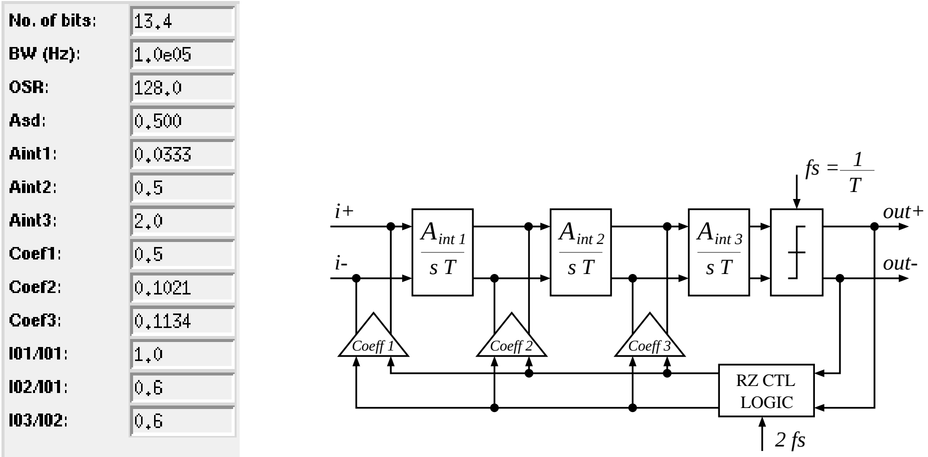

Figure 7.3: *System specifications for ΣΔ design automation.*

7.3 Circuit Synthesis

The design methodology of continuous-time current-mode ΣΔ modulator has been implemented in a design automation program for the special case of a third order CIFB topology. The program has been implemented in C language. In Figure 7.2, we show a flowchart describing the implemented ΣΔ circuit synthesis tool. An interactive graphical interface has been implemented to enter the input specifications, the circuit characteristics, the technology process and some layout information. This graphical interface displays the circuit synthesis results. This provides an easy way to explore the design space for the designer.

In order to help the designer check the resulting circuit, the different SPICE simulation files necessary to verify the modulator circuit performances are automatically generated by the tool.

In the following we will present the features of this CAD environment :

- System Specifications:

  In Figure 7.3, we show the graphical interface used to define the system specifications of the third order ΣΔ modulator.

- Circuit Characteristics:

  In Figure 7.4 and Figure 7.5, we show the graphical interface used to define the integrator and feedback DAC circuit characteristics.

- Technology Models:

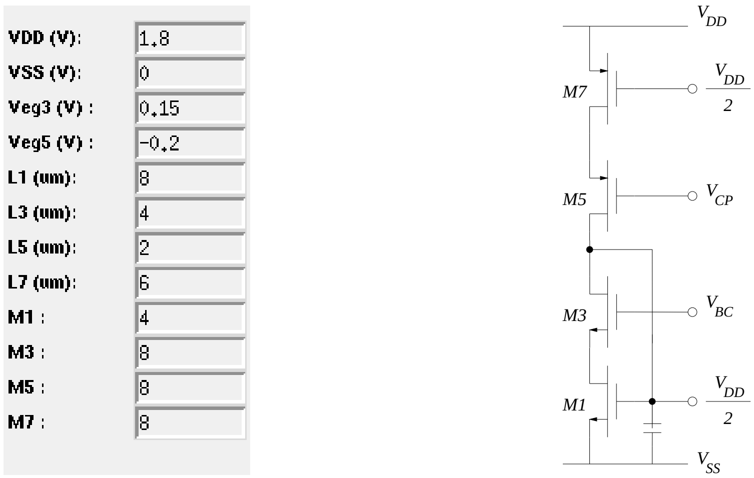

Figure 7.4: *Integrator circuit characteristics for* $\Sigma\Delta$ *design automation*.

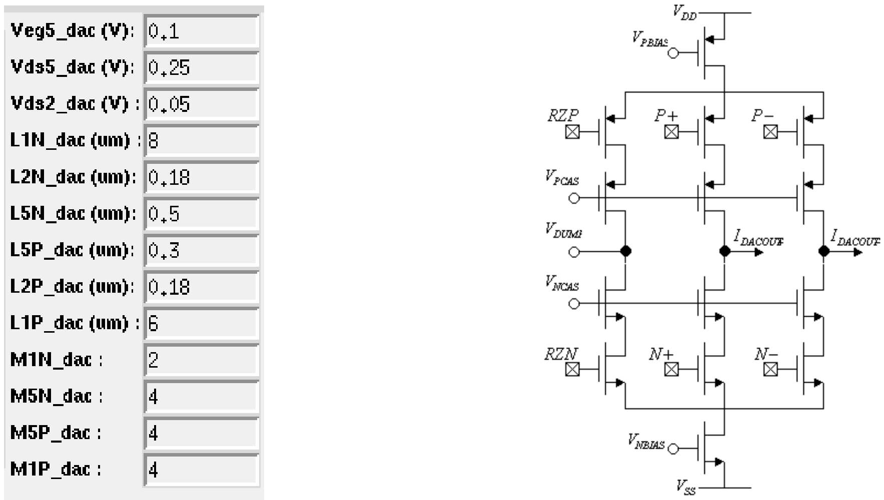

Figure 7.5: *System Specifications* $\Sigma\Delta$ *design automation*.

The BSIM or MM9 transistor models of the used technology process are selected at the beginning of each design.

- Layout Information:
  In addition to the number of fingers, M, of each transistor given with the circuit characteristics, it also possible to give some mismatch information. This information is used during the generation of the SPICE simulation files to introduce mismatch between the sensitive mirror transistors of the integrator.

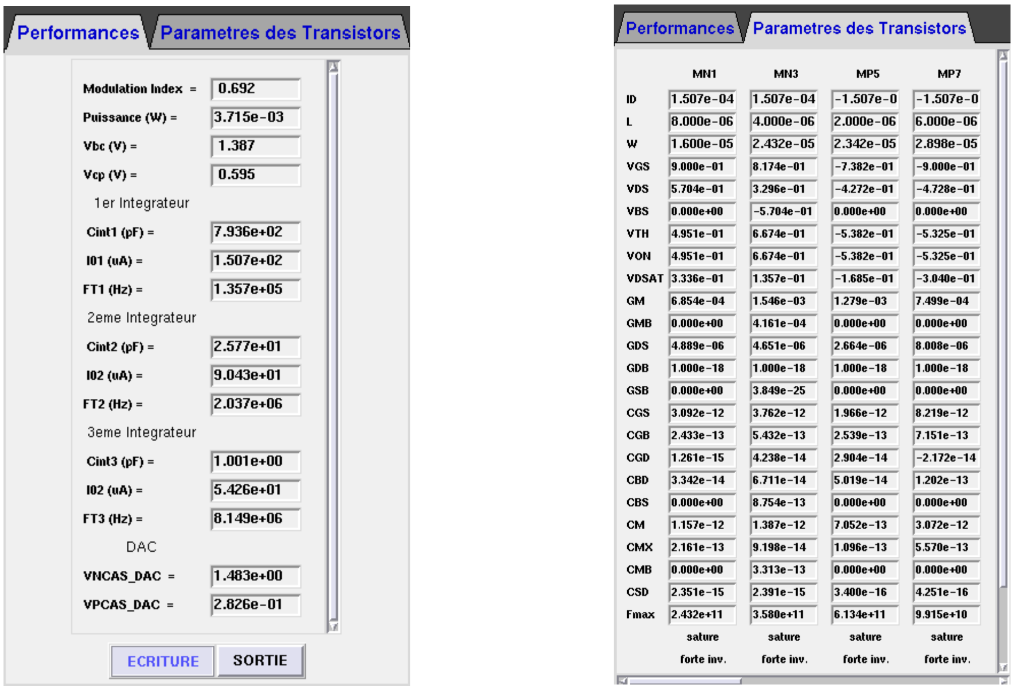

Figure 7.6: *Power consumption, modulation index, integrating capacitances, biasing voltages, ...*

After entering all the input specifications and characteristics of the desired third order continuous-time $\Sigma\Delta$ modulator, we execute the design automation program which gives two set of outputs. The first one, displayed on window presented in Figure 7.6, consists of the main resulting characteristics and performances of the generated circuit, computed by the $\Sigma\Delta$ tool. The second one, displayed in the second window presented in Figure 7.6 provides all the DC and small signal parameters of the integrator transistors computed with the accurate model of transistors. If the power consumption and the capacitors values of the generated circuit are not acceptable, we can modify some input circuit characteristics (Fig. 7.4, 7.5) and regenerate the modulator circuit. When the resulting circuit characteristics are acceptable we can then start the validation procedure. This is described in the following section.

7.4 Circuit Validation

Despite the fact that the transistor sizing functions within COMDIAC use advanced MM9 and BSIM models to size transistors, the design procedure used to calculate the integrating capacitance and the biasing current presented in chapter 5 is based on simplified models of the MOS transistor.

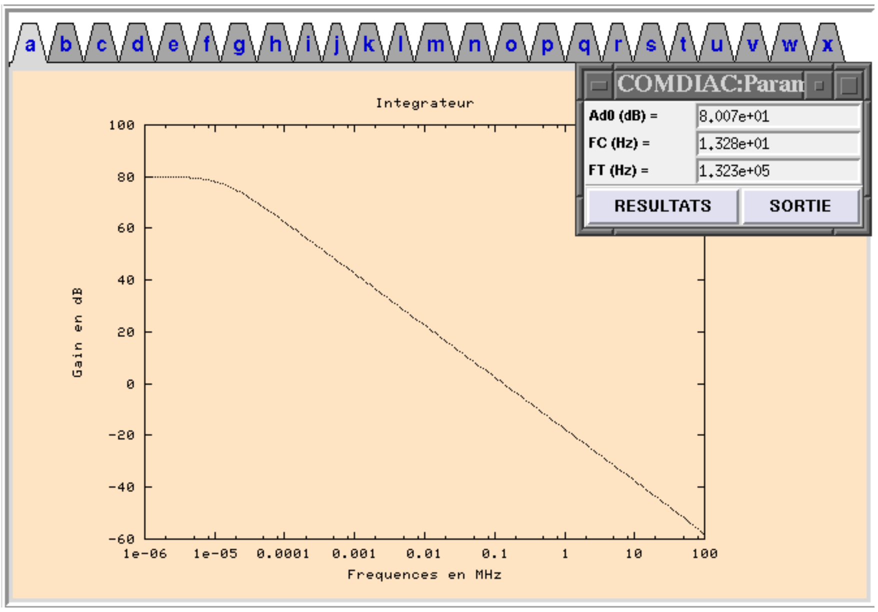

Figure 7.7: *Integrator frequency response.*

Therefore it is necessary to simulate the generated circuits using the MM9 and BSIM SPICE models before starting the layout. In this section, we will describe a set of simulations that are necessary to validate the circuits generated from the design automation tool described in the previous section. The files needed to perform the simulations are provided by the $\Sigma\Delta$ design automation tool.

7.4.1 AC Analysis

First, we start with an AC analysis of the integrators. The objective of these simulations is to verify that the designed integrators have the required frequency response. For each integrator, the following frequency response characteristics should be verified:

- The integrator unity gain frequency, f_T, should be related to the integrator gain, A_{int}, and the sampling frequency of the modulator f_s according to the following relation:

$$f_T = \frac{A_{int}\ f_s}{2\ \pi} \tag{7.5}$$

  This relation can be derived directly from equation (5.15).

- The DC gain, A_0, should be sufficiently high. The DC gain of the integrators in $\Sigma\Delta$ modulators should be greater than the oversampling ratio [Wongkomet95].

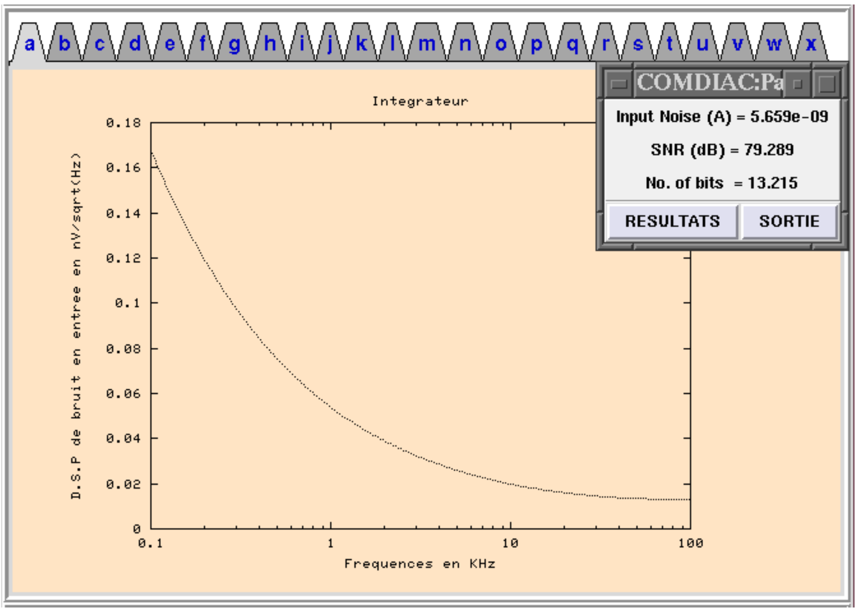

Figure 7.8: *The input noise current in the band of interest.*

The unity gain frequency and the DC gain of the integrator are measured from the simulation and displayed in a small window along with the frequency response in the main window, as shown in Figure 7.7.

7.4.2 Noise Analysis

As already described in chapter 5, it is assumed that the quantization noise power is sufficiently lower than the circuit noise to be neglected. There exists two types of circuit noise: thermal noise and 1/f noise. The thermal noise has been carefully analysed in chapter 5, and is taken into account in the design procedure. On the other hand, the 1/f noise has not been taken into account in the design procedure. The 1/f noise can be reduced by having large transistor areas [Gray93].

The purpose of the noise analysis simulation is to verify that the thermal noise and the 1/f noise levels are sufficiently low to achieve the desired signal-to-noise ratio. Usually several iterations are necessary to find the appropriate transistor lengths for the required level of 1/f noise.

The total input noise current in the band of interest is measured by simulation and displayed in a small window along with the noise frequency response, as shown in Figure 7.8. From the total noise current we can estimate the signal-to-noise ratio and the corresponding number of bits that can be expected from the modulator.

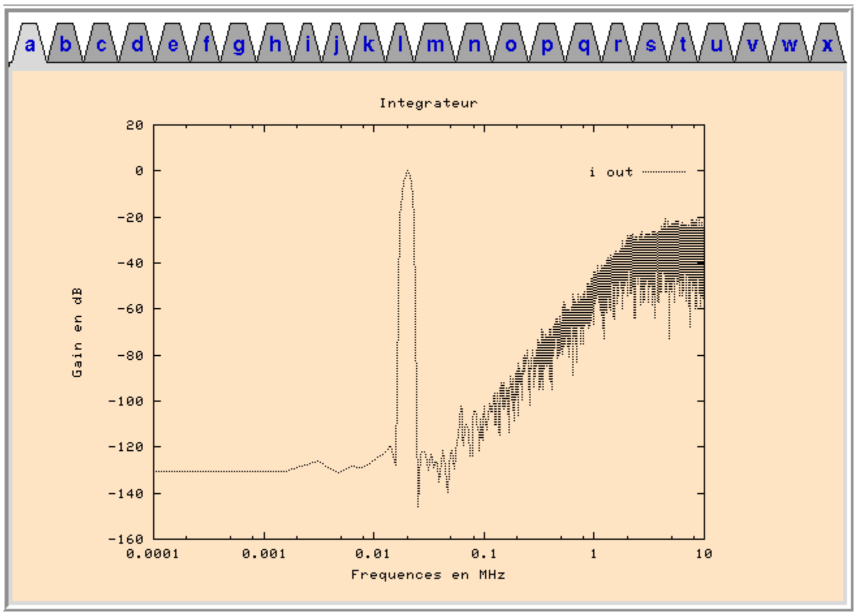

Figure 7.9: *Power spectral density of the generated continuous-time ΣΔ modulator output signal.*

7.4.3 Transient Analysis

Finally, a transient analysis of the complete ΣΔ modulator should be performed. Transient simulation is mainly to estimate harmonic distortion of the modulator, as well as to verify the performance of the comparator, the feedback DACs and the digital circuits generating the sampling clock and the RZ control signals. It can also be used to study the effect of the integrators gain and mismatch in mirror transistors on the overall performance of the ΣΔ modulator, as described in section 5.6.2.

Due to the large number of transistors involved in the simulation of this sampled system, the cpu-time required to accomplish such transient simulations is very high. Therefore, we start by simulating the ΣΔ modulator with an ideal comparator and ideal feedback DACs. If the results are satisfactory, we start replacing each ideal block by its transistor netlist representation. This is done until the complete ΣΔ modulator is modeled by transistors. In Figure 7.9, we show the power spectral density of ΣΔ modulator output signal. From the power spectral density, we can calculate the signal-to-quantization-noise ratio and verify that it is sufficiently low compared to the signal-to-noise ratio measured during the circuit noise analysis.

Table 7.1: *Circuit characteristics of the third order modulator, with the specifications described in Figure 7.3, designed using the design automation program.*

	Circuit I	Circuit II
Technology Process	0.6μm	0.18μm
Supply Voltage	3.3 V	1.8 V
Modulation Index, m	0.7	0.7
1^{st} Integrator Capacitance, C_1	191 pF	794 pF
1^{st} Integrator Current, I_{0_1}	70μA	150μA
Power Consumption	3.2 mW	3.7 mW

7.5 Design Examples

7.5.1 Process Migration

In order to show how the design automation program presented in this chapter is useful in designing continuous-time current-mode $\Sigma\Delta$ modulators, we will present different design examples. We will first design two third order $\Sigma\Delta$ modulators with the same specifications, shown in Figure 7.3, but in different CMOS technology processes. This is to show that the design reuse aspect in the case of process migration. Both circuits achieve the same performances and have the circuit characteristics listed in table 7.1.

7.5.2 Different Specifications

The proposed design automation program is also capable of designing $\Sigma\Delta$ modulators with different specifications. As an example, a new set of $\Sigma\Delta$ input specifications is listed in Figure 7.10. The circuit characteristics of this new design are listed in table 7.2.

7.6 Layout

The layout of the modulators can be generated from the same CAIRO program. As an example, the layouts of two integrators in two different technologies are shown in Figure 7.11 and Figure 7.12.

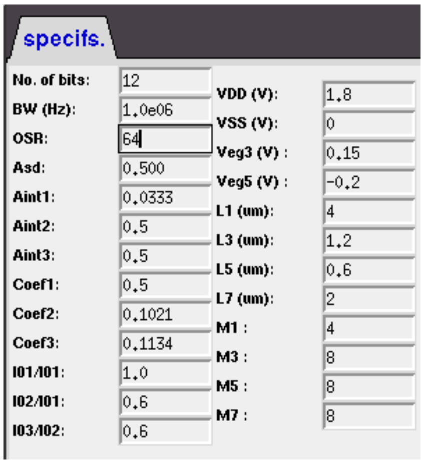

Figure 7.10: *Different specifications for the third order modulator, resolution = 12 bits, $BW = 1MHz$, $OSR = 64$.*

Table 7.2: *Circuit characteristics of the third order modulator, with the specifications described in Figure 7.10, designed using the design automation program.*

	Circuit III	Circuit IV
Technology Process	0.6μm	0.18μm
Supply Voltage	3.3 V	1.8 V
Modulation Index, m	0.7	0.7
1^{st} Integrator Capacitance, C_1	54 pF	225 pF
1^{st} Integrator Current, I_{0_1}	100μA	210μA
Power Consumption	4.5 mW	5.2 mW

They have been obtained with specifications given in Figure 7.3. The two integrators have the same floorplan since the CAIRO layout description uses the template approach [Dessouky00a].

7.7 Design Automation Tool Features

The main advantages of the presented tool may be summarized in the following:

- **Accuracy:** The generated transistors dimensions are very accurate and no fine-tuning is required. That is due to the fact that the circuit sizing tool uses the same equations as the

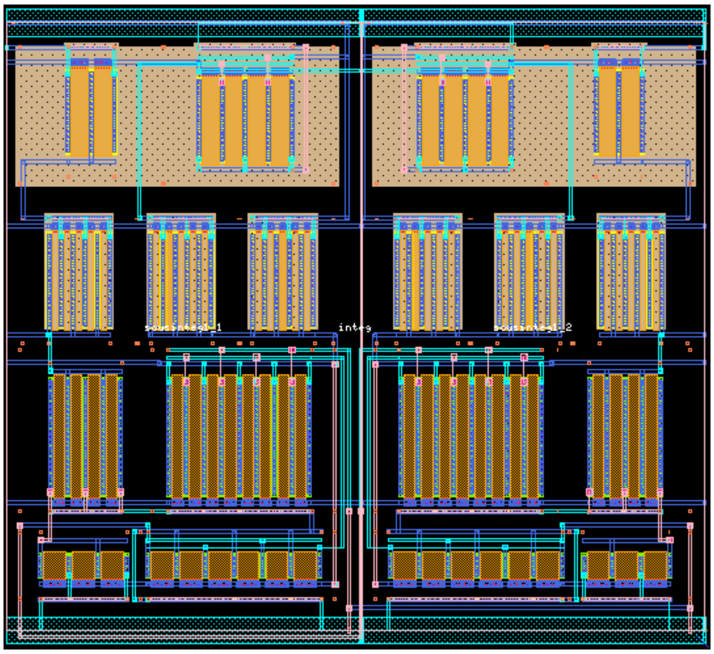

Figure 7.11: *Layout of the first integrator in the* $0.6\mu m$ *technology generated by the layout language CAIRO.*

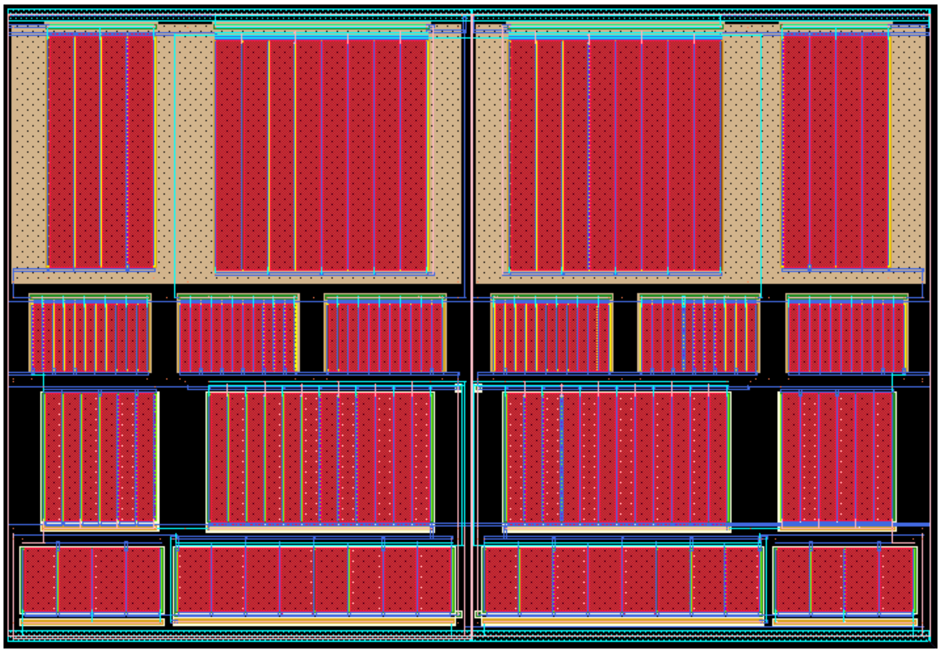

Figure 7.12: *Layout of the first integrator in the* $0.18\mu m$ *technology generated by the layout language CAIRO.*

SPICE-like circuit simulator.

- **Technology independence:** Design equations are defined in such a way to be technology independent. Circuits have been designed in several CMOS technologies ($0.6\mu m$, $0.35\mu m$, $0.25\mu m$ and $0.18\mu m$) with different supply voltages (from 3.3V to 1.5V).
- **Variation tolerance:** The tool was used to implement a 13-bit, 100kHz bandwidth modulator. Measurement results from 45 fabricated chips indicate that the design is robust.
- **Specifications range:** $\Sigma\Delta$ modulators with different signal bandwidths and resolutions (10-14 bits) have been designed.
- **Sizing Time:** A few seconds are required to design the complete $\Sigma\Delta$ modulator.
- **Design Expertise required:** Very little expertise is required to use the tool. A set of simulations is defined to guide the user to the necessary circuit performances that should be verified.
- **User Interaction:** a user friendly graphical interface is used to enter new specifications, modify circuit characteristics and simulate the resulting circuits.

The main drawbacks of the presented tool may be summarized in the following:

- **Generality:** Only the current-mode CT $\Sigma\Delta$ modulator design procedure is available.
- **Adding new design constraints:** The design procedure is optimized for minimum power consumption. Unless modifying the coded procedure, it is not possible to add new design constraints.

7.8 Conclusion

A systematic design method has been used to implement a design automation program for current-mode integrators for continuous-time $\Sigma\Delta$ modulators. Two third order modulators have been designed in different technologies. The circuits satisfy the required specifications of linearity and signal-to-noise ratio.

In this chapter, we have presented a top-down design automation tool for current-mode continuous-time $\Sigma\Delta$ modulators. The calculations of the biasing currents and voltages relies on a set of design equations derived from the simplified MOS transistor model. After biasing of the transistors is completed, the transistor sizing tool COMDIAC is used to calculate the width of each transistor. SPICE netlists are then generated for each block of the modulator.

The tool also permits to perform a set of SPICE simulations to verify the performance of the generated modulator. If the input specifications are satisfied, the layout of the circuit is generated using the layout language CAIRO.

The tool is accurate, rapid, technology independent, has large specification range and requires very little design experience to be used.

Chapter 8

Circuit Implementation and measurements results

8.1 Introduction

This chapter presents the prototype circuit implementation of a third-order current-mode continuous-time $\Sigma\Delta$ modulator based on the analysis and tools developed in the previous chapters.

First, the $\Sigma\Delta$ modulator architecture is described in section 8.2 Then the various circuits of the modulators are presented : the integrator in section 8.3, the feedback DAC in section 8.4, the comparator in section 8.5 and the reference circuit used to generate all the biasing currents and voltages of the modulator in section 8.6.

Measurements results are given in section 8.7. Comparison with some recent implementations is performed in section 8.8.

8.2 $\Sigma\Delta$ Architecture

A third order discrete-time $\Sigma\Delta$ modulator and its equivalent continuous-time modulator are shown in Figure 8.1 and 8.2 respectively. The DT-to-CT transformation method based on the modified-z-transform technique, described in chapter 4, is used to get the CT $\Sigma\Delta$ coefficients taking into account the RZ feedback signal. The discrete-time coefficients [Marques98] and their equivalent continuous-time coefficients [Aboushady99b] for a RZ feedback signal having a pulse

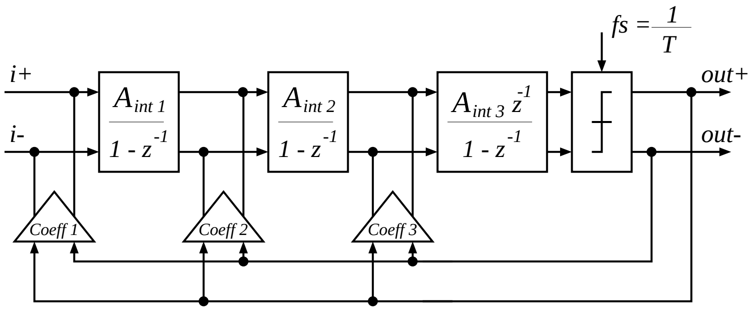

Figure 8.1: *Third-order discrete-time ΣΔ modulator.*

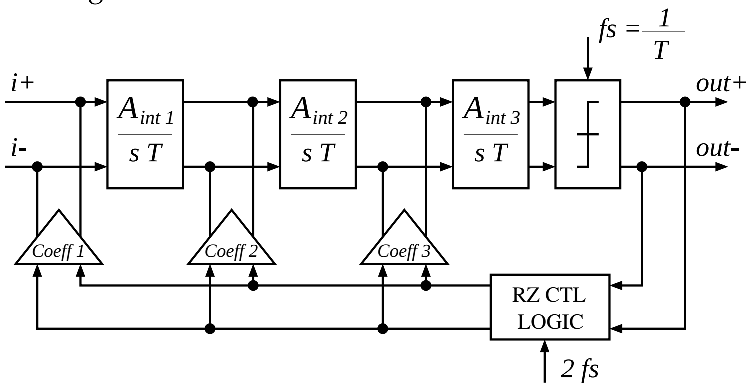

Figure 8.2: *Third-order continuous-time ΣΔ modulator.*

Table 8.1: *DT ΣΔ modulator and its RZ feedback CT equivalent ($t_d = \frac{T}{4}$ and $\tau = \frac{3T}{4}$).*

	A_{int_1}	A_{int_2}	A_{int_3}	Coeff$_1$	Coeff$_2$	Coeff$_3$
DT ΣΔ	0.20	0.50	0.50	1.00	1.00	1.00
CT ΣΔ	0.03	0.50	2.00	0.50	0.10	0.11

delay $t_d = \frac{T}{4}$ and a pulse width $\tau = \frac{3T}{4}$ are listed in table 8.1.

8.3 Integrator

Figure 8.3 shows the fully differential current-mode integrator. Operating at an oversampling ratio of 128, the quantization noise power of the modulator is sufficiently low to be masked by the circuit noise. Based on the thermal noise calculations, the biasing current of the first integrator is calculated such that the signal-to-thermal-noise ratio is 80dB for -6dB input signal.

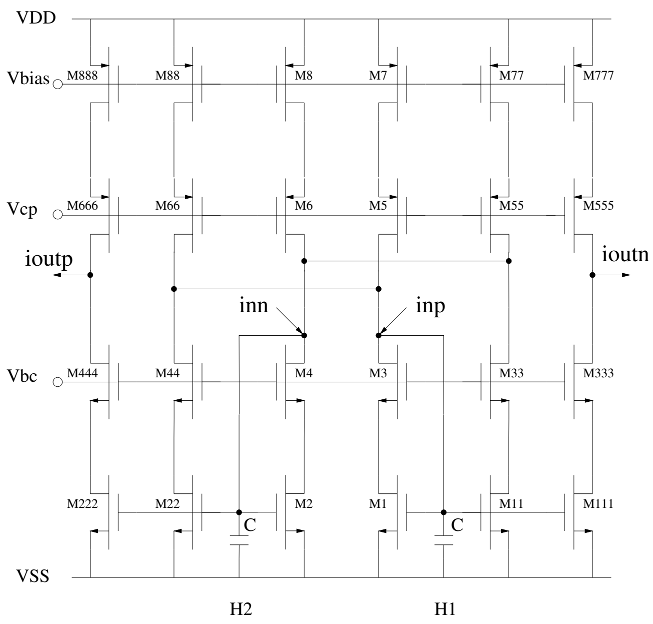

Figure 8.3: *The current-mode integrator.*

Table 8.2: *The integrator biasing voltages, biasing currents and integrating capacitances.*

V_{DD}	V_{CP}	V_{BC}	I_{0_1}	C_1	I_{0_2}	C_2	I_{0_3}	C_3
1.8V	0.6V	1.4V	$150\mu A$	794pF	$90\mu A$	26pF	$54\mu A$	1pF

The mirror transistors $M_1 - M_{111}$ and $M_2 - M_{222}$ have a fairly large length L in order to reduce the 1/f noise. This also applies to the biasing transistors, $M_7 - M_{777}$ and $M_8 - M_{888}$. The differential input voltage-to-current conversion is performed using two $48k\Omega$ resistors. The effect of these resistors on the input noise power is negligible.
Cascode biasing voltages V_{CP} and V_{BC} are calculated for maximum modulation index m of the current mirror. In this design, a modulation index of 0.7 is achieved.

As described in chapter 5, in order to reduce harmonic distortion due to g_m variation, the gain of the first integrator has to be small. In this design $A_{int1} = 0.03$ which leads, for a biasing current $I_{01} = 150\mu$ and a sampling frequency fs =26MHz, to an integrating capacitance $C_1 = 790pF$. This very large value is implemented using high-density polysilicon n-well capacitors [Pavan99]. Since, the nature of these capacitors is similar to transistors, it is expected that some of the matching errors would be eliminated in the integrator gain gm/C.

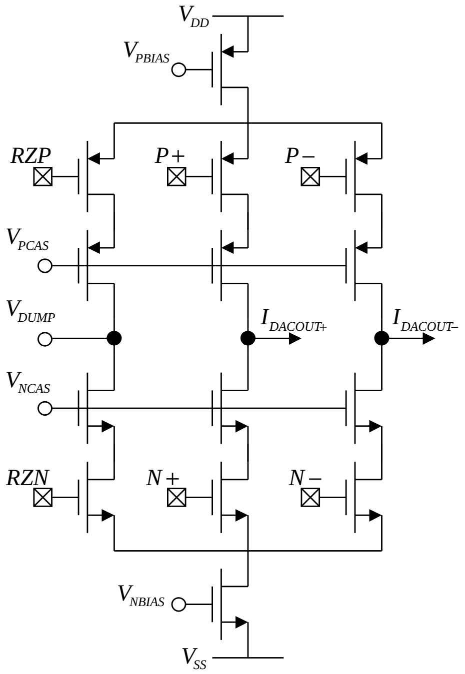

Figure 8.4: *RZ feedback DAC circuit.*

Table 8.3: *The DAC biasing voltages and biasing currents.*

V_{DD}	V_{PBIAS}	V_{NBIAS}	V_{PCAS}	V_{NCAS}	I_{DAC1}	I_{DAC2}	I_{DAC3}
1.8V	0.9V	0.9V	0.3V	1.4V	$52\mu A$	$10.6\mu A$	$11.8\mu A$

Since linearity and noise of the modulator are determined by the performance of the first integrator, the biasing current of the first integrator is large. In voltage-mode $\Sigma\Delta$ modulators, we usually significantly reduce the biasing current of the subsequent integrators [Zwan97]. Unfortunately in current-mode circuits the maximum signal swing, $m\ I_0$, is limited by the biasing current I_0. Significant reduction of the biasing current in the 2nd and 3rd integrators is not possible. Nevertheless, the fact that Aint1 is very small leads to a small signal swing, which permitted 40% reduction of the biasing current in the 2nd integrator and 64% reduction in the 3rd integrator.

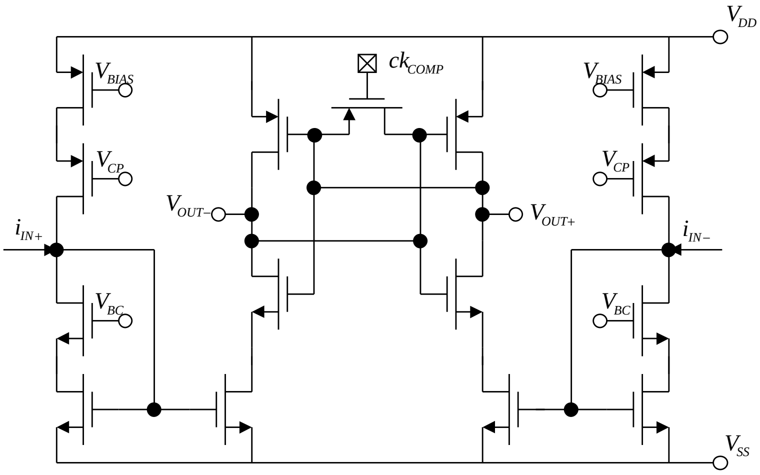

Figure 8.5: *Current-Mode Comparator*.

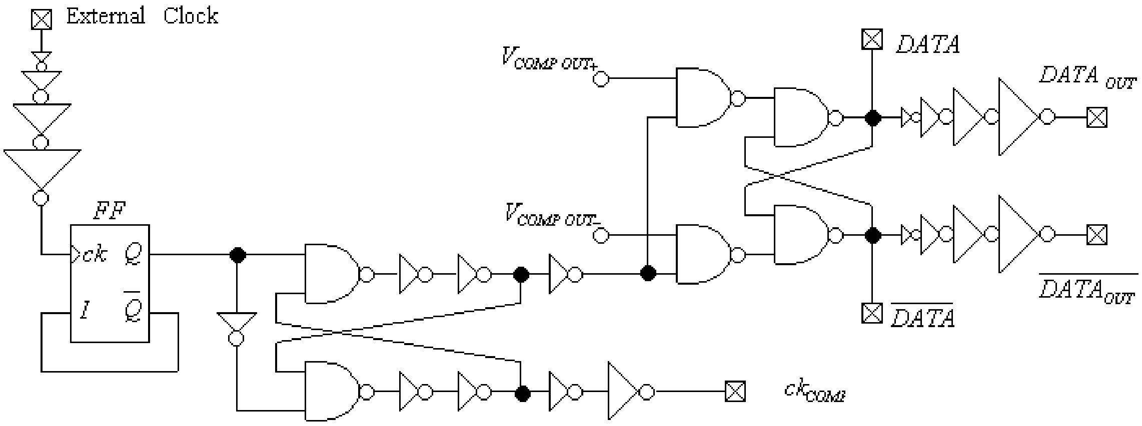

Figure 8.6: *Comparator latch and sampling clock*.

8.4 Feedback DAC

The practical issues concerning the design of the RZ feedback DAC circuit and its digital control circuitry have been described in detail in chapter 6. For the CT ΣΔ modulator coefficients listed in table 8.1 and taking into account the biasing current and the modulation index of the integrators, we calculate the value of the DAC current sources. These values along with the biasing voltages of the current sources and the switch cascode are listed in table 8.3.

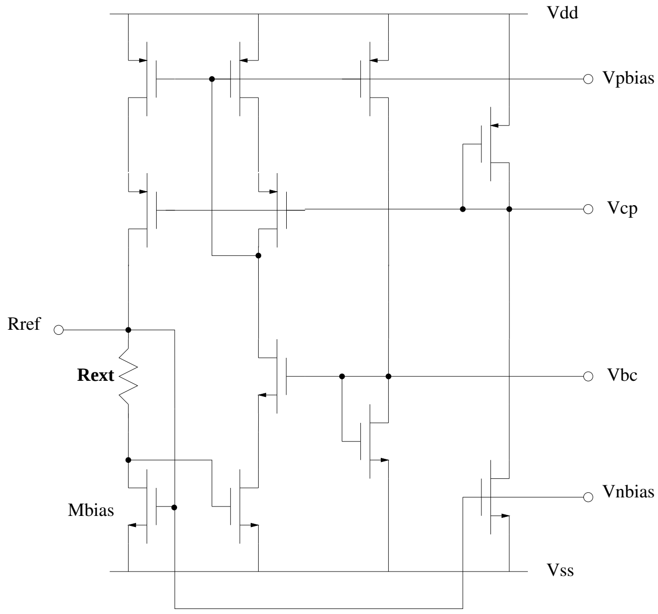

Figure 8.7: *Fixed transconductance bias.*

8.5 Comparator

The comparator circuit is depicted in Figure 8.5. This circuit is similar to the current-mode comparator presented in [Roeintan94]. At its inputs, current mirrors, biased with the same current as the 3rd integrator, copy the input signal to a clocked CMOS cross coupled latch.

The non-overlapping clock signal required for the sampling signal ck_{COMP} and the latch enable signal, responsible for the validation of the comparator output, is shown in figure 8.6.

8.6 Reference Circuit

The fixed transconductance biasing circuit, shown in Figure 8.7 [Pavan00], is used to generate all the biasing currents and voltages of the modulator. Using the simplified MOS transistor model, it can be shown that the transconductance of transistor M_{bias} is constant and process independent. It is maintained at $1/R_{ext}$, irrespective of any variation in threshold voltage, mobility or temperature. The biasing circuit requires only an external resistance of $5.75k\Omega$.

The circuit shown in Figure 8.7 can have a second state where all the currents are zero. In order to avoid this situation, a *start-up circuit* has been implemented [Johns97]. This circuit only affects the operation the constant-g_m biasing circuit if all the currents are zero at start-up.

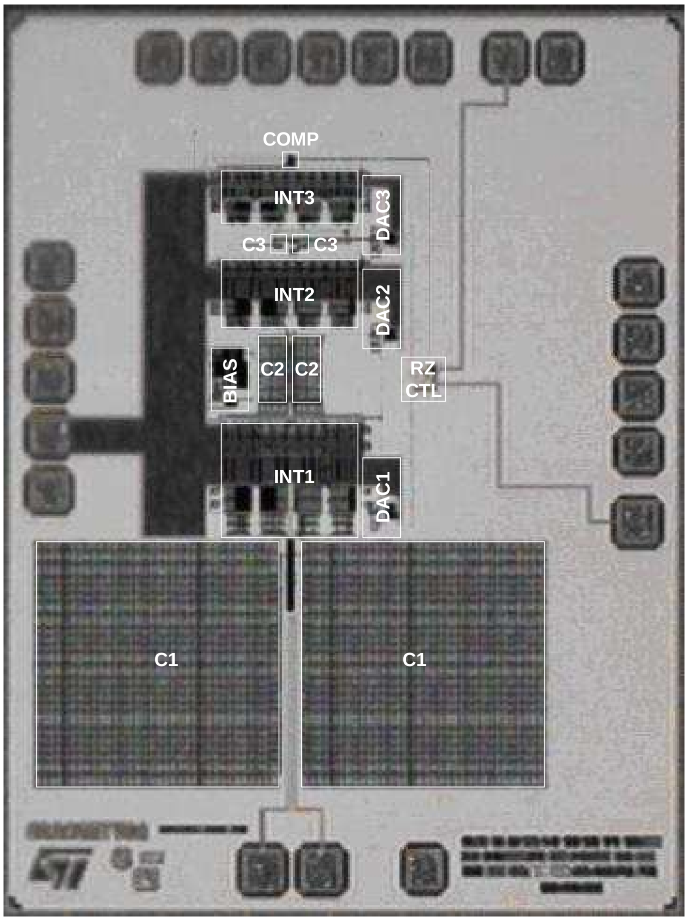

Figure 8.8: *Chip Micrograph/Layout*.

8.7 Measurements

The third-order modulator was fabricated in $0.18\mu m$ CMOS process[1]. The technology offers two types of transistors: Low Leakage MOS with high threshold voltage and High Speed MOS with a lower threshold voltage.

Since our aim is to offer a design for reuse methodology for standard low-cost CMOS technologies, we have chosen to work only with the Low Leakage MOS transistors.

A die-photo of the chip is shown in Figure 8.8. Note that the 2 capacitors of the first integrator (790pF each) occupy 33% of the active area of the complete circuit.

The circuit diagram of the test set-up as well as a photo of the printed circuit board are shown in Figures 8.9 and 8.10 respectively.

[1]Fabrication, test and measurements has been done in STMicroelectronics, Crolles, France.

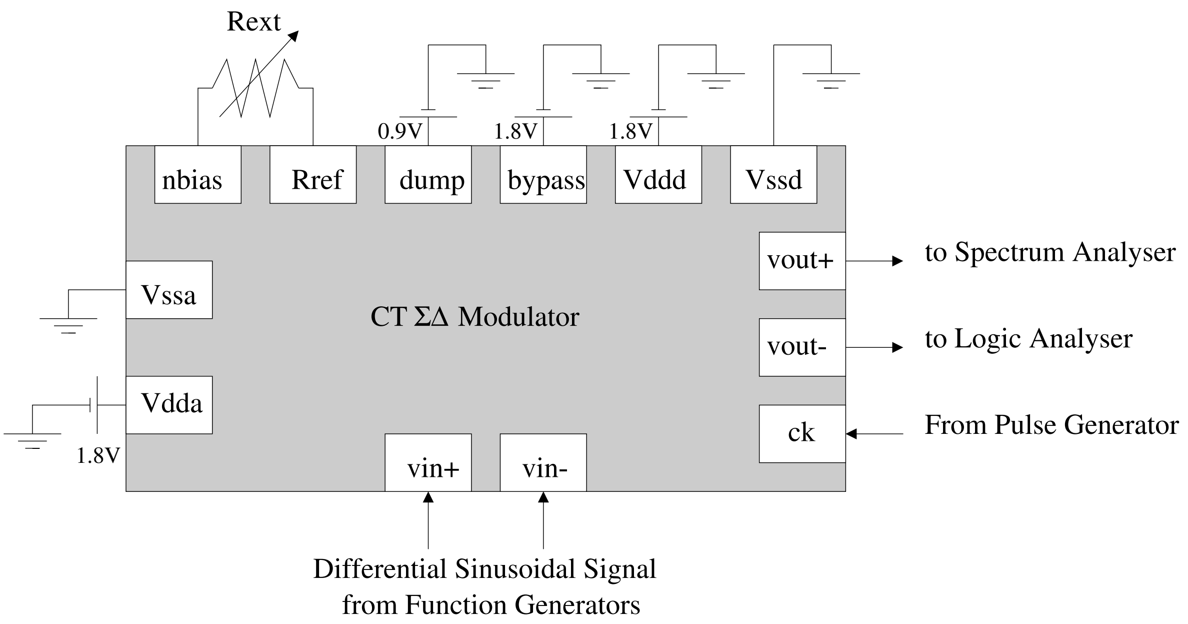

Figure 8.9: *Circuit Diagram of the test setup.*

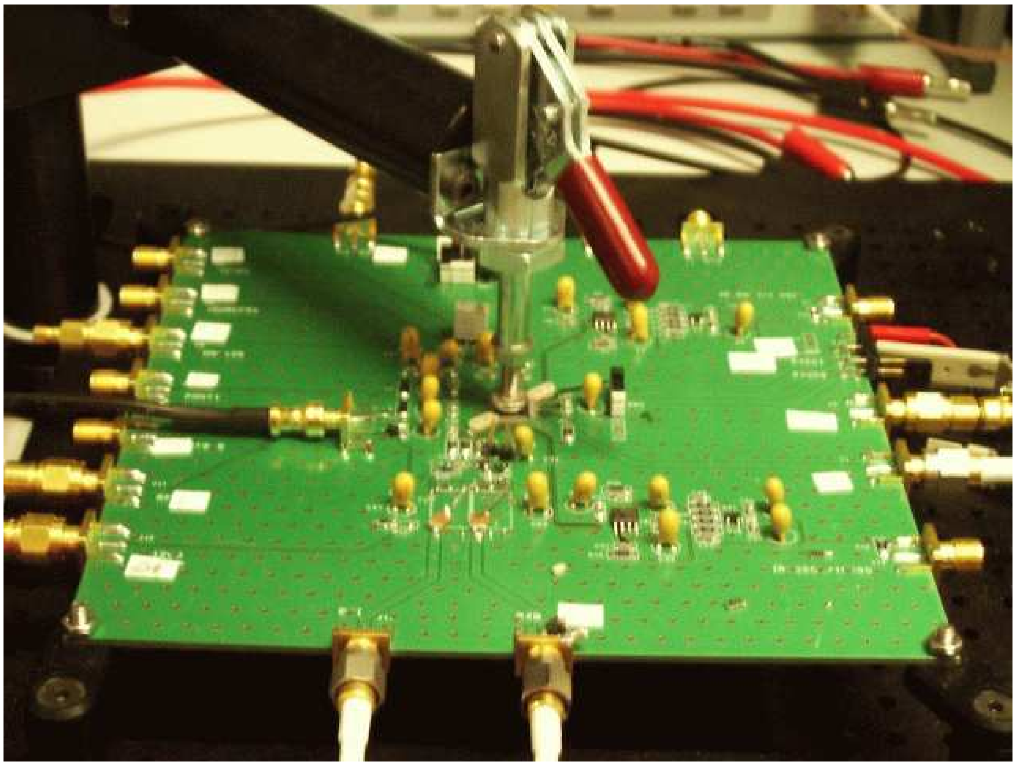

Figure 8.10: *Printed Circuit Board used for measurements.*

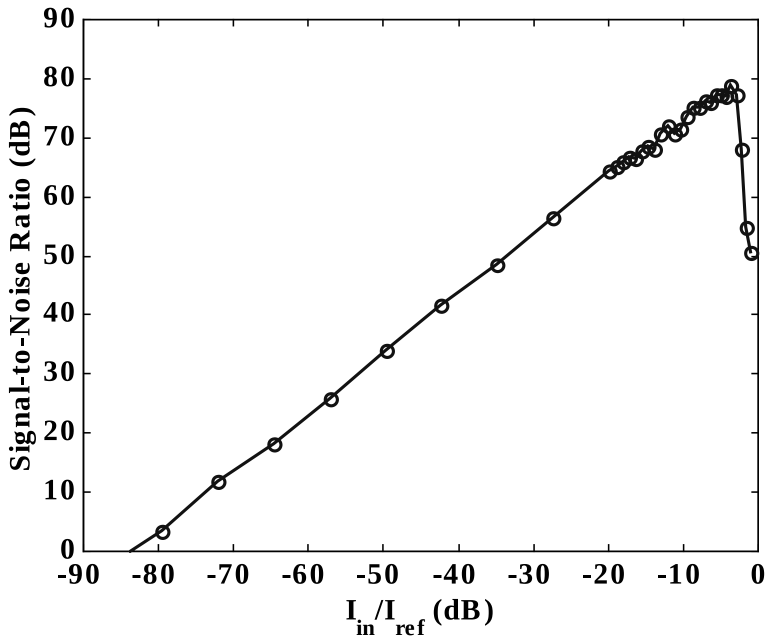

Figure 8.11: *Measured SNR.*

Table 8.4: *Performance summary.*

Dynamic Range	84 dB
SNR	79 dB
THD	-79 dB
Signal Bandwidth	100 kHz
Sampling Frequency	26 MHz
Oversampling Ratio	128
Power Consumption	5 mW
Supply Voltage	1.8 V
Active Area	1.2 x 1.3 mm^2
Technology	0.18 μm, 1PS, 6 AL, CMOS

The differential sinusoidal input signal was generated using two HP3325B synthesizer-function generators. In order to reduce jitter noise, a 1.6 GHz signal was generated using a ROHDE & SCHWARZ signal generator. This signal was then divide by 32 using the HP8133A pulse generator to obtain a ”clean” clock signal of $2 * f_s = 52$MHz required to generate on-chip the 26MHz sampling frequency and the $\frac{T}{4}/\frac{3T}{4}$ RZ feedback signal.

The output can either be directly viewed to a ROHDE & SCHWARZ spectrum analyzer or send to the HP16500C logic analyzer. The DATA collected from the logic analyzer can then be send to a PC in order to perform windowing, FFT and SNR calculations using LABVIEW.

Figure 8.11 shows the measured SNR in function of I_{in}/I_{ref}, where I_{ref} is defined as the maximum input current of the 1st integrator ($I_{ref} = mI_{01}$). When clocked at 26 MHz, the modulator achieves a dynamic range of 84dB and a peak SNR of 79dB. For a 25kHz input signal the THD is -79dB. The power consumption, including the biasing circuit, is 5mW at 1.8V supply. Key performance parameters are summarized in Table 8.4.

8.8 Performance Comparison

In table 8.5 we compare the circuit implemented in this work to other recently published CMOS CT and DT $\Sigma\Delta$ modulators having similar bandwidth specifications. The comparison is based on a definition of the Figure of Merit, FM, given in [Medeiro99]:

$$\text{FM} = \frac{\text{Power Consumption (W)}}{\text{Output Rate (Sample/second)} \quad 2^{\text{resolution (bit)}}} \quad 10^{12} \quad \text{(pJ)} \tag{8.1}$$

The Figure of Merit (FM) resulting from equation (8.1) is in pico-Joule (pJ) and represents the energy needed per conversion. The CMOS $\Sigma\Delta$ modulators are listed in table 8.5 in an ascending FM order. Compared to the other CT and DT SC implementations, only the circuit presented in [Breems00] achieves a lower FM than the circuit implemented in this work.
We can also note the following features compared to the other implementations:

- The first implementation of high performance current-mode CT $\Sigma\Delta$ modulator.
- For the given bandwidth specifications, it has the lowest supply voltage in standard CMOS technology.[2]
- High sampling frequency is achieved at low voltage supply.
- The current-mirror-based integrator structure is regular and well-suited to design automation.
- Large integrating capacitors resulted in high chip area.

[2]The circuit in [Matsuya94] is fabricated in a Multi-Threshold CMOS technology

Table 8.5: *Performance comparison of this work with other recently published $\Sigma\Delta$ modulators having similar bandwidth specifications.*

Reference	SNR (dB)	BW (kHz)	f_s (MHz)	V_{DD} V	Power (mW)	Area (mm^2)	CMOS Process	Architecture	FM (pJ)
[Breems00]	82	100	13	2.5	1.8	0.2	0.35μm	4^{th} order RC, Gm-C	0.7
This Work	**79**	**100**	**26**	**1.8**	**5**	**1.56**	**0.18**μm	3^{rd} **order Gm-C**	**2.7**
[Yin93]	93	160	20.48	5.0	65	1.6	1.2μm	2-1 MASH SC	4.4
[Nagari00]	66	100	13	2.7	2.0	0.18	0.5μm	2^{nd} order SC	4.9
[Matsuya94]	58	192	6	1.0	1.56	2.5	0.5μm	2^{nd} order RC	5.0
[Dedic94]	90	100	3.25	5.0	40.0	2.0	1.2μm	2-2-2 MASH SC	6.1
[Yasuda98]	79	100	5	2.7	14.8	5.4	0.6μm	3-bit, 2^{nd} order SC	8.0
[Rebeschini90]	91	80	10.24	5.0	76.0	3.0	1.5μm	1-1-1 MASH SC	13
[Comino91]	54	72	20	5.0	3.0	0.9	2.0μm	1^{st} order Gm-C	40
[Minogue95]	68	100	13	5.0	94.0	-	0.8μm	7^{th} order SC	182

8.9 Conclusion

In this chapter, the implementation of a 13-bit, 100 kHz bandwidth, $\Sigma\Delta$ modulator, consuming 5 mW at 1.8V, has been presented.

High density polysilicon n-well capacitors are used to implement the large integrating capacitors of the first integrator. All the biasing currents and voltages of the integrator, comparator and DAC were generated using a fixed-transconductance reference circuit.

Measurement results from silicon implementation matched the expected performances and circuit characteristics given. This validates our design procedures and the circuit synthesis tool developed throughout the previous chapters.

Performance comparison of this work with other recently published $\Sigma\Delta$ modulators having similar bandwidth specifications, shows that the presented third order current-mode continuous-time $\Sigma\Delta$ modulator has good performances. This indicates that current-mode CT $\Sigma\Delta$ may have interesting performances in recent and future low voltage standard CMOS technologies.

Chapter 9

Decimation Filter

9.1 Introduction

In this chapter, a power efficient multi-rate multi-stage Comb decimation filter for mono-bit and multi-bit $\Sigma\Delta$ A/D converters is presented. Polyphase decomposition in all stages, with high decimation factor in the first stage as proposed in section 9.3, is used to significantly reduce the sampling frequency of the Comb filter in comparison with other approaches presented in section 9.2. Several implementations, discussed in section 9.4, indicate that proper choice of the first stage decimation factor can considerably improve power consumption, area and maximum sampling frequency, as illustrated by the results of section 9.5. In multibit $\Sigma\Delta$ A/Ds, this optimum first stage decimation factor is f unction of the input word length (section 9.5).

9.2 Performance of Existing Designs

Power consumption of decimation filters in $\Sigma\Delta$ A/D converters is receiving increasing attention [Pan00][Maulik00][Gao00]. Comb filters, shown in Fig. 9.1(a), are widely used in the decimation filter of $\Sigma\Delta$ A/D converters. These filters operate at maximum sampling frequency before any decimation takes place. The power consumption of Comb filters is then very high [Barrett97] [Aboushady97]. The transfer function $H(z)$ of a Comb filter of order k and for a decimation ratio M is defined by

$$H(z) = \left(\frac{1 - z^{-M}}{1 - z^{-1}}\right)^k . \tag{9.1}$$

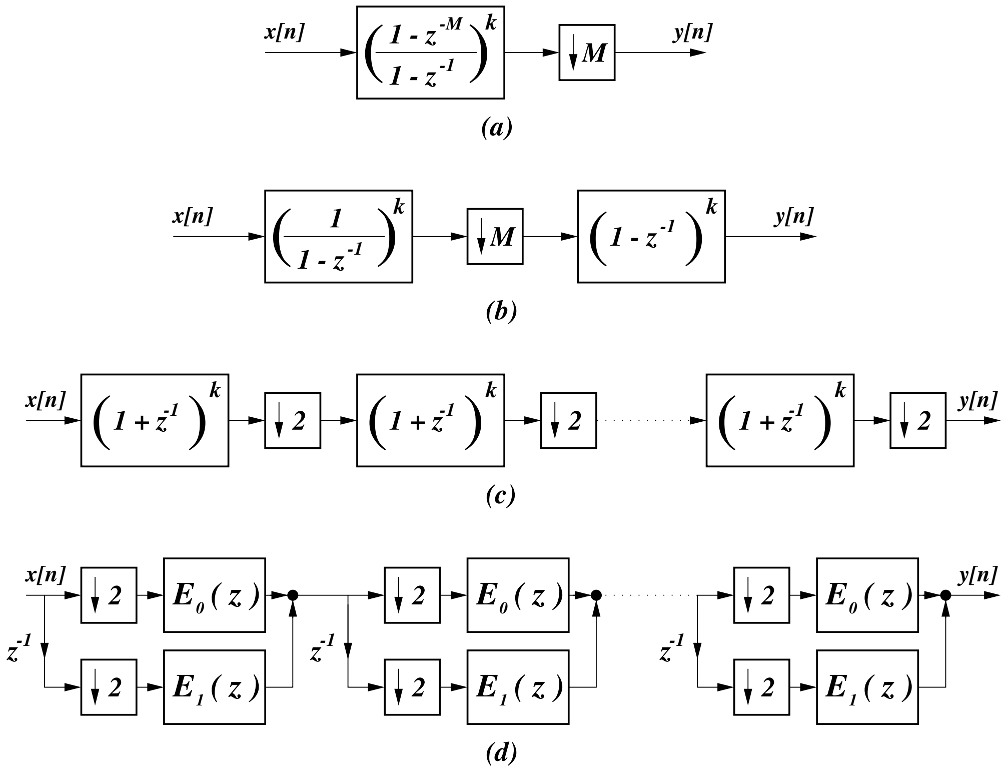

Figure 9.1: *(a) Comb filter. (b) IIR-FIR implementation. (c) FIR2: cascade of FIR filters each decimating by 2. (d) POLY-FIR2: Polyphase decomposition applied to FIR2. .*

These filters were usually implemented using the IIR-FIR technique [Dijkstra88], Fig.9.1(b). Recently lower power consumption has been achieved using the FIR2 [Gao00], and the POLY-FIR2 [Gao99], implementations, shown in Fig.9.1(c) and Fig.9.1(d) respectively.

In the IIR-FIR structure, shown in Fig.9.1(b), the FIR filter, $(1 - z^{-1})^k$, operates at a sampling frequency M times lower than the IIR filter, $(\frac{1}{1-z^{-1}})^k$. In order to avoid register overflow in the IIR filter, the word length of the IIR filter has to be equal to $(W_0 + k\, log_2 M)$ bits [Hogenauer81], where W_0 is the number of bits at the filter input. The major drawback of this architecture is that the IIR filter is operating at maximum sampling frequency and with a very large word length. Equation (9.1) can be written in the following form:

$$H(z) = \prod_{i=0}^{(log_2 M)-1} \left(1 + z^{-2^i}\right)^k . \tag{9.2}$$

Applying the commutative rule [Chu84], we get the FIR2 structure shown in Fig.9.1(c). In this structure, the Comb filter is realized by cascading $log_2 M$ identical FIR filters, $(1 + z^{-1})^k$, each dec-

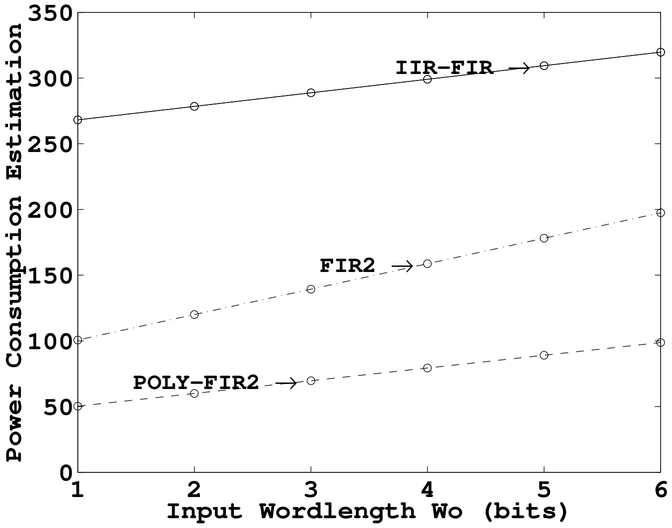

Figure 9.2: *Power consumption estimation for different implementations of a* 5^{th} *order Comb filter with a decimation factor of* 32 *(*$k = 5$ *and* $M = 32$*).* .

imating by 2. The POLY-FIR2 structure [Gao99], illustrated in Fig.9.1(d), is obtained by applying Polyphase decomposition [Bellanger76], to the FIR2 structure. In this case, the decimation occurs at the input of each filter, thus reducing by 2 the sampling frequency of each stage. The FIR2 and the POLY-FIR2 structures have the advantage of not having any register overflow problems and the word length of each stage i is limited to $(W_0 + k\ i)$ bits.

The average power consumption of a digital signal processing system is proportional to: the number of operations performed per sample, the word length and the sampling frequency. In Comb filters, we will assume that the number of operations is equal to the number of partial products to be added. The power consumption, P, can then be defined by the following relation:

$$P = \sum_{i=1}^{l} \frac{NP_i * W_i}{\prod_{j=1}^{i} M_j} \tag{9.3}$$

where NP_i is the number of 1-bit partial products to be added in stage i, W_i the input word length of stage i, M_j the decimation factor in stage j and l the total number of decimation stages.
Equation (9.3) is used to compare the power consumption for different implementations of a 5^{th} order Comb filter, with a decimation factor of 32. Fig.9.2 shows that power consumption of POLY-FIR2 is significantly lower than the two other techniques. All three implementations have the same number of partial product per stage ($NP_i = 10$) [Dumonteix00a]. The very large word length in the first stage of the IIR-FIR technique ($W_i = W_0 + 25$), is the reason behind its considerably

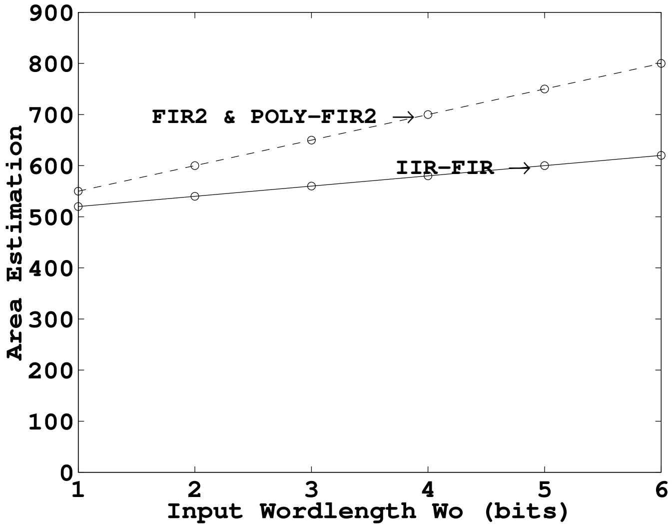

Figure 9.3: *Area estimation for different implementations of a* 5^{th} *order Comb filter with a decimation factor of* 32 *(*$k = 5$ *and* $M = 32$*). .*

higher power consumption. POLY-FIR2 requires exactly the same hardware as FIR2, but operates at half the sampling frequency. An equation similar to (9.3) can be deduced to estimate the area of the circuit. We assume that the hardware required to add the multiplication partial products is dominant. The area, A, can then be defined as

$$A = \sum_{i=1}^{l} NP_i * W_i. \tag{9.4}$$

From Fig.9.3, we can see that the IIR-FIR technique occupies less area than the FIR2 and POLY-FIR2 techniques.

In the next section, we will introduce a different architecture that reduces power consumption and area, especially for low input word length.

9.3 Proposed Comb Filter Architecture

As shown in Fig.9.4(a), we propose to decompose the Comb decimation filter into a first stage FIR filter $H_1(z)$ with a decimation factor M_1, followed by a cascade of FIR $(1 + z^{-1})^k$ filters with a decimation factor 2. The reason behind choosing this representation is that we would like to decimate as much as possible in the first stage. The following stages are kept with the minimum decimation ratio 2 because, when the word length of the input signal is high, reducing the sampling frequency

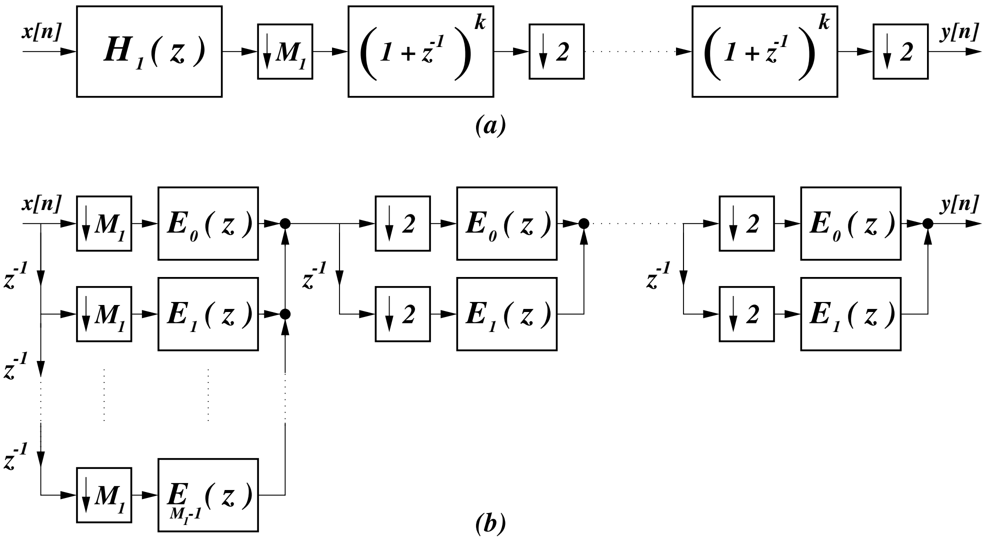

Figure 9.4: *(a) Cascade of FIR with high decimation factor M_1 in the 1st stage. (b) Polyphase decomposition of the 1st stage filter $H_1(z)$ decimating by M_1 and the subsequent filters decimating by* 2..

does not compensate for the added complexity of the Polyphase decomposition. In the following, we will explain how Polyphase decomposition is applied to Comb decimation filters. Equation (9.1) can be written in the following form:

$$H(z) = H_1(z)\ \ H_2(z) \tag{9.5}$$

where,

$$H_1(z) = \left(\sum_{i=0}^{M_1-1} z^{-i}\right)^k \tag{9.6}$$

$$H_2(z) = \prod_{i=0}^{(log_2 \frac{M}{M_1})-1} \left(1+z^{-2^i}\right)^k . \tag{9.7}$$

The expansion of $H_1(z)$ results in an FIR filter of order $k(M_1-1)$

$$H_1(z) = \sum_{n=0}^{k(M_1-1)} h(n) z^{-n}. \tag{9.8}$$

The coefficients of this filter are integers and symmetrical $h(n) = h(N-1-n)$, where $N = k(M_1-1)$. Applying Polyphase decomposition on the filter of equation (9.8), we get

$$\begin{aligned} H_1(z) &= \sum_{n=0}^{k(M_1-1)} h(nM_1) z^{-nM_1} \\ &= z^{-1} \sum_{n=0}^{k(M_1-1)} h(nM_1+1) z^{-nM_1} \\ &\vdots \\ &= z^{-(M_1-1)} \sum_{n=0}^{k(M_1-1)} h(nM_1+M_1-1) z^{-nM_1}. \end{aligned} \tag{9.9}$$

Efficient Polyphase implementation of $H_1(z)$ is shown in Fig.9.4(b). As we can see, decimation takes place before filtering, so multiplications and additions are performed at a sampling frequency M_1 times lower than the frequency of the input signal. The subsequent filters decimating by 2 are nothing but a special case of the general case described above.

Higher values of M_1 will significantly reduce the sampling frequency of the first stage which can be interesting for power consumption. On the other hand, we can see from equation (9.6) that higher values of M_1 will increase the order of the filter $H_1(z)$, which implies more complex coefficients and a higher number of partial products. Note also that the word length of the polyphase filter will increase since it is equal to $(W_0 + k\ log_2 M_1)$ bits.

In order to find the decimation factor M_1 that achieves minimum power consumption, several implementations with different values for M_1 have been implemented and are presented in the following sections.

9.4 Filter Implementation

The choice of the FIR architecture to implement the polyphase filters has an important impact on power consumption. FIR filters are implemented either in a transposed-form or a direct-form. Each of these two forms has one main drawback. The transposed-form requires larger word length for the intermediate registers, which can increase power consumption. The direct-form has a long critical path which limits the maximum sampling frequency of the filter. Since the use of Polyphase decomposition has highly reduced the operating frequency of the filter, the critical path is no longer a problem. Thus we have chosen the direct-form implementation.

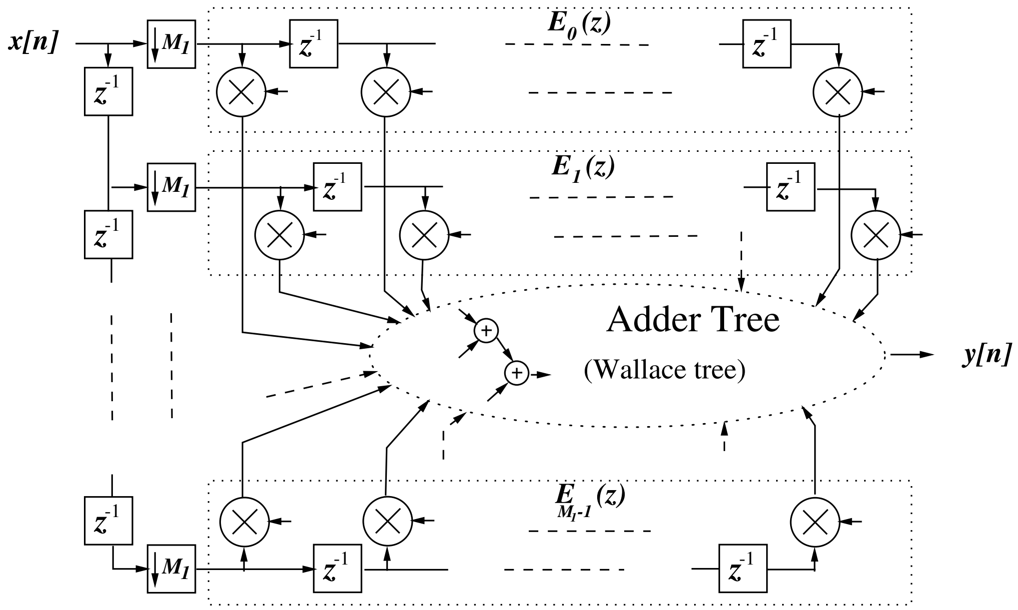

Figure 9.5: *Direct-form implementation of one stage of the Comb filter using one adder-tree.* .

Table 9.1: NP_1 *for all values of* M_1 *(*5^{th} *order Comb)..*

M_1	2	4	8	16	32
NP_1	10	41	139	346	919

Fig.9.5 shows the general architecture for one stage of the comb decimation filter. All the subfilters, E_0, E_1, ..., E_{M_1-1}, resulting from the polyphase decomposition are operating at the same sampling frequency. One way of reducing the required hardware is to gather all additions from the different subfilters into one adder tree. This adder tree is also employed in the multipliers to sum all the partial products. In fact, partial products resulting from different multiplications is gathered with the addition operations in the same adder tree. The Wallace tree [Muller97] is an efficient realization of the adder tree. This technique is usually used in the implementation of high speed multipliers [Muller97][Dumonteix00b]. Note that we have only one Wallace tree for the complete polyphase filter. This has significantly reduced the overall power consumption.

9.5 Performance Evaluation

To study the effect of the decimation factor of the first stage M_1 on the overall performance of the circuit, several 5^{th} order Comb filters, with a total decimation factor M of 32 have been designed. Each filter had: a different decimation factor in the first stage ($M_1 = 2, 4, 8, 16, 32$), and a different input word length ($W_0 = 1, 2, 3, 4, 5, 6$bits). These filters use the proposed system architecture described in section 9.3 and with the implementation described in section 9.4. Table 9.1 lists the number of partial products NP_1 for all possible decimation factors M_1 [Dumonteix00a]. Three criteria have been chosen for evaluation: power consumption, area and maximum sampling frequency. Power consumption and area are estimated using equation (9.3) and (9.4) respectively. The maximum operating frequency, F_{max}, can be estimated by

$$F_{max} = 1 / \underset{i \in \{1,\ldots,l\}}{Max} \left(\frac{log_2(NP_i * W_i)}{\prod_{j=1}^{i} M_j} \right) \tag{9.10}$$

where $log_2(NP_i * W_i)$ is the number of combinational logic layers necessary to sum the partial products of stage i.

The estimated circuit performances, based on equations (9.3), (9.4) and (9.10), are shown in Fig.9.6. The circuits have been designed in a standard low-cost $0.35\mu m$ technology. Simulation results from the designed circuits are shown in Fig.9.7. Power consumption is estimated using a probabilistic simulation program [Dunoyer99]. The area is estimated from the layout and the maximum operating frequency is estimated using a timing analysis tool [Dioury99]. Comparing Fig.9.6 and Fig.9.7, we see that equation-based estimations are very close to the simulation results.

Analyzing these figures, we can see that, for mono-bit $\Sigma\Delta$, minimum power consumption and area are achieved for a decimation factor $M_1 = 16$. The worst performances are obtained when $M_1 = 2$, which is in fact nothing but the POLY-FIR2 structure. Comparing the two implementations for $M_1 = 16$ and $M_1 = 2$: the power consumption is reduced by 30%, the area is reduced by 20%, and the maximum sampling frequency is 5 times higher. In fact, the sampling frequency is limited by the intrinsic propagation delay of the D Flip-Flop.

For multi-bit (6-bit) $\Sigma\Delta$, minimum power consumption and area are achieved for a decimation factor $M_1 = 2$ and $M_1 = 4$. Since higher frequency of operation can be achieved with $M_1 = 4$, the implementation with $M_1 = 4$ is more interesting. In general, for multi-bit $\Sigma\Delta$, we can see that, as the number of bits at the input of the Comb filter decreases, the proposed architecture becomes more interesting.

Polyphase Comb filters of 3^{rd} and 4^{th} order, for mono-bit $\Sigma\Delta$ modulators, have also been designed. The simulation results of these filters along with the 5^{th} order filter are shown in Fig.9.8. We can see that, the proposed Comb filter architecture gives similar results for different orders of the Comb filter.

Although the main purpose from the Polyphase Comb filter architecture was to achieve low-power consumption, significant improvements regarding area and maximum sampling frequency have also been obtained.

9.6 Conclusion

Low-power implementations of a Comb decimation filter for mono-bit and multi-bit $\Sigma\Delta$ A/D converters have been presented. A multi-stage polyphase structure with maximum decimation factor in the first stage has been used. The proper choice of this first stage decimation factor can significantly improve power consumption, area and maximum sampling frequency. In order to find this optimum first stage decimation factor, simple equations have been developed to estimate circuit performances of the proposed architecture. Gathering all the partial products additions into one adder tree has also considerably reduced the required hardware for the circuit.

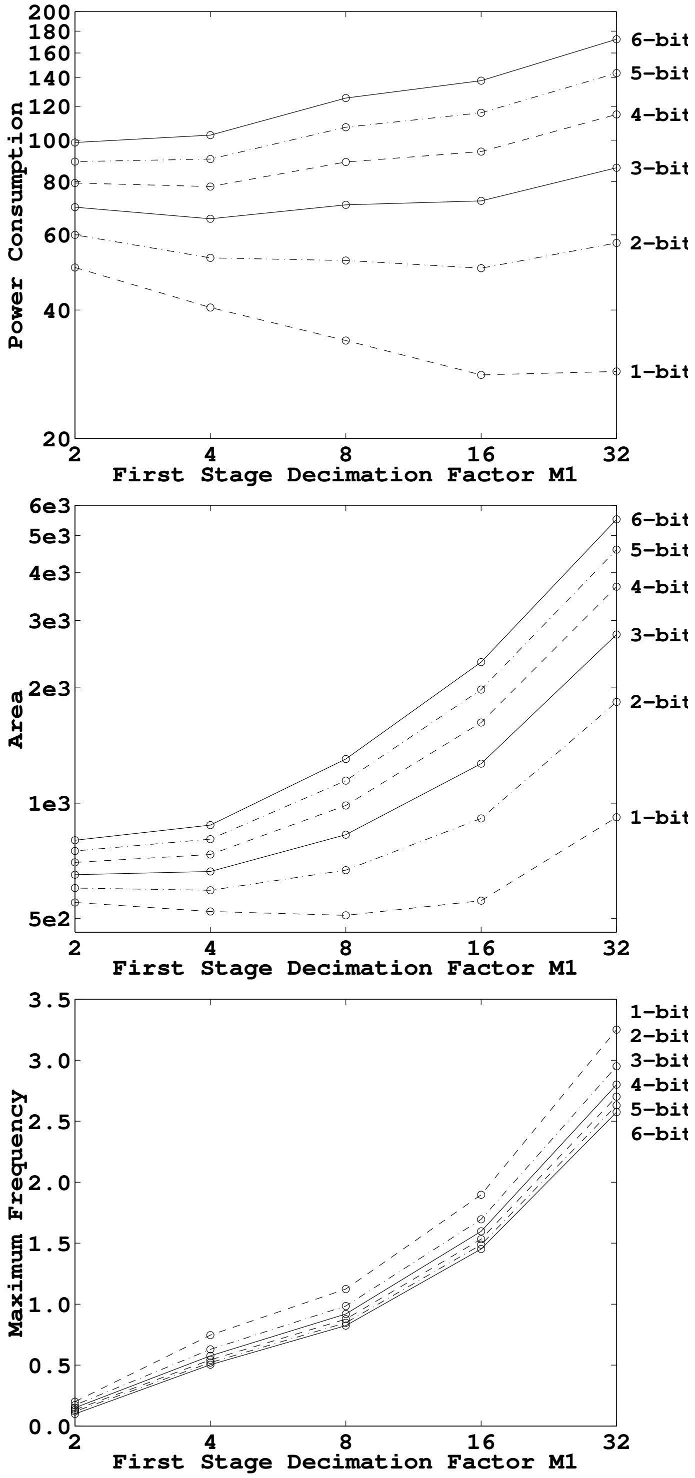

Figure 9.6: *Calculation of Polyphase Comb filters for mono-bit and multi-bit* $\Sigma\Delta$ *modulators. Performances are calculated using equations 9.3, 9.4 and 9.10..*

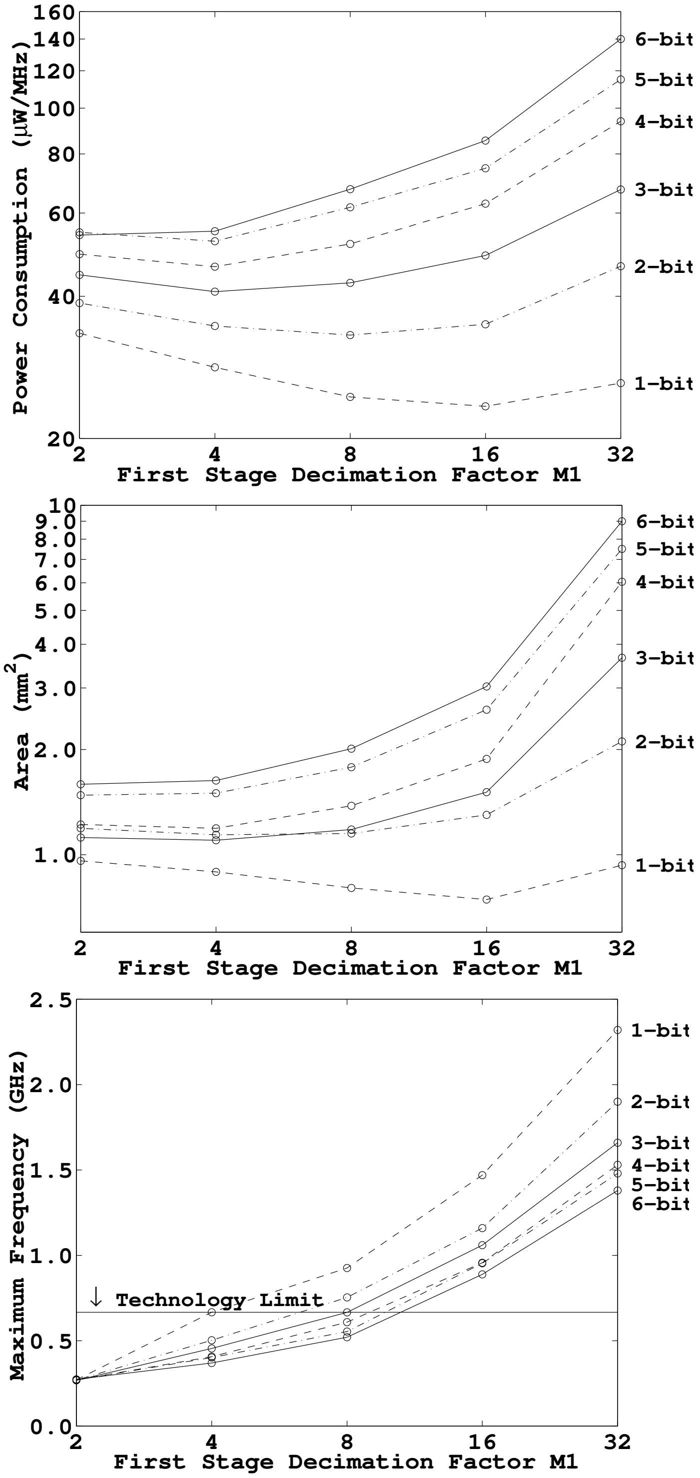

Figure 9.7: *Simulation results of the Polyphase Comb filters for mono-bit and multi-bit $\Sigma\Delta$ modulators. The circuits are designed in a $0.35\mu m$ technology..*

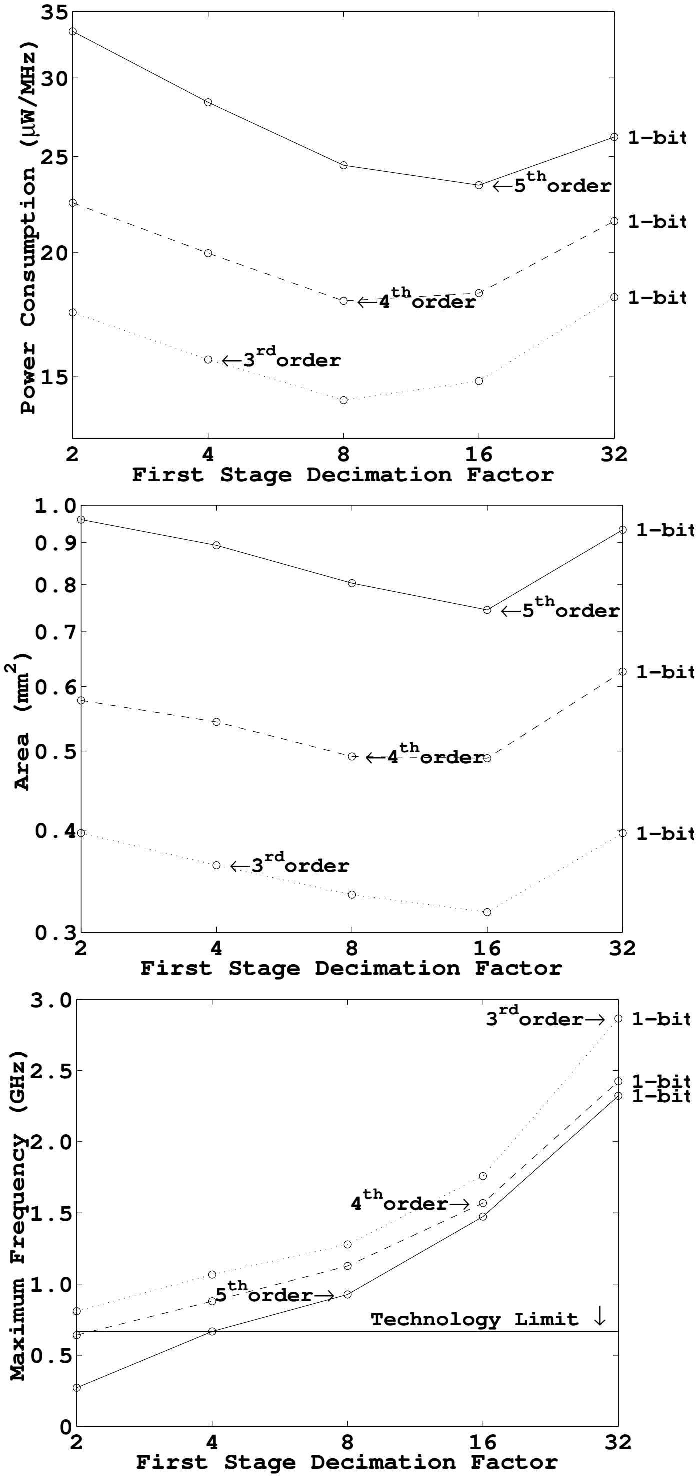

Figure 9.8: *Simulation results of* 3^{rd}, 4^{th} *and* 5^{th} *order Polyphase Comb filters for mono-bit* $\Sigma\Delta$ *modulators. The circuits are designed in a* $0.35\mu m$ *technology..*

Chapter 10

Conclusion

10.1 Research Overview

In this work, several design aspects of CT $\Sigma\Delta$ have been tackled:

System Level Design of Continuous-Time $\Sigma\Delta$

A systematic design approach for DT-to-CT transformation of $\Sigma\Delta$ modulators based on the modified-z-transform technique has been proposed. The proposed technique is general and well-suited to design automation. This technique permits us to take advantage of the already mature and well-established DT $\Sigma\Delta$ modulators. The design technique has been implemented in a symbolic mathematical tool. This tool have been used to generate correspondance tables between CT and DT $\Sigma\Delta$ modulators. It is now possible to get the CT coefficients of an n^{th} order $\Sigma\Delta$ modulators in function of the DT coefficients and the characteristics of the CT feedback DAC. Several high order lowpass and bandpass CT $\Sigma\Delta$ modulators have been designed using this tool. Simulation results show that the DT $\Sigma\Delta$ and its calculated CT equivalent have the same performances. It has also been observed that, for lowpass $\Sigma\Delta$ modulators, DT coefficients might have been directly used in a CT modulator. The DT-to-CT transformation calculations are essential for bandpass $\Sigma\Delta$ modulators.

Circuit Level Design of Continuous-Time $\Sigma\Delta$

A low-power high linearity design procedure for cascode current mirror based integrator is proposed. It has been shown that there is an optimum supply voltage for minimum power consumption. A method has also been described to increase the linearity of the CT integrator only by increasing its integrating capacitance and without increasing its power consumption. These are interesting results that support claims that current-mode circuits are adapted to operate efficiently at low-voltage supply.

Design Automation of Continuous-Time $\Sigma\Delta$

A top-down design automation tool for current-mode CT $\Sigma\Delta$ modulators has been presented. Starting from the $\Sigma\Delta$ system specifications (SNR, THD, BW, ...) and a few circuit characteristics, we generate the complete netlists of the $\Sigma\Delta$ modulator including the integrator, the comparator and the DAC. This tool has been implemented in the COMDIAC environment. The main features of this tool is accuracy, technology independence, large input specification range and rapid sizing. Furthermore, very little design expertise is required to use the tool.

Circuit Implementation

A 3rd order current-mode CT $\Sigma\Delta$ has been implemented in $0.18\mu m$ standard CMOS process. The coefficients of the modulator were calculated using the modified-z-transform technique and then scaled according to the value of A_{int_1} achieving the required linearity. The integrator circuit was designed using the method described in chapter 5 and implemented in the design automation tool described chapter 7. The 13-bit, 100 kHz bandwidth, $\Sigma\Delta$ modulator consumes 5 mW at 1.8V. When compared with other recently reported $\Sigma\Delta$ modulators having similar bandwidth specifications, the measured circuit has a better Figure of Merit than all DT modulators and most CT modulators.

Digital Decimation Filters

Predicting higher sampling frequencies to $\Sigma\Delta$ modulators thanks to the CT technique, higher power consumption is expected in the digital decimation filter. In order to reduce its power consumption, we propose to use a multi-rate multi-stage Comb decimation filter. Polyphase decomposition in all stages, with high decimation factor in the first stage, is used to significantly reduce the sampling frequency. It is shown, by theoretical analysis and simulations, that proper choice of the first stage decimation factor can considerably improve power consumption, area and maximum sampling frequency. Both mono-bit and multi-bit $\Sigma\Delta$ have been studied. In multi-bit A/D, the optimum first stage decimation factor is function of the input wordlength.

10.2 Future Work

Several research points seem interesting to investigate:

System Level Design of Continuous-Time $\Sigma\Delta$

- **Model different shapes of feedback signals:** Designing CT $\Sigma\Delta$ modulators with non-rectangular feedback shapes could be useful to compensate non-idealities in a rectangular feedback signal by modifying the coefficients of the modulator. On the other hand, the shape of the feedback signal can be intentionally modified to reduce clock jitter (chapter 6).
- **CT $\Sigma\Delta$ Simulation Toolbox:** Such a toolbox is needed for rapid simulation of CT $\Sigma\Delta$ non-ideal circuit behavior: non-linearity of the integrator, clock jitter, loop delay and feedback waveform asymmetry. Automatic scaling of the CT $\Sigma\Delta$ coefficients either for maximum output swing or according to a given fixed value of A_{int_1} should also be possible.

Circuit Level Design of Continuous-Time $\Sigma\Delta$

- **Linearization techniques:** The main drawback of the presented circuit is its large area due to the very large values of the first integrating capacitance. This capacitance is excessively high in order to improve the linearity of the first integrator. Linearization techniques, like source degeneration, could be used to improve linearity and consequently reduce the integrating capacitance.
- **Higher bandwidth and sampling frequency:** Classical specifications have been used for the implemented prototype circuit presented in chapter 8. The main reason we were reluctant to design the circuit for more *"agressive"* specifications is that no implementation of current-mirror based CT $\Sigma\Delta$ modulator has ever been reported, so a first *"simple"* implementation

was necessary to validate the design concepts developed in this work. The next step would be to implement another current-mode CT $\Sigma\Delta$ modulator for higher bandwidth and sampling frequency in order to fully exploit its capabilities. In this case, the main limitation to the maximum achievable sampling frequency is expected to be clock jitter noise.

Implementation of a bandpass $\Sigma\Delta$ modulator using the design techniques developed in this work is also an interesting future work.

- **Multibit CT $\Sigma\Delta$:** Sensitivity to clock jitter can be significantly reduced in CT $\Sigma\Delta$ modulators by using a NRZ multi-bit feedback DAC (chapter 6). In this case, problems related to loop delay and waveform asymmetry may upsurge. Furthermore, a linearization technique has to be used to reduce harmonic distortion due to DAC elements mismatch.

- **Conventional Gm-C versus current-mode Gm-C:** A design procedure, similar to the one presented in this work for current-mirror based integrators, should be developed for conventional differential-pair based Gm-C integrators. This would allow us to compare the two techniques to point out the advantages and drawbacks of each technique.

Appendix A

Tables of Discrete-Time and Continuous-Time $\Sigma\Delta$ Coefficients

Table A.1: *3rd order CIFF $\Sigma\Delta$ modulator coefficients.*

	R. Schreier's $\Sigma\Delta$ Toolbox			*modified-z-transform*			
	DT		CT RZ	CT RZ		CT NRZ	
	not scaled	scaled	scaled	not scaled	scaled	not scaled	scaled
$\frac{1}{f_1}$	1	0.6377	0.7686	1	0.6813	1	0.9324
$a_1\ f_1$	0.7999	1.2543	1.0410	0.9362	1.3741	0.6705	0.7191
$\frac{f_1}{f_2}$	1	0.7210	0.7713	1	0.7110	1	0.7642
$a_2\ f_2$	0.2881	0.6266	0.4860	0.3328	0.6870	0.2441	0.3426
$\frac{f_2}{f_3}$	1	0.1745	0.1373	1	0.1599	1	0.1662
$a_3\ f_3$	0.0440	0.5483	0.5407	0.0587	0.7578	0.0440	0.3715

Table A.2: *5th order CRFF $\Sigma\Delta$ modulator coefficients.*

	R. Schreier's $\Sigma\Delta$ Toolbox			*modified-z-transform*			
	DT		CT RZ	CT RZ		CT NRZ	
	not scaled	scaled	scaled	not scaled	scaled	not scaled	scaled
$a_1\ f_1$	0.5562	1.1527	1.2590	0.6070	1.5067	0.4227	0.9553
$\frac{1}{f_1}$	1	0.4825	0.4417	1	0.4029	1	0.4425
$a_2\ f_2$	0.2502	0.9417	0.8775	0.3413	1.6829	0.2495	1.1008
$\frac{f_1}{f_2}$	1	0.5507	0.6455	1	0.5034	1	0.5122
$a_3\ f_3$	0.0543	0.7380	0.5843	0.0681	0.9875	0.05	0.6746
$\frac{f_2}{f_3}$	1	0.2769	0.3259	1	0.3401	1	0.3270
$a4\ f_4$	0.0084	0.4956	0.4178	0.0112	0.7219	0.0084	0.4673
$\frac{f_3}{f_4}$	1	0.2304	0.2163	1	0.2250	1	0.2425
$a5\ f_5$	0.0006	0.4767	0.0619	0.0008	0.7844	0.0006	0.4537
$\frac{f_4}{f_5}$	1	0.0743	0.4823	1	0.0657	1	0.0736
$\frac{{g_1}^2\ f_3}{f_1}$	0.0007	0.0046	0.0033	0.0007	0.0041	0.0007	0.0042
$\frac{{g_2}^2\ f_5}{f_3}$	0.0020	0.1169	0.0192	0.0020	0.1352	0.0020	0.1121

Table A.3: *6th order CRFF bandpass ΣΔ modulator coefficients.*

	R. Schreier's ΣΔ Toolbox			*modified-z-transform*			
	DT		CT RZ	CT RZ		CT NRZ	
	not scaled	scaled	scaled	not scaled	scaled	not scaled	scaled
$\frac{1}{p_1}$	1	0.4476	0.4861	1	0.5246	1	0.5549
$\frac{p_1}{f_1}$	1	0.7654	0.7879	1	0.9174	1	0.7632
$a_1\ f_1$	0.5559	1.6224	1.4520	0.5028	1.0447	0.4931	1.1645
$\frac{f_1}{f_2\ p_2}$	1	0.6330	0.9520	1	0.8751	1	0.7764
$a_2\ f_2\ p_2$	-0.5559	-2.5630	-1.5250	-1.0533	-2.5010	-0.6431	-1.9560
$\frac{f_2\ p_2}{f_3}$	1	0.7250	0.7477	1	0.8720	1	0.6267
$a_3\ f_3$	-0.0211	-0.1342	-0.0774	-0.4531	-1.2340	-0.3036	-1.4740
$\frac{f_3}{f_4\ p_3}$	1	0.1767	0.4896	1	0.2057	1	0.3411
$p_3\ a4\ f_4$	-0.2219	-7.9840	-1.6630	-0.4574	-6.0530	-0.4577	-6.5130
$\frac{f_4\ p_3}{f_5}$	1	0.9026	0.7729	1	0.9419	1	0.7078
$a5\ f_5$	-0.0433	-1.7260	-0.4198	-0.0583	-0.8191	-0.0672	-1.3510
$\frac{f_5}{f_6}$	1	1.1170	1.2810	1	1.5390	1	1.1020
$a_6\ f_6$	0.0525	1.8730	0.3972	0.2282	2.0830	0.1616	2.9470
$\frac{{g_1}^2\ f_2\ p_2}{p_1}$	1.9620	4.0480	2.6160	2.4081	3	2.4081	1.5090
$\frac{{g_2}^2\ f_4\ p_3}{f_2\ p_2}$	2	15.61	5.4640	2.4673	13.75	2.4673	11.54
$\frac{{g_3}^2\ f_6}{f_4\ p_3}$	2.0380	2.0210	2.0580	2.5275	1.7430	2.5275	3.2390

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