COMPENSATED LAYOUT FOR AUTOMATED ACCURATE COMMON-CENTROID CAPACITOR ARRAYS

DiaaEldin Khalil, Mohamed Dessouky*, Vincent Bourguet**, Marie-Minerve Louerat**, Andreia Cathelin***, Hani Ragai**

**Faculty of Engineering, Ain Shams University, Cairo, Egypt*
***LIP6/ASIM Laboratory, CNRS-UPMC, University of Paris 6, Paris, France*
****STMicroelectronics - Central R&D/DAIS, Crolles, France*

Abstract - *In this paper, a layout scheme for accurate common-centroid rectangular unit-capacitor arrays is presented with detailed explanation of the rules used to improve matching. This layout technique is combined with a common-centroid arbitrary-value capacitor placement algorithm to form an automatic capacitor array generation tool. Finally, design and measurement results of a test chip that intends to evaluate the effectiveness of this automatic array generation tool are presented. Results indicate significant improvements in ratio accuracy.*

I. INTRODUCTION

The performance of many analog circuits is directly related to accurate capacitor ratios, which have a direct impact on a wide range of applications such as high precision filters for wireless communications and baseband. Using parallel unit capacitors instead of a single capacitor has a considerable effect in reducing ratio mismatch [1]. In addition, common-centroid geometries and interdigitization are particularly of great importance in reducing mismatch and achieving high accuracy as they help reducing the effects of gradients and random errors in fabrication [2]. Systematic sources of mismatch can be eliminated by using a group of precise rules during the layout phase as described in [3]. However, these rules require complicated and time-consuming full-custom layout.

Motivated by the importance of achieving high precision in capacitor ratios and that precise layout is still done in a case-by-case full custom approach, previous work focused on an automatic algorithm to arrange arbitrary capacitor ratios with common-centroid geometries in rectangular unit-capacitor arrays [4]. This work focuses on a generic precise layout scheme for such arrays. Both are integrated in an automatic capacitor array generator as a part of the IP design environment CAIRO+ [5]. Results are verified through a test chip and compared with conventional layout techniques throughout fifty dices of the same wafer to evaluate the effects of the algorithm and layout on capacitor ratio accuracy.

In section 2, the common-centroid algorithm is rapidly highlighted. In section 3, the details of accurate layout techniques are explained. In section 4, the test chip design is overviewed. In section 5, measurement results are presented. Finally, in section 6, conclusions are drawn.

II. PLACEMENT ALGORITHM

The main advantage of the placement algorithm presented in [4] is that it handles arbitrary capacitor ratios and not just multiples of the unit capacitor. It provides common-centroid distribution of capacitors, gives special care to equal capacitors, and is easily integrated in CAD tools.

The algorithm classifies capacitors into even, odd, and non-integer according to their ratio to the unit capacitor. Since even capacitors can be symmetrically distributed throughout the rectangular array, the non-even part of odd and non-unit capacitors are placed first as near to the center of the array as possible while the remaining even parts and even capacitors are placed afterwards with interleaved sequence. This idea makes the centroids of all capacitors nearest to the center of the array and thus reduces possible mismatch due to gradients. In addition, the algorithm gives special care to the arrangement of equal capacitors, which are identically interleaved to reduce second-order effects besides having exactly the same centroid.

III. PROPOSED ACCURATE ARRAY LAYOUT

Conventional layout of complex-ratio capacitor arrays ignores the common-centroid arrangement of unit capacitors seeking easy, simple routing and compact area [6]. However, common-centroid geometries proved to be of great importance in achieving high accuracy in matching capacitor ratios. They provide good cancellation of random variations across the array and the gradients in fabrication processes [2]. Designers tend to use common-centroid arrays only for simple ratios in arrays with limited number of capacitors.

In addition, there are specific systematic sources of mismatch that result from the effects of layout and fabrication processes on relative capacitance values [3]. Systematic sources of mismatch are identified and stated in order of importance as follows: mismatched perimeter ratios, proximity effects in unit capacitor lithography, mismatched long-range fringe capacitance, and mismatched interconnect capacitance. Thus, capacitor array layout must follow special rules to reduce the effect of these sources on mismatch. Figure 1 shows an example of the proposed capacitor array layout composed of five capacitors with a ratio of 1.2:5.8:7:7:8. Rules used in the array layout are discussed in the following subsections.

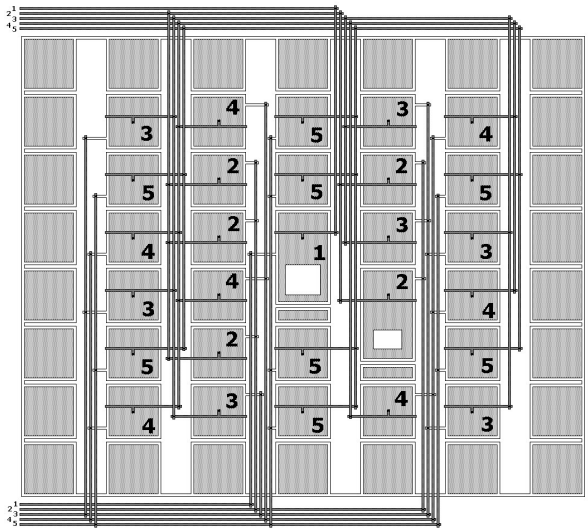

Figure 1
The New Capacitor Array Layout

A. Capacitor Array Layout Rules

These rules are deduced based on systematic sources of mismatch. They tend to make mismatch sources affect each unit capacitor equally so that capacitance errors are ratioed and hence matched. Non-unit capacitors layout rules are discussed in subsection *C*. To clearly demonstrate layout rules, figure 1 represents an example of a complete array layout while figure 2 represents a zoomed view on a unit capacitor showing nearby structures and routing. These figures can clearly illustrate the following rules.

Using parallel square unit capacitors instead of a single large capacitor provides a perimeter ratio equal to the desired area ratio. Thus, the fringe capacitance from the perimeter of the upper and lower plates is matched to the area ratio. Also line width variations do not affect area ratio as all unit capacitors are affected equally and thus the change in capacitance is ratioed.

Long-range fringe capacitance however needs additional care. Unit capacitors at the edge of the array suffer less fringing than those internal to the array due to adjacent structures and wide streets of lower plate. These unequal effects produce mismatch. Thus, the array is surrounded by dummy unit capacitors to act as adjacent structures as shown in figure 1. Moreover, each unit capacitor has a separate bottom plate so that the lower plate street bordering each unit capacitor is the same, producing equal long-range fringing. These separate lower plates are interconnected exactly in the same manner as the upper plates.

Mask misalignment is also important. The lower plate should be larger than the upper plate to account for mask misalignments that may occur during fabrication and so the unit capacitor area is not affected. Also, interconnects passing over the unit capacitor must run across two opposite sides of the capacitor so that the added overlap capacitance between the interconnect and the lower plate is not affected by mask misalignment as shown in figure 2. When the mask move to one side one overlap increase while the other decrease.

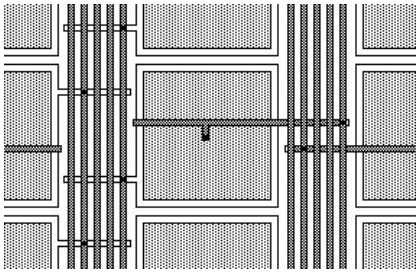

Figure 2
Unit Capacitor and Adjacent Structures

Proximity effects due to variations in light interference and chemical processes in fabrication depending on the location of the adjacent structures is of great effect on mismatch. To overcome these proximity effects, the layout around each unit capacitor, for a range from 30 to 50 μm, must be as identical as possible. This includes the introduction of dummy unit capacitors around the array, and the insertion of dummy fillings in spaces left from non-unit capacitors. Moreover, interconnects for the upper plates are identical as well as those for the lower plates. Routing channels for connecting the parallel unit capacitors have equal widths, making the distance separating unit capacitors uniform horizontally and vertically. This insures that all structures around the unit capacitors of the array are identical so that proximity effect variations are also identical for each unit capacitor and thus the effects are matched.

B. Routing Rules

Connecting parallel unit capacitors is not simple in common centroid capacitor arrays. Unit capacitors forming a large capacitor may be widely spread across the array. In addition to upper plates, lower plates should also be connected. Thus to provide automatic array generation, routing must follow specified rules that provide easy connection and also prevent increasing mismatch. The following rules are also illustrated in figures 1 and 2.

Routing wires are either horizontal or vertical to prevent any intersection or overlap capacitance. Routing of upper plates is separated from that of lower plates to avoid additional coupling and overlap capacitance. Routing channel is either for upper plates or the lower plates of the adjacent unit capacitors. Upper routing channels and lower routing channels are interchanged successively as shown in figure 1.

Interconnect to unit capacitor does not run at its center to allow interconnect of the opposite unit capacitor to have access to the shared routing line as shown in figure 2. This is done for upper and lower plates. Grounded lines separate long adjacent parts of routing lines running close to each other. This option is not shown in the layout of figure 1.

C. Non-unit Capacitor Layout Rules

The proposed layout is capable of handling arbitrary ratios that are not just multiples of the unit capacitor. It has special layout rules for the non-unit part of the

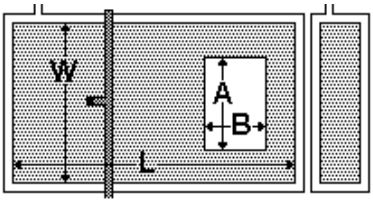

Figure 3
Non-unit Capacitor Using Slotted Rectangle Technique

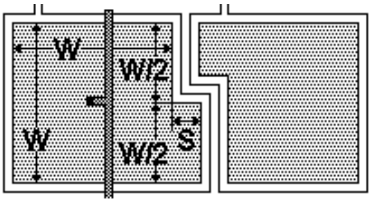

Figure 4
Non-unit Capacitor Using Added Stub Technique

capacitor. These rules also intend to compensate the effects of systematic sources of mismatch.

Non-unit capacitors are used to implement non-integer ratios in rectangular structures rather than square capacitors [1]. Their ratio to the unit capacitor is between 1 and 2. The layout of the non-unit capacitor must occupy at most the area of two adjacent unit capacitors. The layout employs the slotted rectangle technique [1], shown in figure 3. The smaller dimension of the rectangle is equal to the unit capacitor side ***W***. The other dimension of the rectangle and slot dimensions are calculated in a way to keep the same overall perimeter-to-area ratio as the square unit capacitor while respecting the required ratio ***R*** according to the following equations:

$$A/W + B/W + AB/W^2 = R - 1 \quad (1)$$

$$L/W = AB/W^2 + R \quad (2)$$

When the non-unit capacitor ratio ***R*** is near to 1, the slotted rectangle technique is no more suitable since the slot dimensions become too small to be realized without layout design rule errors. The stub technique [1], shown in figure 5, is alternatively used. A small rectangular part of width ***W/2*** is attached to the unit capacitor from one side. The length of the stub is calculated according to the required ratio ***R*** to keep the same perimeter-to-area ratio according to the following equation:

$$S/W = 2(R-1) \quad (3)$$

Like unit capacitors, the non-unit capacitor has a separate bottom plate so that the lower plate street bordering is the same as that of unit capacitor. The remaining unused part of the area of the two unit capacitors is filled with dummy structures with the same lower plate street bordering. These rules provide matched long-range fringe capacitance for the non-unit capacitor, and matched proximity effects since structures surrounding the non-unit capacitor are nearly identical to those surrounding the unit capacitor.

Interconnects passing over non-unit capacitors must also run across two opposite sides as shown in figure 3 and 4 to compensate for mask misalignment. However, the interconnect width is multiplied by the ratio ***R*** to provide matched overlap capacitance.

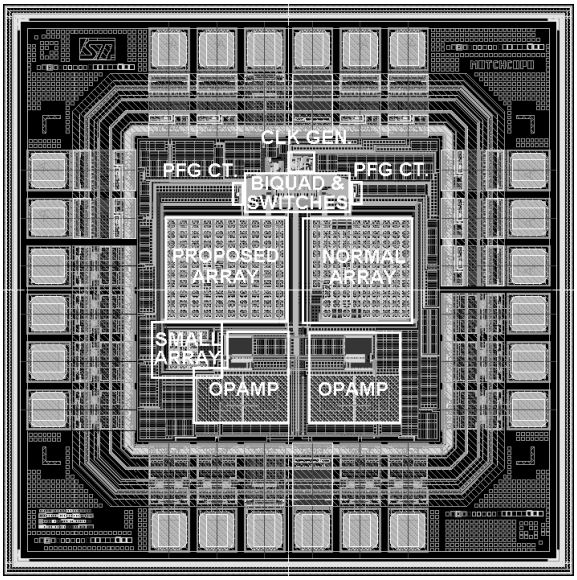

Figure 5
Test Chip Layout

IV. TEST CHIP

A test chip is designed to evaluate errors in capacitance ratio between two capacitor arrays: the first uses the common-centroid placement algorithm and the proposed layout scheme while the second is a conventional non-common-centroid capacitor array [6]. Two techniques are employed to evaluate ratios. Since the precision of switched capacitor circuits (SC) depends on capacitor ratios [6], a SC low-pass biquad was the main part of the test chip. In addition, a pseudo-floating gate circuit for the measurement of the ratio between two capacitors [7] is employed with switches to select the desired capacitor ratio. The chip is designed in STMicroelectronics 0.18-micron technology under a supply of 1.8V. It has thin oxide MIM capacitor used to implement the capacitor arrays. The final layout is illustrated in figure 5. The total chip area is 1072mm x 1072mm. The core area is 570mm x 570mm.

V. MEASUREMENTS

Measurements are performed on 31 chips using GPIB enabled instruments under MATLAB control, which is used for acquisition and also for data post-processing.

Measurements are classified into two main parts: frequency response measurements and capacitor ratio measurements. The measured frequency responses of *all* 31 chips using both arrays are all plotted in figure 6 (a). Also figure 6 (b) shows the standard deviations of all chips responses versus frequency for both arrays. The important specifications of the frequency responses are extracted. Their mean and standard deviation values for both arrays are presented in table I. Results indicate that using the proposed common-centroid layout provided

less variation by a factor around two in A_{DC} and f_0 and a factor more than six in Q.

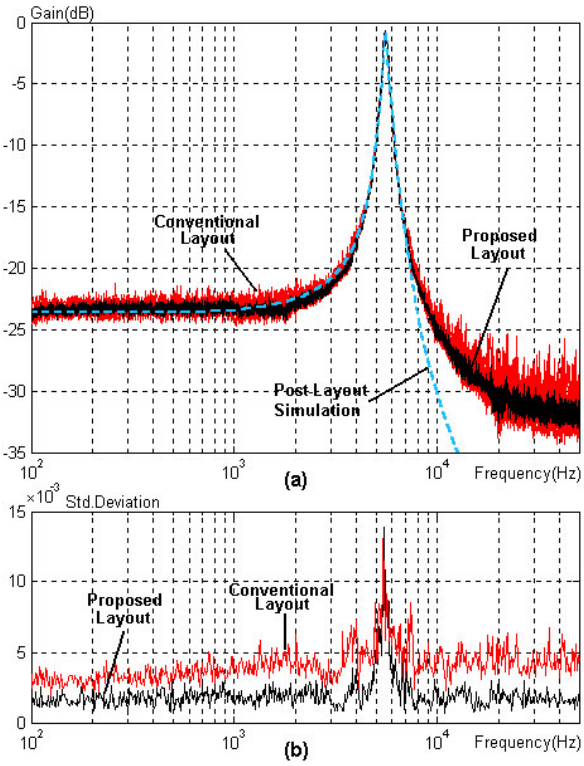

Figure 6
(a) Measured Frequency Response of All Chips
(b) Standard Deviation of Frequency Response

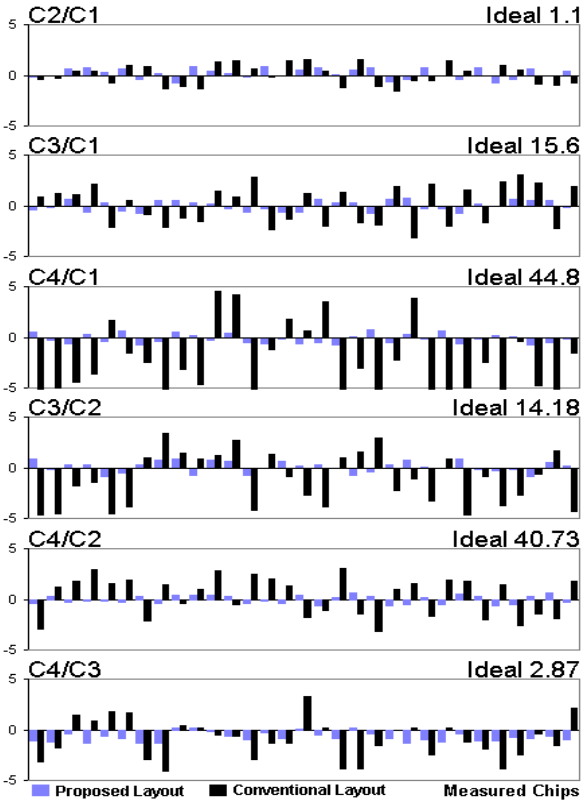

Figure 7
Percentage Error in Measured Ratios

Table I
Frequency Response Parameters

		Proposed Capacitor Array	Conventional Capacitor Array
A_{DC} (dB)	Mean	-23.688	-23.675
	Std. dev.	0.1898	0.4543
f_O (Hz)	Mean	5559.7	5562.7
	Std. dev.	8.2330	14.947
Q	Mean	13.512	13.409
	Std. dev.	0.0389	0.2474

Capacitor ratio measurements include all six ratios for the four capacitors. Figure 7 presents percentage error in measured ratios for each one of the measured chips. Percentage error is defined as follows:

$$Error\% = \frac{MeasuredRatio - IdealRatio}{IdealRatio} \times 100 \quad (4)$$

Capacitor ratio measurements indicate that mismatch in ratios is reduced by more than 50%. As clear from measurement results, it can be concluded that the proposed common-centroid layout allows achieving higher precision in capacitor ratios. Also it provides less variation of the ratios across the wafer, indicating reduced effects of process variations.

VI. Conclusions

In this paper, a proposed layout scheme for high precision rectangular capacitor array is presented. Layout rules are explained in details. A test chip to evaluate the new common-centroid layout is designed, fabricated, and measured. Measurements showed less variation from ideal behavior for the new array layout by a factor that ranges from two to six times. It can thus be concluded that the new array layout, besides being completely automated, improves matching accuracy and reduces the effects of process variations, which have a direct impact on a wide range of applications.

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