A High Level SoC Energy Analysis Method with good Accuracy using Cycle Accurate Simulation

Ana Abril, Habib Mehrez, Frédéric Pétrot, Jean Gobert* and and Carolina Miro*
ASIM/LIP6 Lab, University Paris VI & Philips Applied Technologies*
4, place Jussieu, 75252 Paris cedex 05, France
Email: Ana.Abril@lip6.fr

This paper presents a method for energy consumption estimation and optimisation on hardware-software embedded systems-on-chip using cycle-accurate simulation.

Higher level energy estimations of SoC are proposed by some other approaches [2] [3] [4] [5]. Each one covers one stage on the highest levels of the design flow. However none enables to estimate and optimize the energy dissipation of all elements of an architectural description of an embedded system. A complete approach allowing this should *a)* use concurrent and very fast simulation, *b)* provide the energy dissipation of all the components including new accelerators and the interconnections with enough accuracy and *c)* give the energy dissipation evolution of the system to experiment dynamic low power techniques at system level. We present a new approach that, using some ideas from previous approaches, attempts to gather all these needs.

An embedded system is a complex combination of components like processors, coprocessors, memories and interconnections created to execute a given application. To develop the system architecture and communications, a system simulation using functional and very abstract models of the components is used at the beginning of the design flow. The cycle-accurate C-based simulation allows this very fast functionnal analysis because the simulation speed and the performance accuracy are very high for a short modelling time. We use TSS a system level simulation framework developed by Philips [1].

To perform the energy estimation at cycle accurate level, the functional models of the components are enriched with an energy view and the energy estimations are obtained during cycle accurate simulations. To do that, the basic functional states of the state machine of each TSS model are analyzed in order to estimate energy consumption per transition. These energies per transition are associated to the model state machine and accumulated during the simulation of a particular application, giving the energy estimation per component and for the entire system at point in time. This is not a completely accurate estimation but it is sufficient to find the best hardware architecture scenario in terms of power consumption. This method can be generalized for all others simulators that model the components at cycle level in states machines like SystemC.

The transitions between states represent the functionality of the component per cycle. For each transition, one or more basic operations are executed with a dynamic and static energy consumption associated. The set of energies per operation is the energy model of the hardware block and these values are calculated using several methods: *1) macro-modelling*, giving a library of values measured at low level, *2) fast-modelling*, using equations where parameters are easily estimated from technological, structural and functional information and, *3) entropy*, estimating the unknow parameters using entropy equations. The processor and memory energy values are calculated using macro-modelling with information from datasheets. Hardware accelerators and interconnect use fast modelling equations using parameters estimated from low level information or using entropy.

This approach has been validated on a HW/SW MPEG-4 video decoder system example, obtaining energy estimations during simulation. The accuracy of these estimations depends on the accuracy of the cycle-accurate functional modelisation and on the accuracy of the energy values. Our TSS functional models are well defined and the energy values are calibrated from RTL measurements, so the error of the energy estimation is considered lower than **6%** from physical measurements.

The energy results show that the SDRAM memory and the processor are the most power consuming elements. To reduce their energies we have applied several low power techniques at architectural level, specially on the memory. The more interesting techniques are another memory hierarchy, data embedded compression before memory storage, clock gating for all elements, several frequencies between the components and voltage reduction on the processor. Although these techniques are applied by component, their effect influences all the system giving very important energy reductions and our approach allows to study this effect. The maximum reduction obtained applying all techniques together is **93%**. This is a very good result that demonstrates the interest of our approach for the fast and early energy evaluation and optimization of embedded systems-on-chip at architectural level.

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