Evaluation of Capacitor Ratios in Automated Accurate Common-Centroid Capacitor Arrays

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Abstract

In this paper, design and measurement results of a test chip that intends to evaluate differences between layout techniques for rectangular unit-capacitor arrays are introduced. Precision capacitor ratios are compared using a switched-capacitor biquad and a pseudo-floating gate configuration. The test chip is used to evaluate the effectiveness of an automatic common-centroid capacitor array generation tool with ***arbitrary*** *capacitor ratios. Results indicate significant improvements in ratio accuracy, which have a direct impact on a wide range of applications such as filters for wireless communications, hard drives, and high precision baseband processing.*

1. Introduction

The key performance of many analog circuits is directly related to accurate capacitor ratios. It is well known that using parallel unit capacitors has a great effect in reducing ratio mismatch [1]. In addition, common-centroid geometries are considered particularly important to reduce mismatch and achieve high accuracy as they help reducing the effects of gradients and random errors in fabrication [2]. Specific layout rules have been defined to decrease systematic sources of mismatch [3]. However, the application of such rules requires time-consuming complicated full-custom layout.

To solve the problem of precision capacitor array generation, previous work [4] focused on a generic layout for rectangular unit capacitor arrays and an algorithm to automatically arrange arbitrary capacitor ratios in such arrays with common centroid geometries. This work was integrated in an automatic capacitor array generator as a part of the IP design environment CAIRO+ [5].

It was important to evaluate both the layout and the algorithm. No tool provides the ability to exactly simulate the sources of mismatch during fabrication, thus it was important to fabricate a test chip. Measurements over 50 dice from the same wafer can account for the existing mismatch. This paper describes a test chip for the purpose of evaluating the process of capacitor array generation. In section 2, previous work is highlighted. In section 3, the detailed design of the test chip is introduced. In section 4, the complete layout of the chip is illustrated. In section 5, measurement results are presented. In section 6, final conclusions are drawn.

2. Automated Accurate Capacitor Arrays

The main advantage of the placement algorithm presented in [4] is that it handles arbitrary capacitor values and arranges them automatically with a common centroid. The algorithm classifies capacitors into even, odd, and non-integer according to their ratio to the unit capacitor. Since even capacitors can be symmetrically distributed throughout the rectangular array, the non-even part of odd and non-unit capacitors are placed first as near to the center of the array as possible while the remaining even parts and even capacitors are placed afterwards with interleaved sequence. This idea makes the centroids of all capacitors nearest to the center of the array and thus reduces possible mismatch due to gradients. In addition, the algorithm gives special care to the arrangement of equal capacitors, which are identically interleaved to reduce second-order effects besides having exactly the same centroid.

The layout of the automated array [4] reduces systematic mismatch errors [3]. For example, it provides matched perimeter ratios, matched long-range fringe capacitance, and equal proximity effects in unit-capacitor photolithography. Non-unit capacitors follow the above

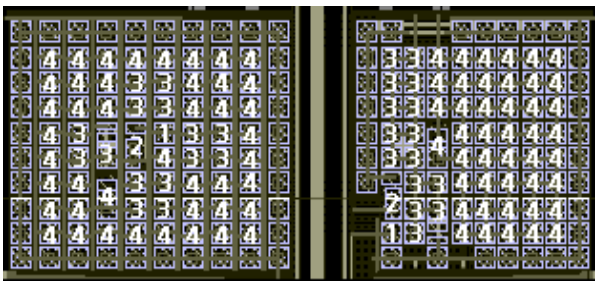

Figure 1. Proposed and Conventional Layouts

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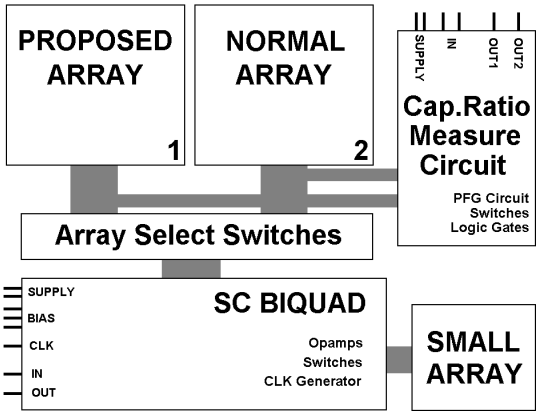

Figure 2. Test Chip Block Diagram

constraints and do not exceed two cells. The array layout is expandable to any required dimensions. Also a systematic routing scheme is defined for arbitrary unit-capacitor distribution. Routing ensures matched parasitic interconnect capacitance. Both the algorithm and layout scheme can be easily implemented in CAD tools.

Figure 1 compares two layouts of the same array consisting of four 1:1.1:15.6:44.8 capacitors. The first uses the proposed placement algorithm and layout that favors common centroid placement with routing channels (left), while the second uses conventional array layout that favors compactness with units of the same capacitor placed next to each other (right).

3. Test Chip Design

The aim of the test chip was to evaluate errors in capacitance ratio in two capacitor arrays: the first uses the proposed common centroid scheme while the second is a conventional non-common centroid one.

Two techniques are employed to quantify capacitor ratios. Generally, the precision of switched capacitor circuits depends on capacitor ratios [6]. So, a switched capacitor biquad was chosen as the main part of the test chip. In addition, a pseudo-floating transistor gate circuit for the measurement of the ratio between two capacitors [7] is employed with CMOS switches to select the desired capacitor couple from the array. Figure 2 shows the general block diagram of the chip.

Instead of having two complete circuits for each array, only one active circuit is deployed with CMOS switches to switch between the two arrays. Therefore, since the active circuit is common, differences in performance are only related to differences between the two arrays. Simulations proved that using the switches doesn't affect the biquad performance. Moreover, this design reduces the required chip area by nearly 25%, due to sharing of switches, transistors, and especially opamps that occupy much area.

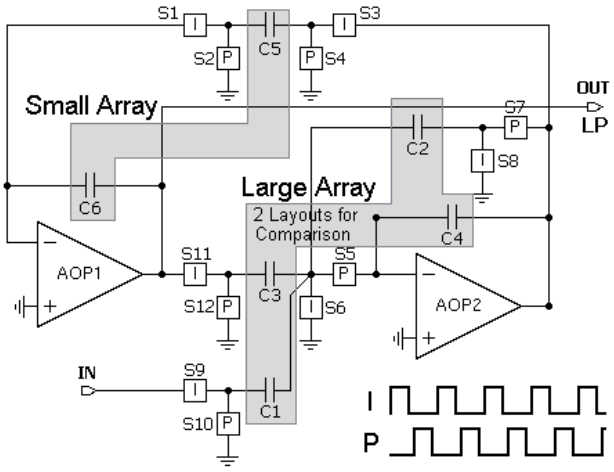

Figure 3. Biquad Schematic

Capacitor	C1	C2	C3	C4	C5	C6
Value (pF)	0.2	0.22	3.12	8.96	0.2	0.582

Table 1. Capacitor Values

3.1. Switched-Capacitor Biquad

The first part of the circuit is a switched-capacitor biquad. Through the measurement of its transfer function for both arrays, differences in performance can evaluate the effect of the proposed common centroid layout.

The ideal design of the biquad is shown in figure 3. This Fleischer-Laker switched-capacitor biquad has a Tchebychev transfer function. It is designed with an F-circuit topology using OCEANE [8]. The capacitor values are chosen with dynamic range scaling to make both integrators overload at the same level and thus have largest dynamic range at the output. Capacitor values are shown in table 1. The small array, composed of C5 and C6, uses the proposed common centroid layout while the large array, composed of C1-C4, is implemented two times as shown in figure 1. We can switch between the two layout implementations to evaluate the difference in performance.

The biquad has the following specifications: dc gain A_{DC}=-23.86dB, cut-off frequency f_O=5.5kHz, quality factor Q=13.96, and sampling frequency f_S=100kHz. A large Q, has been chosen so that the circuit would be more sensitive to capacitor ratio errors. The specs are related to capacitor ratios as follows:

$$A_{DC} = 20 \cdot \log\left(\frac{C1}{C3}\right) \quad (1)$$

$$f_O = \frac{f_S}{2\pi} \cdot \cos^{-1}\left(1 - \frac{C5 \cdot C3}{C6 \cdot (C2 + 2C4)}\right) \quad (2)$$

$$Q = \sqrt{\frac{C3 \cdot C5}{2C2 \cdot C6}\left(1 + \frac{2C4}{C2} - \frac{C3 \cdot C5}{2C2 \cdot C6}\right)} \quad (3)$$

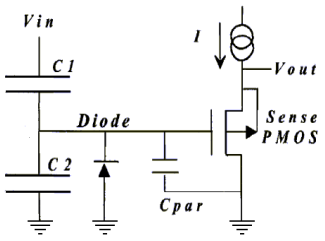

Figure 4. Pseudo-Floating Gate Circuit [7]

Two identical opamps are used, namely a 2-stage miller-compensated opamp for larger output swing. The opamps are designed to be directly connected to the pads without buffers. The opamp has a dc gain of A_{DC}=100dB, a gain-bandwidth product of f_T=3.5MHz, and a phase margin of PM=72º for a 70 pF load.

The biquad switches are generally CMOS. Switches near each opamp are NMOS and use advanced clocks to reduce charge injection errors [6]. Extra switches are added to be able to switch between the two arrays. These switches are controlled by two external pins, one for each array, so that both can be isolated completely from the biquad during capacitor ratio measurement as explained in the following section.

3.2. Capacitor Ratio Measurement Circuit

For capacitor ratio measurement, pseudo-floating gate technique is considered the easiest, most effective and compact way [7]. In addition, it requires very simple measurement setup with only DC signals. The measurement circuit consists mainly of a PMOS transistor with the couple of capacitors under test, *C1* and *C2* connected to its gate as shown in figure 4. With a constant bias current, the output voltage is expressed as:

$$V_{OUT} = \left(\frac{C1}{C1 + C2 + Cpar} \right) \times V_{IN} + V_{TSAT} \qquad (4)$$

where V_{TSAT} is a constant depending on the bias current, pseudo-floating node parasitic charge, the sense PMOS threshold voltage, and transconductance parameter, while *Cpar* is the parasitic capacitance at the gate.

A diode is introduced on the transistor gate as in [7]. This diode provides protection against antenna effects. However, the diode introduces leakage reverse current that causes output drifts with measurement time.

Switches are essential for the selection of the two required capacitors from the array. A small logic circuit reduces the number of external pins needed for this selection to only four pins, one for each capacitor. Thus, by selecting two of the four pins, the two corresponding capacitors are connected appropriately. There are two measurement circuits, one for each array, sharing input and selection pins to measure the ratio in both arrays simultaneously. Thus, the difference in measurement is only related to the ratio rather than the input.

4. Layout

The chip is designed in STMicroelectronics 0.18-micron technology with: supply 1.8V, single poly layer, and 6 metal layers. It also has thin oxide MIM capacitor that is used to implement the capacitor arrays.

Guard rings are used to isolate noisy digital core parts from noise sensitive analog core parts to prevent noise from being coupled through substrate. In addition, interrupted pad rings technique for separating digital supply and signal pads from their analog counterparts is used for low supply noise and substrate coupling between them. Also to reduce noise, power and ground pads are placed next to each other such that bond wires produce mutual inductance that reduces noise. They are also placed on central less inductive pins in the package with the shortest bond wires. Output buffers, high current IOs, and such aggressors are placed near power and ground pads while input buffers, analog signals, and such victims are placed as far as possible.

The final layout is illustrated in figure 5. The placement of capacitors in both arrays are shown in figure 1 for comparison. The chip appears to be pad- limited. The total chip area is 1072mm x 1072mm. The core area is 570mm x 570mm. The chips are received in TQFP32 plastic packages.

5. Measurements

Measurements are performed on 31 chips using GPIB

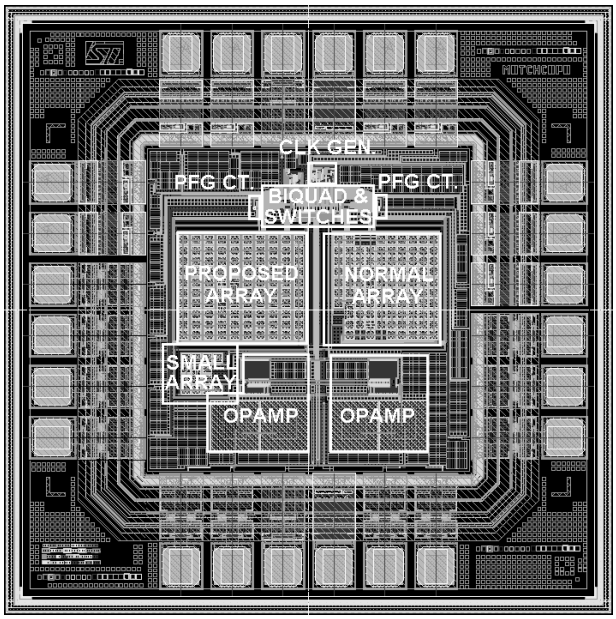

Figure 5. Complete Test Chip Layout

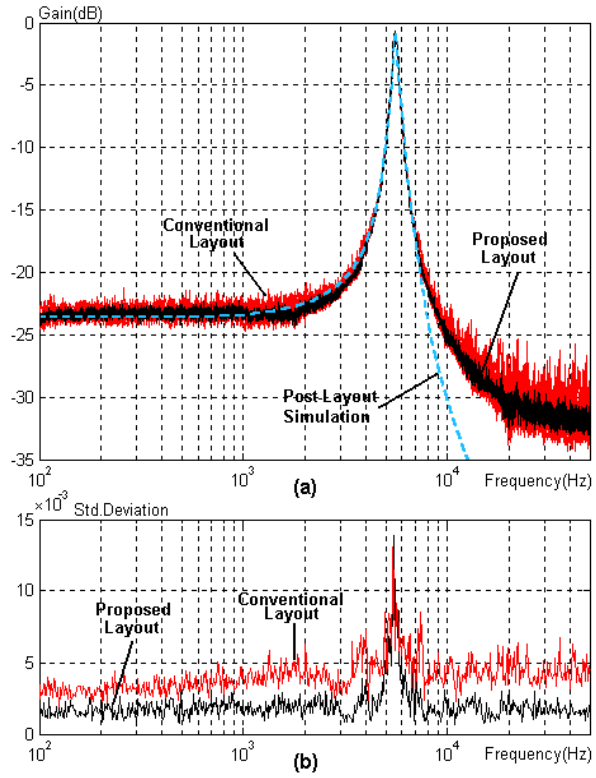

Figure 6.
(a) Measured Frequency Response of All Chips
(b) Standard Deviation of Frequency Response

enabled instruments under MATLAB control, which is used for both data acquisition and post-processing.

Measurements are classified into two main parts: frequency response measurements and capacitor ratio measurements. The frequency response is measured by stepping the input signal frequency while measuring the output at each frequency. Then using MATLAB, the frequency response can be plotted. The measured frequency responses of *all* 31 chips using both arrays are all plotted on the same figure as shown in figure 6 (a). Also figure 6 (b) shows the standard deviations of all chips responses versus frequency for both arrays. The important specifications of the frequency responses are extracted. Their mean and standard deviation values for both arrays are presented in table 2. Results indicate that using the proposed common centroid layout provided less variation by a factor around two in A_{DC} and f_0 and a factor more than six in Q.

Capacitor ratio measurements include six ratios for four capacitors (C1/C2, C1/C3, C1/C4, C2/C3, C2/C4, C3/C4). The capacitor ratio, for example C1/C2, is measured by applying constant current of 1μA to the source of the PMOS while its voltage V_{OUT} is monitored. First, C2 is connected to ground while the input voltage V_{IN} is applied to C1. V_{IN} is stepped in time to values of 0.1V, 0.2V, 0.3V and V_{OUT} is measured. V_{OUT} drift versus

		Proposed Capacitor Array	Conventional Capacitor Array
A_{DC} (dB)	Mean	-23.688	-23.675
	Std. dev.	0.1898	0.4543
f_O (Hz)	Mean	5559.7	5562.7
	Std. dev.	8.2330	14.947
Q	Mean	13.512	13.409
	Std. dev.	0.0389	0.2474

Table 2. Mean and Standard Deviation of Frequency Response Parameters

time is calculated in each V_{IN} step then integrated and

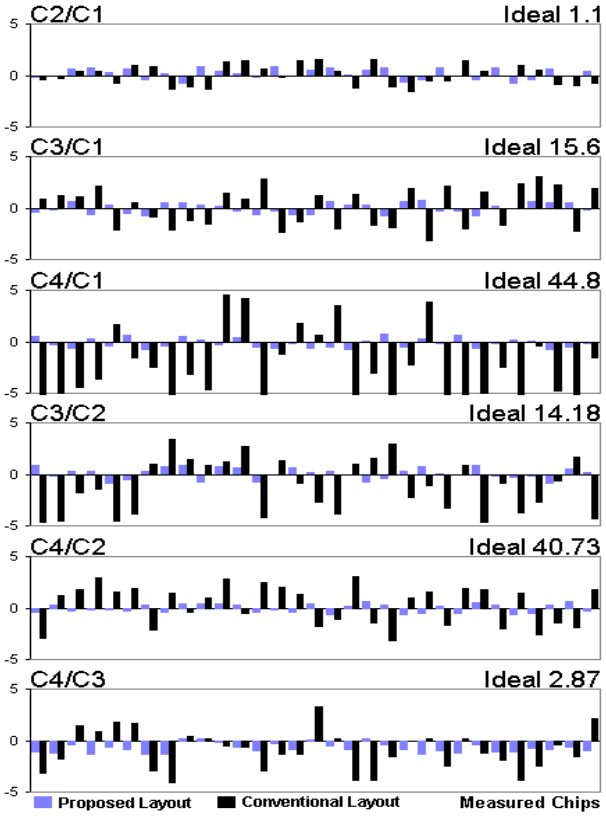

Figure 7. Percentage Error in Measured Ratios

cancelled to produce drift corrected V_{OUT}. The slope S_1 of V_{OUT}/V_{IN} is then calculated. This is repeated for C1 grounded while V_{IN} is applied to C2 and the slope S_2 of V_{OUT}/V_{IN} is calculated. Finally double slope relation is used to calculate capacitor ratio [7] as follows:

$$\frac{S1}{S2} = \frac{C1}{C1+C2+Cpar} \div \frac{C2}{C1+C2+Cpar} = \frac{C1}{C2} \qquad (5)$$

Figure 7 presents percentage error in measured ratios from ideal values for each one of the measured chips. Percentage error is defined as follows:

$$Error\% = \frac{MeasuredRatio - IdealRatio}{IdealRatio} \times 100 \qquad (6)$$

Capacitor ratio measurements indicate that mismatch in ratios is reduced by more than 50%. It can be concluded that the proposed common centroid layout allows achieving higher precision in capacitor ratios, provides less variation of the ratios across the wafer, and reduced susceptibility to process variations.

6. Conclusions

In this paper, the impact of a previously proposed placement algorithm and layout for high precision capacitor ratios in rectangular unit capacitor arrays is demonstrated via a real-life Si circuit. The design of the test chip is presented in details. The chip is composed of a switched-capacitor biquad and capacitor ratio measurement circuits. Measurements showed less variation from ideal behavior for the proposed array by a factor that ranges from two to six times.

It can be concluded that the proposed array, besides being completely automated, improves matching accuracy and reduces the effects of process variations, which have a direct impact on a wide range of applications such as filters for wireless communications, hard drives, and high precision baseband processing.

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