A simple 3.8mW, 300MHz, 4-bit flash analog-to-digital converter

Laurent de Lamarre[a], Marie-Minerve Louërat[a] and Andreas Kaiser [b]

[a]LIP6 - UPMC Paris 6, 12 rue Cuvier, 75005 Paris, France;
[b]IEMN-ISEN UMR CNRS 8520, 41 Bd Vauban, 59046 Lille Cedex, France

ABSTRACT

This paper presents a fully differential comparator that can be used in a N bit Flash A/D converter as continuous-time sigma-delta modulator quantizer. The comparator is an extension of the dynamic comparator presented by Lewis and Gray,[1] resulting in a 4 bit A/D. Its main advantages are : compact architecture based on MOS transistor only, without any passive components such as resistance ladder or switch capacitance, fully differential input and output voltages, operating at very low voltage. Using this comparator, a 4 bit flash A/D converter has been designed in a $0.13\mu m$ CMOS technology, under 1.2V supply voltage. It operates at 300Msample/s, suitable for over sampled data converter. The simulation shows a 3.8mW power consumption for the whole ADC.

Keywords: Flash ADC, Low Voltage, Oversampled Converters, Analog design

1. INTRODUCTION

Continuous-time $\Sigma\Delta$ modulators are now used for wireless communication systems for their ability to get rid of the anti-aliasing filter compared to the discrete-time architecture. They have demonstrated high resolution capabilities at low-power consumption. Yet one main disadvantage of the continuous-time modulator is its sensitivity to clock jitter in the feed-back signal. One interesting solution to decrease the continuous-time $\Sigma\Delta$ modulator sensitivity to clock jitter is to use a multi-bit quantizer.[2,3]

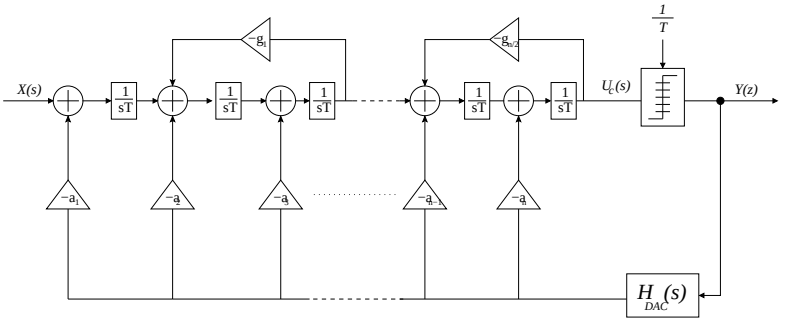

Figure 1. Architecture of a nth order feedback $\Sigma\Delta$ modulator.

In $\Sigma\Delta$ modulators, the main specifications for the quantizer are offset, speed, area and power consumption requirements. Taking advantage of the fact that, in such converters, non-idealities of the quantizer are subject to the same noise-shaping operation as the quantization noise, the offset specification of the quantizer is generally relaxed and does not degrade the performance of the converter. Moreover the quantizer has to operate at the speed required by the oversampling process. Therefore it must be implemented as a flash A/D converter.

Further author information: (Send correspondence to L.d.L.)
L.d.L.: E-mail: laurent.delamarre@lip6.fr, Telephone: +33 (0)1 44 27 71 23
M.M.L.: E-mail: marie-minerve.louerat@lip6.fr, Telephone: +33 (0)44 27 71 08
A.K: E-mail: Andreas.Kaiser@isen.fr

This paper presents a fully differential flash A/D converter that can be used as the 4-bit quantizer of a continuous-time $\Sigma\Delta$ modulator (Fig. 1). It is based on a fully differential comparator, which is an extension of the dynamic comparator presented in[1, 4, 5] and used in pipelined converters. Its main advantages are : compact architecture based on MOS transistors only, with progammable threshold voltage , fully differential input and output voltages, operation at very low voltage. Yet, as discussed in[5] , special care must be taken to handle offset voltages resulting from matching issues.[6]

Using this comparator, a 4 bit flash A/D converter has been designed in a 0.13 μm CMOS technology, under 1.2V supply voltage, without any passive component such as resistance ladder or switch capacitance. It operates at 300Msample/s and is suitable for over sampled data converters. The simulation shows a 3.8mW consumption for the whole converter.

This paper presents the architecture of the flash converter, using only active devices in section 2. In section 3, the design of the comparator is discussed, with special attention to mismatch effects. Simulation results are given in section 4.

2. DIFFERENTIAL FLASH ADC

2.1. 4 bit ADC Architecture

The block diagram of the 4 bit fully differential flash converter is shown in Fig. 2. The differential input signals (V_{in+} and V_{in-}) are simulateously compared with a set of 15 DC voltage thresholds implemented within the programmable comparator. Only 2 reference voltages are required to provide the 15 threshold voltages of the comparators. In fact, two banks of 14 NMOS transistor each, acting as controlled resistor are used. Proper biasing of input signal of the NMOS gates either by V_{ref+} or V_{ref-} allows to control the threshold, as illustrated by Fig. 3 of section 2.2.

Note that no resistor are needed in this architecture. The 15 comparator bank outputs a string of $2 * 15$ bits which is the thermometer coded input. It is encoded after the comparator bank.

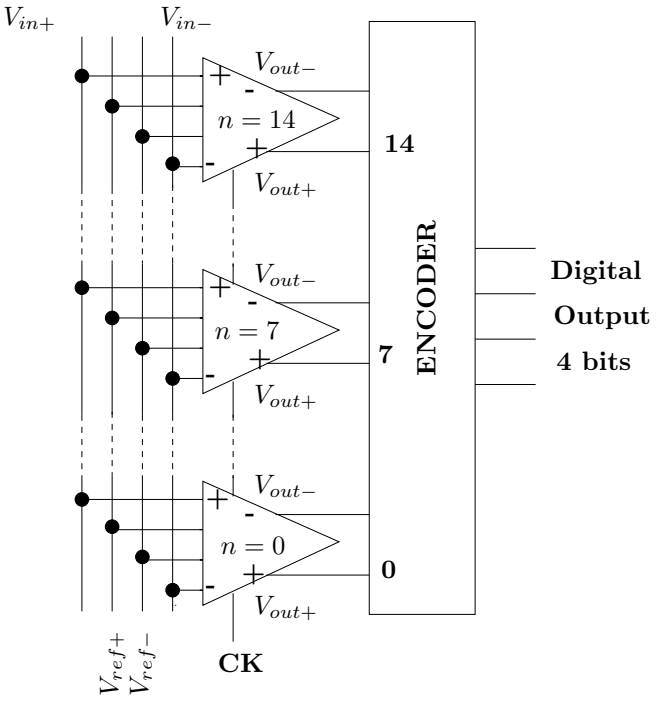

Figure 2. 4 bits A/D Flash Converter.

2.2. Differential comparator

The comparator topology, shown in Fig. 3 (a), is based on a cross-coupled inverter latch. A NMOS transistor, connecting the outputs of the inverters, is used as a switch, controlled by the sampling clock, to balance the latch. The currents flowing in the inverters are controlled by a set of NMOS transistors connected to their sources and operating in the triode region. These transistors act as variable steering resistors, controlled by the input signal and the reference voltages.

The comparison occurs in two phases. In the reset phase, the switch is ON and the outputs of the latch are equal. During this phase, a static current flows through the branches of the circuit. In the settling phase, the switch turns OFF and the final state of the latch is reached depending on the difference between the currents steered to the inverters. The configuration used for the steering resistors is shown in Fig. 3 (b). M1, M2 and M3 are divided respectively into $(2^{NB}-2)$, n and $(2^{NB}-2-n)$ parallel elementary transistors.

Transistors M1-M2-M3 are all in triode region, the conductance expressions for the left and right branches for the nth comparator are

$$G_L = \mu_n Cox \frac{W_1}{L_1}\left(\left(2^{NB}-2\right)\left(V_{in+}-V_{th}\right)+\left(2^{NB}-2-n\right)\left(V_{ref-}-V_{th}\right)+\left(n\right)\left(V_{ref+}-V_{th}\right)\right)$$

$$G_R = \mu_n Cox \frac{W_1}{L_1}\left(\left(2^{NB}-2\right)\left(V_{in-}-V_{th}\right)+\left(n\right)\left(V_{ref-}-V_{th}\right)+\left(2^{NB}-2-n\right)\left(V_{ref+}-V_{th}\right)\right)$$

where NB is the quantizer number of bit and n is the comparator index number($0 \leq n \leq 2^{NB}$). W_1 and L_1 are the width and length of the elementary transistor. The equality between G_R and G_L is reached for the following differential input voltage,

$$V_{in,th} = \frac{2^{NB}-2-2n}{2^{NB}-2}\left[V_{ref+}-V_{ref-}\right] \tag{1}$$

which is the nth comparator threshold voltage. Therefore the comparator threshold voltages can be set by selecting the number of transistors connected to V_{ref+} or V_{ref-} in each branch.

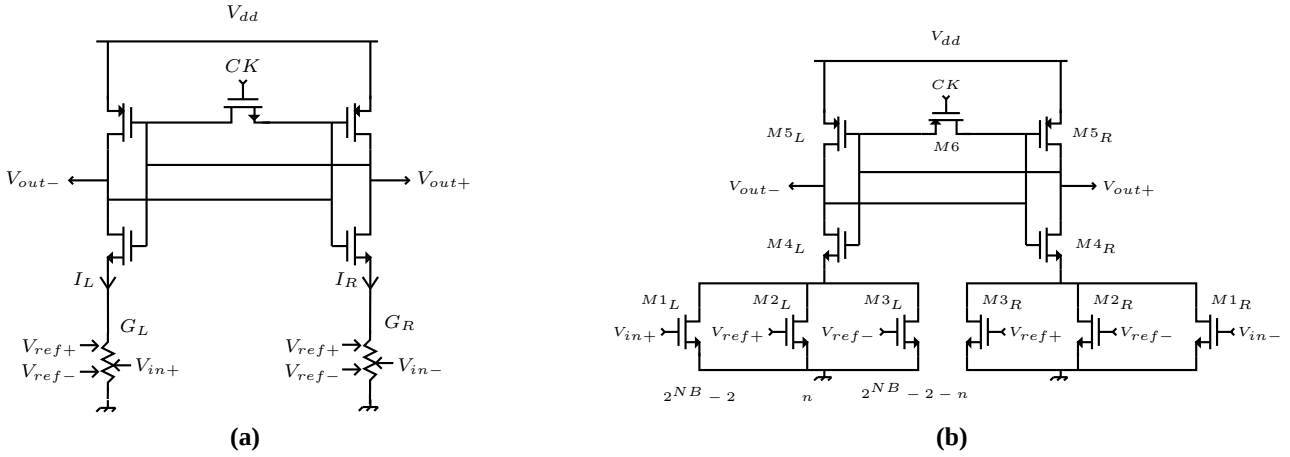

Figure 3. Comparator topology principle.

3. DESIGN OF THE DIFFERENTIAL COMPARATOR

3.1. Effects of Mismatch

Eq. (1) holds true only if there is no mismatch between transistors M1-M2-M3, on both sides of a comparator. Assuming the transistors threshold voltage in the two branches differs by ΔVth, eq. (1) becomes

$$V_{in,th} = \frac{2^{NB} - 2 - 2n}{2^{NB} - 2} [V_{ref+} - V_{ref-}] + 2\Delta V_{th} \quad (2)$$

We can see that the comparator threshold voltages are directly modified by the transistor's threshold voltage deviation ΔV_{th}. The comparator input offsets will be at least equal to this deviation.

A threshold voltage mismatch of transistor M4 results in a mismatch of the drain-to-source voltages of the triode transistor, between the lefthand and righthand branches. This can cause a very significant difference of the branch currents. If the current deviation ΔI due to mismatch on M4 is greater than the maximum amplitude of the current change due to input voltage, the current flowing through the right and left branches may even never become equal. This effect is illustrated in figure 4.

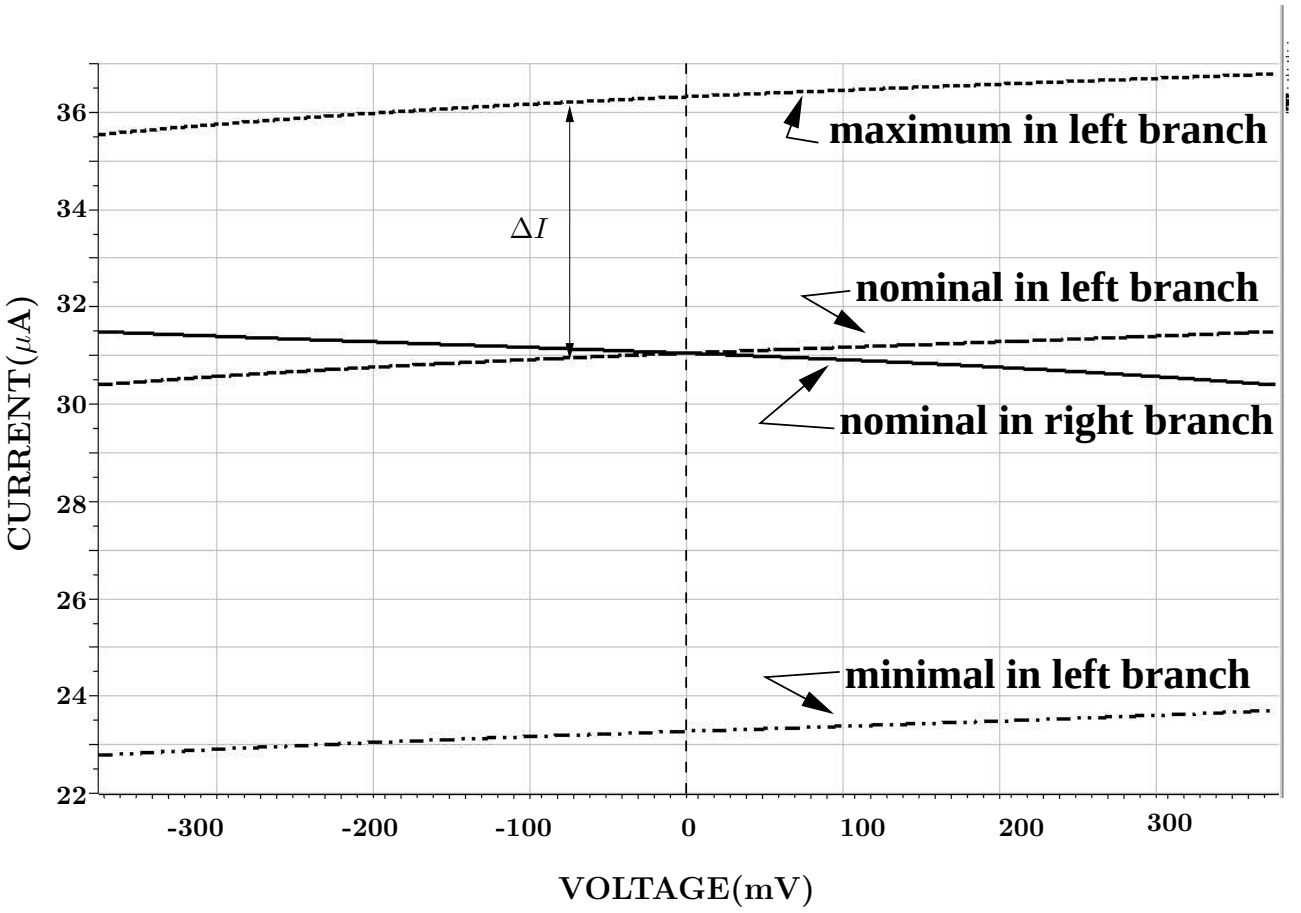

Figure 4. Illustration of the mismatching effects. Currents (A) in both branches of the 8th comparator (n=7) versus differential input voltage(V), in nominal case and resulting from Monte Carlo analysis(minimum and maximum cases). The nominal threshold voltage is $0V$ for this comparator.

3.2. Gain and Matching Improvements

In order to minimize the effects described in the previous section, the dimensions of transistors M1-M4 must be large enough to reduce their threshold voltage deviation. These transistors must be carefully drawn using appropriate layout techniques. In our design the transistors in triode region are distributed on a matrix around a common center, and are inter-digitized when they are on the same line.

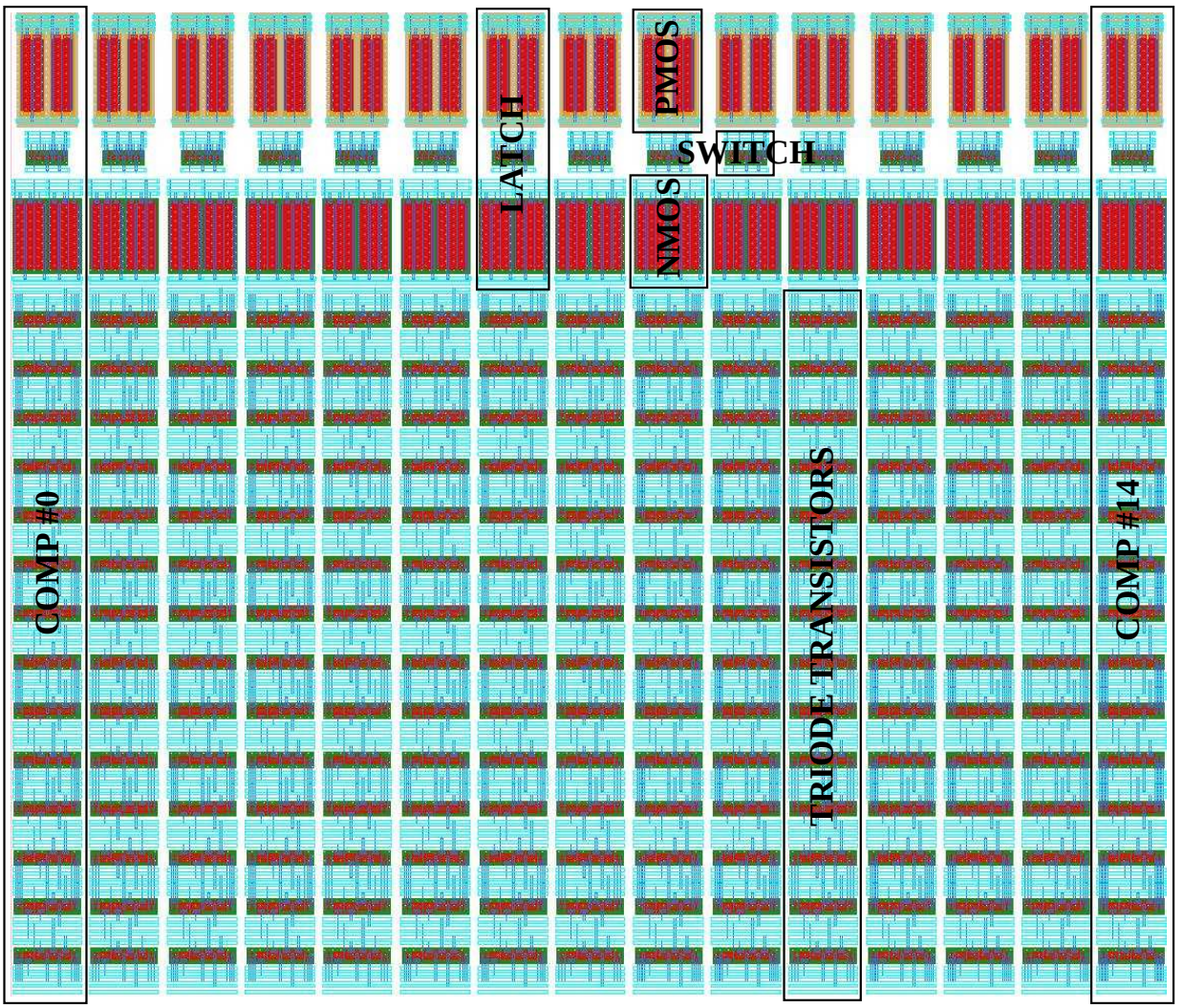

Figure 5. Layout placement.

The transconductance between the differential input signal and the branch currents can be raised to reduce the input offset. At first order this variation depends on the ratio between the transconductance of transistor M4 and the total transconductance of transistors M1-M2-M3. If gm_4 is dominating $gm_{1,2,3}$, transistor M4 sets the current in a branch and its variation with the input signal will be small. To improve the total gain we have to raise M1-M2-M3 transconductance. Assuming its expression is

$$gm_{1,2,3} = \mu_n C_{ox} \frac{W_1}{L_1} V_{ds1}$$

.

one way to raise it, is to increase the drain to source voltage of these transistors, while keeping it below the saturation voltage in order to stay in the triode region.

3.3. Design trade-offs

In order to reduce the mismatch of the transistors in triode region, it is advised to not use minimum channel length. By increasing the length, the transistor threshold voltage value is decreased. As a result, either a smaller

value for the minimal input voltage can be accepted, or the drain to source voltage V_{ds1} can be raised to reduce the offset voltage. However increasing the drain to source voltage of transistors M1-M2-M3 decreases the effective gate voltage of M4 and worsens the current mismatch error.

By increasing the inverter transistor lengths, the current mismatch is reduced but the gate capacitance C_{gs} is increased. Assuming that the latch is loaded by a standard inverter cell, the latch output capacitances are dominated by the gate capacitance of the latch inverters. To carry the same current, if the transistor length grows, the width must grow in the same proportions. As C_{gs} is proportional to WL product the load capacitance of the latch grows quadratically with transistor length increase. The set up time of the latch will increase drastically.

The layout area is dominated by transistor M1-M2-M3. (fig 5) For a given drain-to-source voltage V_{ds1}, minimum size transistor for the element width of M1-M2-M3 sets the power consumption. It can be further reduced by increasing the transistor length, at the cost of a corresponding increase in the layout area.

During the optimization of the circuit, V_{ds1}, the branch currents and the transistor lengths have been chosen as independent variables. First, the dimensions of transistors M1-M2-M3 are calculated. This can be done quite easily by taking all gate voltages equal to the common mode voltage. This reproduces quite accurately the situation close to the threshold voltage of the comparator. Then, the inverters are sized to provide in the reset phase an output voltage of half the supply voltage. The independent variables are tuned to optimize the comparator speed and offset voltage.

The switch does not affect the current deviation, so its length could be chosen to the minimal process value. The width is determined by simulation to keep the reset time smaller than the settling time of the comparator.

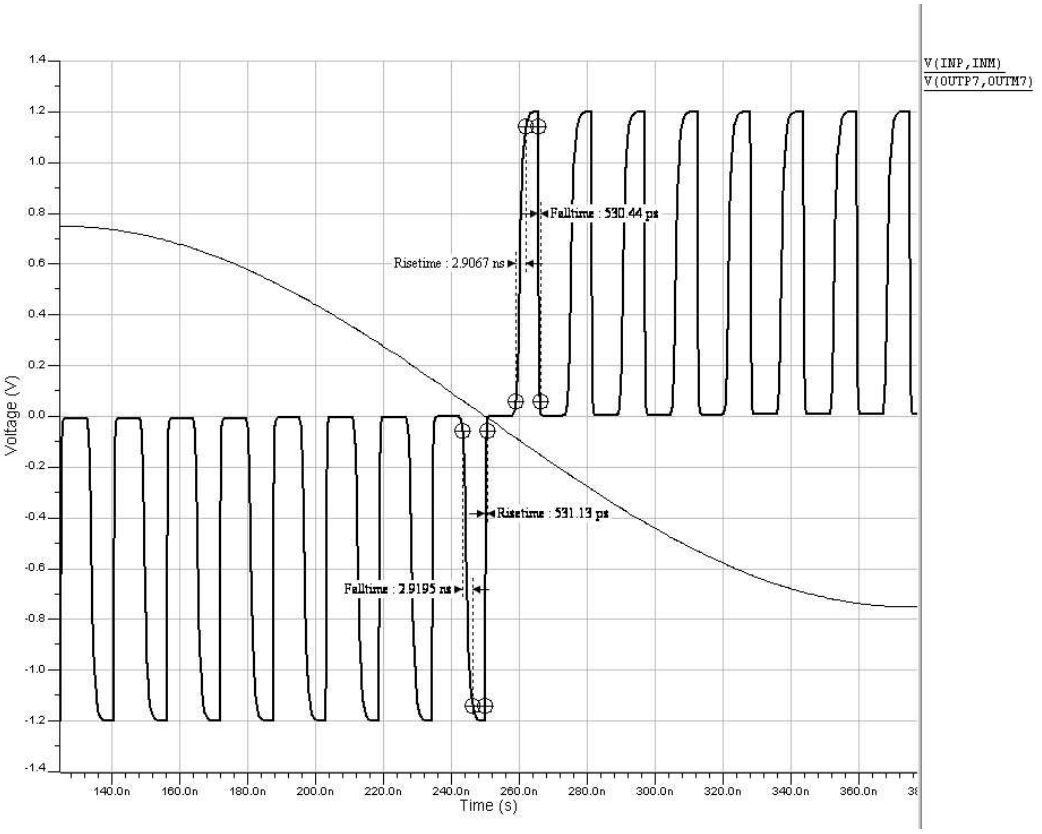

Figure 6. Transient analysis of one comparator. The maximum sample frequency is about 300MHz.

The comparator was designed using a standard $0.13\mu m$ CMOS technology, under $1.2V$ supply voltage. The minimum input voltage accepted, to keep transistor M1 gate-to-source voltage above the threshold voltage V_{th1},

is $0.45V$. As the maximum input value is the supply voltage, the input common mode voltage is $0.825V$. The reference voltage V_{ref+} (respectively V_{ref-}) is set one quantization step below the maximum input voltage (respectively above the minimum input voltage). The final transistor dimensions are presented in Table 1 for a drain-to-source voltage V_{ds1} equal to $150mV$. The current flowing through the comparator's branches for the threshold voltage is about $80\mu A$. The layout placement of the 15 comparators is shown in figure 5 and was generated using the CAIRO+[7,8] environment. The die area is $0.017mm^2$.

trans	$L(\mu m)$	$W(\mu m)$
M_1	1.3	$14 * 0.5$
M_4	0.91	23.3
M_5	0.91	17.3
M_6	0.13	2.6

Table 1. transistor dimensions.

4. SIMULATION RESULTS

The comparators threshold voltages are calculated using a DC analysis during the reset phase. The extracted value is the differential input voltage for which the currents flowing in the two branches become equal. Repeating this measure in a Monte Carlo analysis we obtain the average value and standard deviations of the comparators threshold value (Table 2).

comparator	theory $[V]$	average value $[V]$	standard deviation $[mV]$
0	-0.328125	-0.3743	13.624
1	-0.28125	-0.2788	13.639
2	-0.234375	-0.2306	13.924
3	-0.1875	-0.1831	12.616
4	-0.140625	-0.1377	12.413
5	-0.09375	-0.0911	12.804
6	-0.046875	-0.0457	11.986
7	0.0	0.00031	12.911
8	0.046875	0.4442	12.536
9	0.09375	0.0902	12.466
10	0.140625	0.1365	13.252
11	0.1875	0.1841	13.182
12	0.234375	0.2306	13.055
13	0.28125	0.2791	13.325
14	0.328125	0.3276	12.959

Table 2. Threshold voltage, Theory vs statistical analysis.

The dynamic characteristic of the circuit is simulated for a sinusoidal input signal of maximum amplitude, with a frequency of 2MHz and for a 64MHz sampling frequency. The simulation results are shown on figure 6. The maximum settling time measured is about 3ns for a reset time of 530ps. The maximum expected sampling frequency is 280MHz.

The simulation gives a static power consumption for the whole comparator of 3.8mW during the reset phase, and of 2.6 mW in dynamic operation at 64Msample/s.

5. CONCLUSION

In this paper, a fully differential 4 bit flash A/D converter which uses a fully differential dynamic comparator, using only MOS transistors, that is optimized for speed and accuracy has been designed. An analysis was given

of the effects of MOS transistor impairments on converter offset accuracy. The A/D converter is suitable for continuous-time $\Sigma\Delta$ modulator with multi-bit quantizer.

ACKNOWLEDGMENTS

The authors gratefully acknowledge the help of Pierre Nguyen Tuong for providing the CAIRO+ environment, Vincent Bourguet with the layout design. They would like to thank their colleagues in the CAIRO+ team, with special mention to Jacky Porte, for the fruitful discussions.

REFERENCES

1. T. B. Cho and P. R. Gray, "A 10 B, 20 Msample/s, 35 mw Pipeline A/D Converter," *IEEE Journal of Solid State Circuits* **30**, pp. 166–172, 1995.
2. P. Jespers, *Integrated Converters : D to A and A to D Architectures, Analysis and Simulation*, Oxford University Press, Oxford, 2001.
3. Y. Geerts, M. Steyart, and W. Sansen, *Design of multi-bit Delta-Sigma A/D Converters*, Kluwer Academic Publishers, Boston, 2002.
4. S. H. Lewis and P. R. Gray, "A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter," *IEEE Journal of Solid State Circuits* **22**, pp. 954–961, 1987.
5. L. Sumanen, M. Waltari, and K. Halonen, "A Mismatch Insensitive CMOS Dynamic Comparator for Pipeline A/D Converters," *ICECS 2000*, pp. 33–35, 2000.
6. M. Pelgrom, J. Rens, M. Vertregt, and M. Dijkstra, "A 25-Ms/s 8-bit CMOS A/D Converter for Embedded Application," *IEEE Journal of Solid State Circuits* **29**, pp. 879–886, 1994.
7. D. Khalil, M. Dessouky, V. Bourguet, M. Louërat, A. Cathelin, and H. Ragai, "Evaluation of Capacitor Ratios in Automated Accurate Common-Centroid Capacitor Arrays," *ISQED 2005*, pp. 143–147, 2005.
8. H. Aboushady, L. de Lamarre, N. Beilleau, and M.-M. Louërat, "Automatic Synthesis and Simulation of Continuous-Time Sigma-Delta Modulators," *DATE 2004*, pp. 674–675, 2004.