CAPTURING RC-INTERCONNECT EFFECT IN CROSSTALK ANALYSIS

P. RENAULT, P. BAZARGAN-SABET
UNIVERSITY OF PARIS 6, FRANCE

KEYWORDS: Verification tools, RC-circuit of interconnect

ABSTRACT: With deep submicron (DSM) technologies, coupling capacitance and resistance-capacitance of the interconnect, can have a significant impact on signal integrity and timing performance. In this paper, first we briefly describe a crosstalk noise evaluation method which determines the crosstalk noise but neglects the RC of the interconnect. Then, we propose an approach to extend this method taking into account the RC. It consists in modelling the RC-network with a simplified circuit, which can easily be integrated into the crosstalk noise evaluation tool. We determine the output waveform of the RC-network according to the input. Then, we compute the parameters of the simplified circuit. We experimentally verify that the proposed method can accurately estimate the crosstalk noise.

INTRODUCTION

Approximately 10 years ago, with the micron technologies, chip designers focus on device analysis. The parasitic elements such as coupling capacitance/inductance, resistance-capacitance-inductance of interconnects, transistors diffusion drain and source capacitance were neglected.

The advent of deep submicron technologies has changed all of this: with thinner metal width, coupling capacitance between neighbouring signal and the intrinsic resistance[10] of a wire can not be neglected. These parasitic elements can generate functional/timing failure.

New verification tools have been created to detect functional failure [3][4] and timing failure [1][6]. In addition, new design methodologies [11] and routers [13][14], have been proposed to take the coupling capacitance into account.

Several methods have been proposed to take into consideration RC-networks. For example, [7] and [8] propose to determine the crosstalk peak noise with RC of interconnect. These methods are quite simple and give a good accuracy for very small RC-networks. But, due to the complexity of the RC-networks and the huge number of parasitic elements these methods are not accurate enough. Besides, some works [5] have been carried out to approximate the delay due to interconnect without coupling capacitance. AWE [9] and the first three moments method [12] are the main methods used in the industrial tools. In [12], the output waveform of an RC-network is modelled in the time domain by

$$x_{out}(t) = k_1.e^{p_1.t} + k_2.e^{p_2.t} \tag{1}$$

which can be written in the frequency domain as

$$\hat{H}_{out}(p) = \frac{k_1}{p-p_1} + \frac{k_2}{p-p_2} \tag{2}$$

Expanding $\hat{H}_{out}$ around $s=0$ gives

$$\hat{H}_{out}(p) = -\sum_{j=0}^{+\infty} \frac{k_1}{p_1^{j+1}} p^j - \sum_{j=0}^{+\infty} \frac{k_2}{p_2^{j+1}} p^j \tag{3}$$

where k_1, k_2, p_1, p_2 are unknown.
To determine the four parameters, the first three moments method uses the transfer function of the RC-network H_{out}, which can be written as

$$H_{out}(p) = \frac{X_{in}(p)}{X_{out}(p)} \tag{4}$$

Using the series expansion of H_{out} about $s=0$ gives

$$\tilde{H}_{out}(p) = m_0 + m_1.p + m_2.p^2 + m_3.p^3 + ... \tag{5}$$

where m_i is known.
Then, we can used the m_0 to m_3 moments to determine the parameters k_1, k_2, p_1, p_2. It gives :

$$p_1 \approx \frac{m_2}{m_3} \qquad p_2 \approx p_1 . \frac{\frac{m_0}{m_1} - \frac{m_1}{m_2}}{\frac{m_1}{m_2} - \frac{m_2}{m_3}} \tag{6}$$

$$k_1 = \frac{1+m_1 p_2}{p_1 - p_2} p_1^2 \qquad k_2 = \frac{1+m_1 p_1}{p_1 - p_2} p_2^2$$

[9] is the extension of [12] for a variable number of moments. These methods are accurate. As soon as one try to integrate this RC-reduction into a verification tool, however, two difficulties arise. It is well known that AWE [9] can be unstable. A criticism we would raise is how integrate the model reduction in a crosstalk or timing evaluation tool ?

In this paper, we propose to model the RC-networks with a simplified circuit, which can be used in verification tools. This paper is organised as follows. First, we describe the crosstalk noise evaluation tool. Then, we expose our reduction method. Finally, we show the experimental results.

A FIRST TOOL

The aim of a crosstalk analysis tool is to determine the amount of noise injected on each signals during the transition of its neighbours. Our approach relies on two main points. On one hand, we propose an analytic noise model that leads to the expression of the noise. From this expression, the maximal voltage induced by the crosstalk noise can be derived. On the other hand, the tool provides a method to determine the aggression configurations, i.e. which of the aggressors of a signal contribute to the noise produced on that signal. This method is based on a timing analysis that exhibits the time intervals where each signal may switch.

The aggression configurations

In a real size circuit, a signal may be coupled through a crosstalk capacitance to thousands of signals. However, at a given time, not all of these aggressors produce a noise on the victim. The noise produced on the victim is due to the transition of the aggressors. The effects of these transitions increase the noise on the victim only if they occur in the same time and in the same direction. The proposed method uses a symbolic event-driven simulation engine to determine the instability intervals of each signal (see [2]). The output of a gate become unstable (may switch) if one its input is unstable. The instability interval of the input is transmitted to the output after a delay. This delay is the propagation delay between the input and the output and depends on the type of the transition (falling or rising). The aggression configurations on each signal are determined from the instability intervals of its aggressors. An aggression configuration is a subset of the victim's aggressors. An aggressor is in a aggression configuration if its instability intervals intersect the instability intervals of all the other aggressors of the configuration. The result of this step is a set of aggression configurations calculated for each signal considered as a victim. Then, the noise model has to compute the noise peak voltage for each of these configurations.

The noise model

This model gives an expression of the noise produce on a victim for a given configuration (see [10]). The peak voltage induced by the crosstalk noise is derived from this expression. To obtain a realistic expression of the noise one has to take care of the environment of the victim. Obviously, the aggression configuration determines which aggressors participate to the produced noise (active aggressors). However, the presence of the other aggressors (silent aggressors) has an impact on the noise. Silent aggressors absorb a part of the current created by the active aggressors. This tends to reduce the noise on the victim. Besides, each active aggressor has some capacitance coupling with other victims (secondary victims). The noise produced during the transition of an aggressor is shared by all of its victims. Thus, the presence of secondary victims tends also to reduce the noise on the considered victim.

The proposed approach uses several approximations to obtain an analytic expression of the noise produced on the victim. First, a simple resistor approximates signal drivers. Then, silent aggressors are modelled as a ground capacitance added to the victim's line. In the same way, secondary victims are modelled as an additional ground capacitance seen by the active aggressors. In the last approximation step, each active aggressor is represented as an independent current source.

Applying these approximations, an equivalent scheme (see fig. 1) is obtained for each victim depending on the aggression configuration. In this circuit, R_v represents

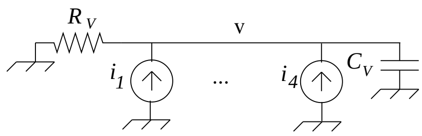


Fig. 1. Final equivalent circuit

the equivalent resistance of the victim's driver, C_v the total ground capacitance seen by the victim and the current sources i_k the active aggressors. The noise expression is obtained resolving the equation characterising the circuit.

MODELING RC-INTERCONNECT

Even if the previous model gives a good estimation of the noise, in deep submicron design the line that connects the output of a gate to the input of a receiver cannot be considered as a simple equipotential. In fact, the resistance of this line is far to be negligible. Taking into account this resistance makes the crosstalk analysis much more complex. In deep submicron designs, each signal is modelled as a distributed RC circuit connected to its aggressors through a distributed coupling capacitance.

In this paper we propose a method to reduce this coupled RC circuit into a simple scheme such as it can be taken into account in the method presented above.

Stating the problem

Let's consider an RC-network composed by $m+1$ nodes numbered of 0 to m. We note $n+1$ to m the initial point of a wire, called input node. $n+1$ to m are the final point of a wire, called output node and 1 to n are the node not connect to the initial or final point of the wire, called internal nodes. 0 is the ground voltage. Each RC-network can be characterised by a system of n equations:

$$S_t \begin{cases} G_1.x_1(t)+C_1.x_1'(t)=\sum\limits_{j=0}^{m} G_{1j}.x_j(t)+\sum\limits_{j=0}^{m} C_{1j}.x_j'(t) \\ \vdots \\ G_n.x_n(t)+C_n.x_n'(t)=\sum\limits_{j=0}^{m} G_{nj}.x_j(t)+\sum\limits_{j=0}^{m} C_{nj}.x_j'(t) \end{cases} \tag{7}$$

where

- $x_i(t)$ is the waveform of the node i in the time-domain.
- $x_i'(t)$ is the waveform first derivative.

- G_i is the total conductance of node i: $G_i = \sum_{l=0}^{m} \frac{1}{R_{il}}$
- C_i is the total capacitance of node i: $C_i = \sum_{k=0}^{m} C_{ik}$
- G_{il} is the conductance between node i and l.
- C_{ik} is the capacitance between node i and k.

The resolution of this system gives, for each node, the following solution

$$x_i(t) = \sum_{k=1}^{n} a_{ik}.e^{-h_k.t} + a_{i0} \tag{8}$$

where a_{i0} is the known voltage when $t \to +\infty$ of the node i, a_{ik} a coefficient in Volt and h_k a frequency.
Next, we present an exact waveform evaluation technique that will be used to provide simplified circuit parameters.

Determining the Output Waveform

We present our method for determining the output waveform without approximation. First, we determine the n frequencies. To determine the n frequencies, we find n equations. In an RC-network, we know the initial value of the node i, called x_{i0}. It gives a first equation:

$$a_{i1} + a_{i2} + \cdots + a_{in} = x_i(0) - a_{i0} = x_{i0} \tag{9}$$

In order to find the $n-1$ other equations, we transform, by computation, the initial system S_t in an equivalent system without coupling capacitance:

$$S_{eq} \begin{cases} G'_1.x_1(t) + C'_1.x'_1(t) & = \sum_{j=0}^{m} G'_{1j}.x_j(t) \\ \vdots & \\ G'_n.x_n(t) + C'_n.x'_n(t) & = \sum_{j=0}^{m} G'_{nj}.x_j(t) \end{cases} \tag{10}$$

We know not only the initial value of node i but also the initial values of all the nodes of the circuit. Thus, we can determine the initial value of the first derivative of the node i, $x'_i(0)$ noted x_{i1}. On the other hand, from the expression of the node i (eq. 8), we obtain a second equation

$$a_{i1}.h_1 + a_{i2}.h_2 + \cdots + a_{in}.h_n = -x_{i1} \tag{11}$$

By the same way, we obtain a set of equations (S_{der}) where $a_{i1}, \cdots, a_{in}$ and $h_1, \cdots, h_n$ are the variables.

$$S_{der} \begin{cases} \sum_{j=1}^{n} h_j^0 a_{ij} & = (-1)^0 x_{i0} \\ \vdots & \\ \sum_{j=1}^{n} h_j^n a_{ij} & = (-1)^n x_{in} \end{cases} \tag{12}$$

To solve this non-linear system (S_{der}), we express the frequencies h_i without the coefficients a_{ij}. We modify the system S_{der} to make it linear by eliminating the variable a_{ij}. First, we eliminate the variable a_{i1}

$$\begin{cases} \sum_{j=2}^{n} h_j^0 \quad (h_j - h_1)a_{ij} = (-1)^1(x_{i1} + h_1 x_{i0}) \\ \vdots \\ \sum_{j=2}^{n} h_j^{n-1}(h_j - h_1)a_{ij} = (-1)^n(x_{in} + h_1 x_{in-1}) \end{cases} \tag{13}$$

After n iterations, we obtain, for the node i, the equation:

$$\sum_{i=1}^{n} h_i x_{in-1} + \sum_{i=1}^{n} \sum_{j=i+1}^{n} h_i h_j x_{in-2} + \cdots + \prod_{i=1}^{n} h_i x_{i0} = -x_{in} \tag{14}$$

where h_i are the variables. For simplify, we note $\sigma_{n-1}, \cdots, \sigma_0$ such as the previous equation can be written as

$$\sigma_{n-1}x_{in-1} + \sigma_{n-2}x_{in-2} + \cdots + \sigma_0 x_{i0} = -x_{in} \tag{15}$$

Applying this equation on each node, we obtain n equations with n unknowns (σ_i) which can be written as

$$\begin{pmatrix} x_{10} & \cdots & x_{1n-1} \\ \vdots & \vdots & \vdots \\ x_{n0} & \cdots & x_{nn-1} \end{pmatrix} \begin{pmatrix} \sigma_0 \\ \vdots \\ \sigma_{n-1} \end{pmatrix} = - \begin{pmatrix} x_{1n} \\ \vdots \\ x_{nn} \end{pmatrix} \tag{16}$$

σ_i are obtained from the resolution of this system. Then, we determine the frequencies h_i from σ_i by computing the root of the polynomial $P_n(h)$

$$P_n(h) = h^n - \sigma_{n-1}h^{n-1} + \sigma_{n-2}h^{n-2} + \cdots + (-1)^n \sigma_0 \tag{17}$$

Now, all the frequencies h_i are known. We compute the coefficients a_{ij} with the equation system S_{der}.

Simplified Circuit

In crosstalk evaluation tools, there are two kinds of signal, the aggressors and the victim. Note that the main goal of the simplified circuit is to be integrated into crosstalk verification tools. To this end, we have merely chosen a simplified circuit composed by two parts: the victim model and the aggressor model.
Figure 2 shows the output of a victim signal without coupling capacitance and the model used for the victim signal. This model has an exponential form and is a simple RC element.

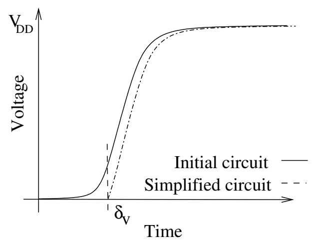


Fig. 2. Output signal of the initial and simplified circuit

The victim model gives the following voltage equation

$$\hat{x}_{out}(t) = \begin{vmatrix} 0 & t \in [0, \delta_v] \\ V_{DD}.(1 - e^{-\frac{(t-\delta_v)}{\tau_v}}) & t \in [\delta_v, +\infty[\end{vmatrix} \tag{18}$$

where $\tau_v = R_{lv}C_{lv}$

To determine τ_v and δ_v such as $\hat{x}_{out}$ is a good approximation of x_{out} (initial circuit). We use the distance d between two functions and defined as

$$d(\hat{x}_{out}, x_{out}) = \int_0^{+\infty} (x_{out}(t) - \hat{x}_{out}(t))^2 dt \qquad (19)$$

$\hat{x}_{out}$ is a good approximation of x_{out} if $d(\hat{x}_{out}, x_{out})$ is minimal. It gives

$$\left\{ \begin{array}{lcl} \dfrac{\partial}{\partial \delta_v} d(\hat{x}_{out}, x_{out}) & = & F_1(\delta_v, \tau_v) = 0 \\ \dfrac{\partial}{\partial \tau_v} d(\hat{x}_{out}, x_{out}) & = & F_2(\delta_v, \tau_v) = 0 \end{array} \right. \qquad (20)$$

This non-linear system is solved using the Newton-Raphson method with partial derivation, which gives δ_v and τ_v.

Now, we have to determine the aggressor parameters. In [10] the active aggressors a_i are replaced by an equivalent current source defined as $I_{ai}e^{-\frac{t}{\tau_{a_i}}}$. This approximation is really simple and the current generated by several aggressors can be added. We have chosen to use a similar approximation. However, in order to take into account the RC-networks, we have to modify this model. The noise of a victim composed by n nodes coupled with an aggressor is significant after some delay. Thus, we propose to add a delay δ_a to the current source describe in [10]. The model of the aggressor signals is a current source $I_{ai}e^{-\frac{t-\delta_{a_i}}{\tau_{a_i}}}$. The output signal can be expressed as

$$\hat{x}_{out}(t) = \left| \begin{array}{ll} 0 & t \in [0, \delta_a] \\ -\dfrac{I_a \tau_a}{C_{lv}}.(1 - e^{-\frac{t-\delta_a}{\tau_a}}) & t \in [\delta_a, \delta_a + \delta_v] \\ \dfrac{I_a \tau_a}{C_{lv}}[(1 - \dfrac{\tau_a}{\tau_a - \tau_v}.e^{-\frac{\delta_v}{\tau_a}}).e^{-\frac{t-(\delta_a+\delta_v)}{\tau_v}} & \\ +\dfrac{\tau_v}{\tau_a - \tau_v}.e^{-\frac{t-\delta_a}{\tau_a}}] & t \in [\delta_a + \delta_v, +\infty[\end{array} \right. \qquad (21)$$

The simplified circuit of an RC-network composed by n aggressors is shown in figure 3.

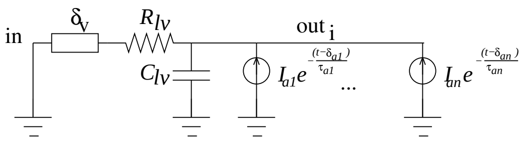


Fig. 3. Simplified circuit for an RC-network composed by n aggressors

Integration in the crosstalk evaluation tool

Let's consider an output signal out_i coupled with n active aggressors. The simplified circuit is shown in figure 4. R_v and C_v represent the victim driver. The resistor and capacitor of the aggressor drivers are take into account in the current sources.

We have seen in the introduction that the instability period can be computed with the gate delay and the instability periods of the input signals. But, the modelization of the RC-networks adds some delay on the aggressor interconnection. Thus, to determine which aggressors make a

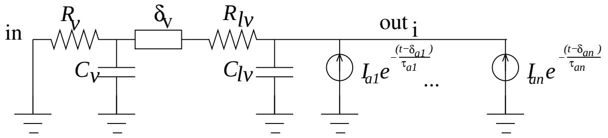


Fig. 4. Simplified circuit of an output signal out_i coupled with n active aggressors

transition in the same time, we have to take into consideration the delay δ_a in the static instability analysis.

Finally, the simplified circuit for the crosstalk noise analysis is shown in figure 5.

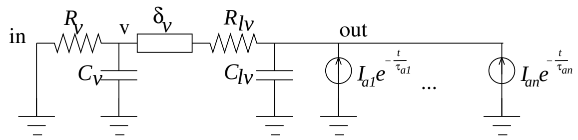


Fig. 5. Simplified circuit for crosstalk noise analysis

We have

$$x_{out}(t) = K_1.e^{r_1.t} + K_2.e^{r_2.t} + \sum_{i=1}^{n} K_{ai}e^{-\frac{t}{\tau_{ai}}} \qquad (22)$$

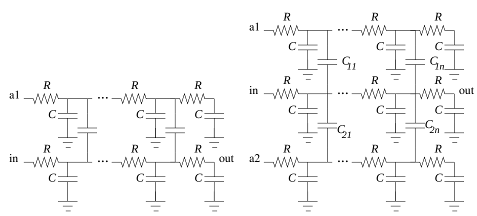
where τ_1, τ_2 are the time constants and depend of the values of the resistors and capacitors. K_1, K_2 and K_{ai} are some coefficient.

In order to determine the crosstalk noise of the signal out, we determine with the Newton-Raphson method the time t_{noise} which $x'_{out}(t_{noise}) = 0$. Then, the noise peak is

$$V_{noise} = K_1.e^{r_1.t_{noise}} + K_2.e^{r_2.t_{noise}} + \sum_{i=1}^{n} K_{ai}e^{-\frac{t_{noise}}{\tau_{ai}}} \qquad (23)$$

EXPERIMENTAL RESULTS

A prototype tool that implements all the concepts described in this article has been developed. This prototype has been tested over two kind of RC-networks: networks with coupling capacitance with two outputs or three outputs (see fig. 6) and a variable number of internal nodes ranging from 50 to 500.



(a) two outputs (b) three outputs

Fig. 6. Network with coupling capacitance

Accuracy

In this section we compare the results obtained with the initial RC-circuit and the simplified circuit when $V_{DD} = 1V$.

Figure 7 shows the output signal of an RC-circuit composed by 100 nodes with one aggressor when the victim input signal is stable to V_{SS} and the aggressor input signal makes a transition from V_{SS} to V_{DD} and the simplified circuit.

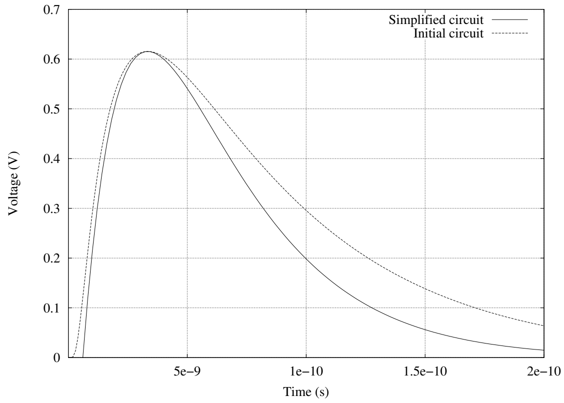


Fig. 7. Simplified circuit versus initial RC-circuit

We can see that the simplified circuit output is null for $t \in [0, \delta_a]$. Then, before the peak, the curves obtained with the initial and simplified circuit are closed. The peak obtained with the two curves has the same value. But, after the peak, the simplified circuit gives a satisfying approximation of the initial circuit.

The table 1 presents the results obtained with the initial circuit composed by a victim coupled with two active aggressors and simplified circuit.

TABLE 1. Peak value and error with the proposed method compared to an electrical simulation

Number of node	Simplified circuit (V)	Initial circuit (V)	Error
100	0.202	0.182	2.0%
150	0.156	0.182	2.6%
200	0.138	0.174	3.6%
250	0.118	0.144	2.6%
300	0.156	0.182	2.6%
350	0.098	0.182	8.4%

The error is equal to 3.56% for a 200-nodes circuit and remains less than 10%.

The table 2 presents the peak voltage obtained with the electrical simulation of the initial circuit, with the first three moments method and with our simplified circuit. We used the RC-networks composed by a victim coupled with two, three or four active aggressors and a variable number of internal node and a variable values of resistor and capacitor.

We can see, that the error obtained with the simplified circuit is closed to the one obtained with the first three moments method. However, with the use of simplified circuit we can integrate the presence of interconnect into verification tool.

Execution Time

The figure 8 shows the execution time obtained, on a 1 GHz PC computer with 1 GByte RAM, to determine the frequencies h_j with the proposed method. We can see

TABLE 2. Peak value and error with the first three moments method and with the simplified circuit compared to an electrical simulation

# aggr.	Elec. simu.	First 3 moment	Error	Simpl. circuit	Error
2	0.296	0.258	3.8%	0.318	2.2%
3	0.522	0.420	10.2%	0.492	3.0%
3	0.620	0.500	12.0%	0.500	12.0%
4	0.632	0.512	12.0%	0.498	13.4%
4	0.546	0.502	4.4%	0.506	4.0%

that it takes nearly 50 seconds to compute the frequencies of an RC-circuit with 500 nodes and 3 outputs.

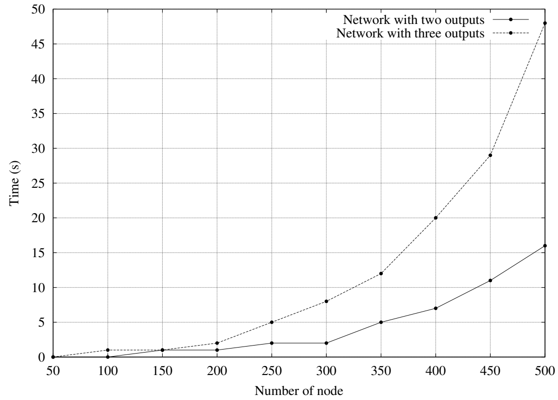


Fig. 8. Execution time for determining the frequencies

Figure 9 shows the execution time obtained to compute the coefficients a_{ij}. For an RC-circuit with 500 nodes and 3 output, it takes nearly 25 seconds to determine the coefficients.

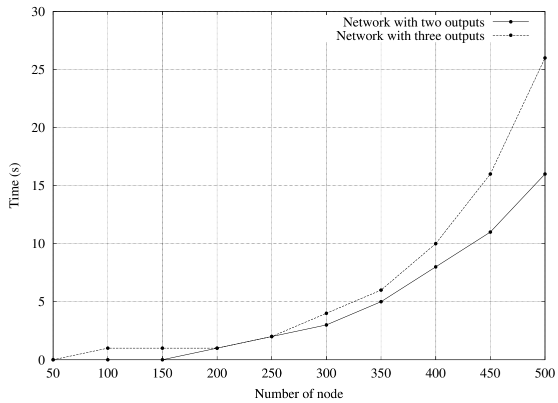


Fig. 9. Execution time for determining the coefficients

Discussion on the proposed method

It must be emphasised that, the parameter evaluation of the simplified circuit can be apply on output obtained with other method such as electrical simulation or AWE. In fact, to decrease the computation time of the proposed method, we can determine the output waveform according to the input with fast method. Then, we can determine the parameters of the simplified circuit.

The proposed method consists in modelling each aggressor by a current source. An RC-circuit composed by n aggressors is modelled by n current sources. Then, the model is integrated into a verification tool. In the contrary, no equivalent circuit is built by the first three moments method. For each aggression configuration, the first three moments method has to be apply in order to reduce the RC-circuit and evaluate the peak noise. For an RC-circuit with n aggressors, the maximum number of aggression configuration is

$$\sum_{p=1}^{n} C_n^p = \sum_{p=1}^{n} \frac{n!}{p!(n-p)!}$$

For example, 1023 aggression configurations exist for an RC-circuit with 10 aggressors. To conclude, the first three moments method is faster than the proposed method but the gain can be lost because of the number of aggression configuration.
The results show that 50 seconds are needed to model an RC-circuit with 500 nodes. Such an RC-circuit represents global interconnect. In a real circuit, the local or intermediate interconnect are modelled with nearly 100 nodes. With the proposed method, it takes 2 seconds to reduce such an RC-circuit. Nevertheless, 2 seconds is too long for a 1 million signals circuit. In fact, even the first three moments method is inadequate. An answer consists in applying two steps. First, a very simple and fast method determines the set of signals for which a crosstalk noise can appear. This set of signals represents a very small percentage of the total number of signals. Then, the proposed method is apply on this set of signals. Thus, the computation time of the proposed method is not unacceptable.

CONCLUSION AND FUTURE WORKS

In this paper, we propose a method to reduce the RC-circuit with coupling capacitance. This method is composed by two steps. First, we determine the output waveform according to the input. Then, we compute the parameters of the simplified circuit. We show that the proposed simplified circuit can be integrated into a noise evaluation tool. In addition, the peak noise obtained with the proposed method compared to an electrical simulation remains less than 10% of error.
The proposed method can be improved following two directions. First, we can develop new efficiency techniques to compute the output waveform. The second improvement concerns the process evolution. With very deep submicron processes the inductance of the interconnect can have a significant impact on the circuit. Thus, the method has to be modified to take into consideration the inductance of the interconnect.

THE AUTHORS

Dr. Patricia Renault and Dr. Pirouz Bazargan-Sabet are with the department of ASIM, LIP6, 12 rue Cuvier, Paris. The ASIM department of LIP6 focuses on the design of highly complex integrated circuits, the development of advanced CAD tools for VLSI, and hardware architecture of systems.
E-mail:patricia.renault@lip6.fr, pirouz.bazargan@lip6.fr

REFERENCES

[1] G. Avot, A. Greiner, MM. Lourat, D. Karim, A. Lester, and A. Debreil. Use of mutiphase stability intervals to handle crosstalk with the timing analyzer hitas. In *Proceedings of the Design Automation and Test in Europe Conference*, 2002.

[2] P. Bazargan-Sabet and P. Renault. Using symbolic simulation to exhibit worst case crosstalk noise configuration. In *Proceedings of the LATW*, 2003.

[3] M. Becer, R. Vaidyanathan, C. Oh, and R. Panda. Signal integrity management in an soc physical design flow. In *Proceedings of the ISPD*, 2003.

[4] P. Chen and K. Keutzer. Towards true crosstalk noise analysis. In *Proceedings of the ICCAD*, 1999.

[5] W. C. Elmore. The transient response of damped linear networks with particular regard to wideband amplifiers. *Journal of applied physics*, vol. 19, January 1948.

[6] M. Hashimoto, Y. Yamada, and H. Onodera. Capturing crosstalk-induced waveform for accurate static timing analysis. In *Proceedings of the ISPD*, 2003.

[7] A. B. Kahng, S. Muddu, and D. Vidhani. Noise model for multiple segmented coupled rc interconnects. In *Proceedings of the International Symposium on Quality Design*, 2001.

[8] P. Morton and W. Dai. An efficient sequential quadratic programming formulation of optimal wire spacing for crosstalk noise avoidance routing. In *Proceedings of the ISPD*, 1999.

[9] L. Pillage and R. Rohrer. Asymptotic waveform evaluation for timing analysis. *IEEE transactions on computer-aided design*, vol. 9, april 1990.

[10] P. Renault, P. Bazargan-Sabet, and D. Le Du. A mos transistor model for peak voltage calculation of crosstalk noise. In *Proceedings of the ICECS*, 2002.

[11] R. Saleh, D. Overhauser, and S. Taylor. Full-chip of udsm designs. In *ICCAD, IEEE/ACM*, pages 453–460, 1998.

[12] B. Tutuianu, F. Dartu, and L. Pileggi. An explicit rc-circuit delay approximation based on the first three moments of the impluse response. In *DAC, IEEE/ACM*, 1996.

[13] H. Xiang, K.Y. Chao, and M. Wong. An eco algorithm for eliminating crosstalk violations. In *Proceedings of the ISPD*, 2004.

[14] H. Zhou and D.F. Wong. Global routing with crosstalk contraints. In *Proceedings of the DAC*, 1998.