# Automatic Translation of SystemC Simulation Model From VHDL RTL Model : a Semantic Approach

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March 20, 2006

## Goal

**RTL2CFSM** uses a semantic approach to perform both :

- **Syntax Translation** : VHDL to SystemC
- **Abstraction** : Synthesizable RTL to FSM

## Method

We propose these following steps :

1. **VHDL Parsing** creates Petri Networks representing simulation semantic;
2. **Semantic Analysis** allows to obtain a set of single assignments;
3. **FSM Abstraction** determines a mapping between single assignments and FSM functions;
4. **SystemC driving** produces module implementation in SystemC language.

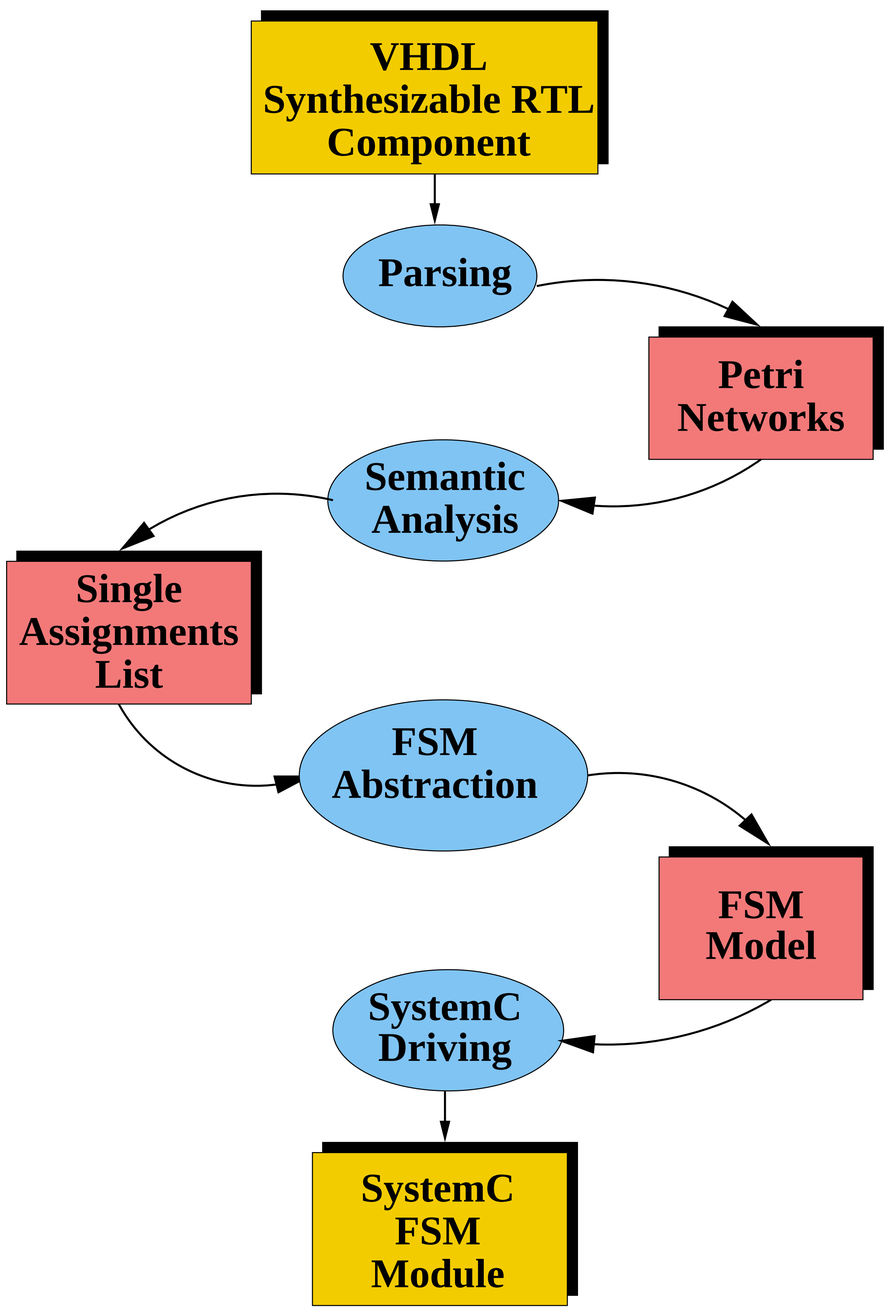


FIGURE 1: RTL2CFSM Workflow

## FSM Abstraction

FSM abstraction consists in finding a mapping between single assignments and FSM functions.
FSM abstraction has two steps :

- Construction of an Extended Boolean Network from single assignments;
- Support analysis to tag each single assignments $ASG_A$.

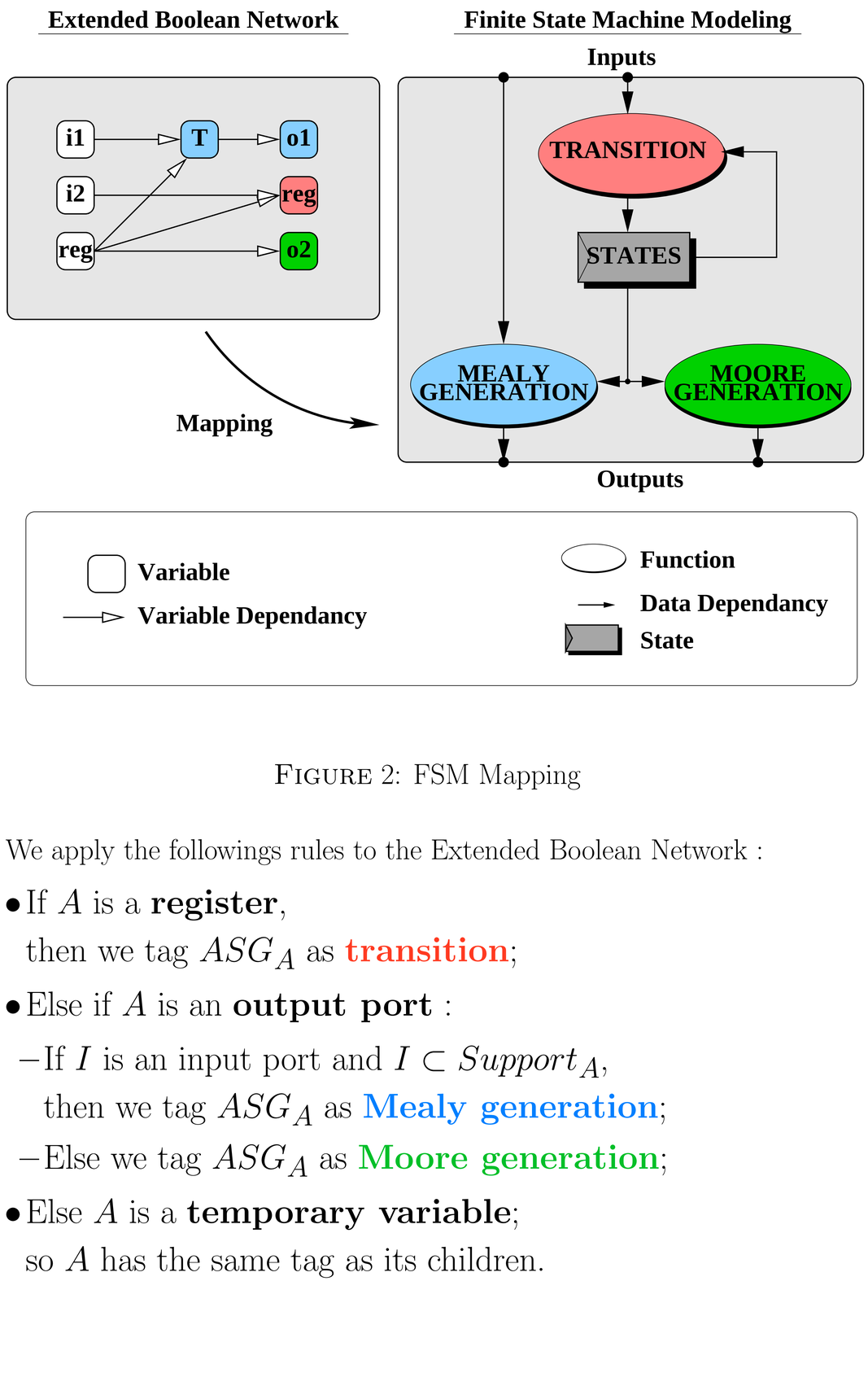


FIGURE 2: FSM Mapping

We apply the followings rules to the Extended Boolean Network :

- If $A$ is a **register**,
  then we tag $ASG_A$ as **transition**;
- Else if $A$ is an **output port** :
  - If $I$ is an input port and $I \subset Support_A$,
    then we tag $ASG_A$ as **Mealy generation**;
  - Else we tag $ASG_A$ as **Moore generation**;
- Else $A$ is a **temporary variable**;
  so $A$ has the same tag as its children.