Optimizing Resistances and Capacitances of a Continuous-Time ΣΔ ADC

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***Abstract*— The integration capacitor is an important issue when being faced with the power consumption of a ΣΔ analog-to-digital converter. In this paper, we show how the integration capacitance can be derived from signal to noise ratio specifications. In order to decrease the total power consumption of the ΣΔ modulator, a method that optimizes the value of the integrator stage capacitors in the modulator loop filter is proposed.**

I. Introduction

The analog-to-digital ΣΔ converters are commonly used for their good tradeoff between accuracy and power consumption [1]. Continuous-time (CT) modulators have some advantages compared to discrete-time (DT) ones such as the ability to operate with lower power supply, lower sampling rate requirements, lower power consumption, with intrinsic anti-aliasing filtering capability [2]. In another hand the CT ΣΔ modulators are more sensitive to clock jitter than the DT modulators. Moreover, the explicit filtering signal transfer function of a CT modulator can be used to significantly attenuate the interferers that receivers for wireless communications have to deal with [3], [4], [5]. This paper presents a 4-bit continuous-time ΣΔ modulator with 2MHz band-width and 13 to 14 bit SNR which achieves the specification of the UMTS standard [6]. The modulator is based on a feedback architecture. The topology consists of a fifth-order loop filter, a four-bit ADC, a DAC with DWA compensation and an additional feedback coefficient to compensate the loop delay [7].

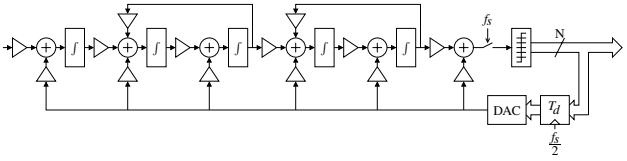

Fig. 1. Converter architecture with multiple feedback, 5^{th} order filter, multibit quantizer and loop delay compensation

The loop filter is based on an integrator cascade and two resonators as depicted in fig.1. In practice, the integration time constant is implemented by passive elements through active RC or Gm-C topologies, resulting in the *RC* product or the C/Gm ratio [8], [9]. In addition, mass-production of consumer electronics requires designs which minimize the manufacturing cost and power-consumption. The circuit cost is related to its surface and possible additional steps of the manufacturing process. Hence, using standard digital CMOS process as the targeted technology is compulsory. The capacitor have a significant influence on the circuit cost. The larger the capacitances, the larger the required area with possible use of extra layers in the manufacturing process. Furthermore, the larger the capacitive load is, the larger current has to be to drive the active parts of the integrators. In this paper we will show how to compute the capacitance from requirements on overall Signal to Noise Ratio of the modulator. We will study the influence of the negative feedback on the thermal noise of the converter. A method to optimize the overall value of the capacitors will be proposed.

II. Noise in the ΣΔ modulator

Figure 2 shows the linearized diagram of the ΣΔ modulator, where the $\overline{U_i}$ stands for the equivalent noise at the input of an integrator stage. Coefficients of a DT architecture are

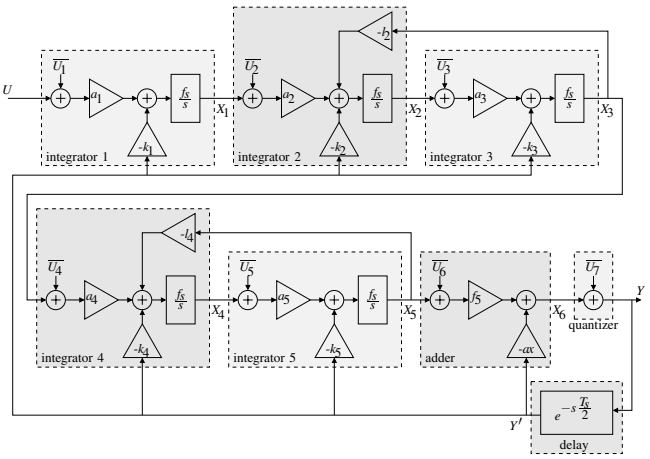

Fig. 2. linearized multiple feedback ΣΔ modulator

obtained from the MATLAB "Delta-Sigma Toolbox" [10]. These coefficients are then converted to obtain coefficients of the CT implementation which has the same Noise (NTF). In order to limit the integrators output below the saturation level, these coefficients are scaled. The new value of the coefficients

a_i, k_i and l_i are calculated with the formula:

$$\tilde{a_i} = \frac{f_{i-1}}{f_i} a_i \quad \tilde{k_i} = \frac{k_i}{f_i} \quad \tilde{l_i} = \frac{f_{i+1}}{f_i} l_i \tag{1}$$

To find out the value of the scaling coefficients f_i the same algorithm presented in [11] is used. We consider an ideal model with a sinusoidal input which has a frequency in the bandwidth and the peak SNR amplitude. The starting value for all the scaling factors is 1. For each stage:

1. simulate the CT ΣΔ modulator with the previously determined scaling factors and the others left to 1.
2. the scaling factor, f_i, corresponding to the i^{th} simulation is calculated using the following expression :

$$f_i = \frac{max(output\ i^{th}\ integrator)}{desired\ i^{th}\ integrator\ output\ swing}$$

The value of the desired output depends on system and circuit levels choices and can be different for each integrator. For stability consideration it is suitable to have a rather small output swing [12].

As the value of the f_i are deferred on the following stage, this method does not modify neither the NTF nor the STF of the modulator.

Equations from the linearized modulator of figure 2 are:

$$\begin{aligned}
Y(s) &= f_5\left(U_6(s)+X5(s)\right)+U_7(s)-axY'(s)\\
Y'(s) &= e^{-s\frac{T_s}{2}}Y(s)\\
sX_5(s) &= f_s\left(a_5\left(U_5(s)+X_4(s)\right)-k_5Y'(s)\right)\\
sX_4(s) &= f_s\left(a_4\left(U_4(s)+X_3(s)\right)-k_4Y'(s)-l_4X_5(s)\right)\\
sX_3(s) &= f_s\left(a_3\left(U_3(s)+X_2(s)\right)-k_3Y'(s)\right)\\
sX_2(s) &= f_s\left(a_2\left(U_2(s)+X_1(s)\right)-k_2Y'(s)-l_2X_3(s)\right)\\
sX_1(s) &= f_s\left(a_1\left(U_1(s)+U(s)\right)-k_1Y'(s)\right)
\end{aligned}$$

From these equations the analytical expression of the transfer functions, from the i input to the modulator output, can be derived. The input-referred in-band noise power of the modulator is calculated as follows:

$$P_{noise} = \sum_{i=1}^{6} \int^{BW} \frac{\overline{U_i}^2 \,\|H_i(f)\|^2}{\|H_1(f)\|^2} df \tag{2}$$

In this equation, the analytical expression of the transfer functions ratios can be derived. Calling $Mi1$ these ratios we obtain the equation of table I for the 5 integrators.

These equations express the shaping of the integrator noise by the modulator. In the case of a Over Sampling Ratio (OSR) equal to 16, these modulus are depicted in figure 3. It appears that the noise of the summing stage (M61) has the same noise-shaping than the quantization noise. The integrator's noise takes advantage of noise-shaping effect. The nearer the integrator is from the quantizer, the stronger is the noise attenuation by the loop. The noise of the first integrator is not shaped by the converter, so it is dominant on the overall noise. However, when the 2^{nd} and 3^{rd} stages noise are brought back in the band-width (fig.3), they also do contribute in a significant way to the overall noise.

$$\begin{aligned}
M11 &= \frac{\|H_1\|}{\|H_1\|} &&= 1\\
M21 &= \frac{\|H_2\|}{\|H_1\|} &&= \frac{2\pi f}{a1 f_s}\\
M31 &= \frac{\|H_3\|}{\|H_1\|} &&= \frac{(2\pi f)^2}{a_1 a_2 {f_s}^2}\\
M41 &= \frac{\|H_4\|}{\|H_1\|} &&= \frac{|-8\pi^3 f^3 {f_s}^2 a_4 a_5 + 2{f_s}^4 l_1 a_3 a_4 a_5 \pi f|}{{f_s}^5 a_1 a_2 a_3 a_4 a_5}\\
M51 &= \frac{\|H_5\|}{\|H_1\|} &&= \frac{\left|16\pi^4 f^4 f_s a_5 - 4\pi^2 f^2 {f_s}^3 a_5 l_1 a_3\right|}{{f_s}^5 a_1 a_2 a_3 a_4 a_5}
\end{aligned}$$

TABLE I

TRANSFER FUNCTIONS RATIOS EXPRESSIONS

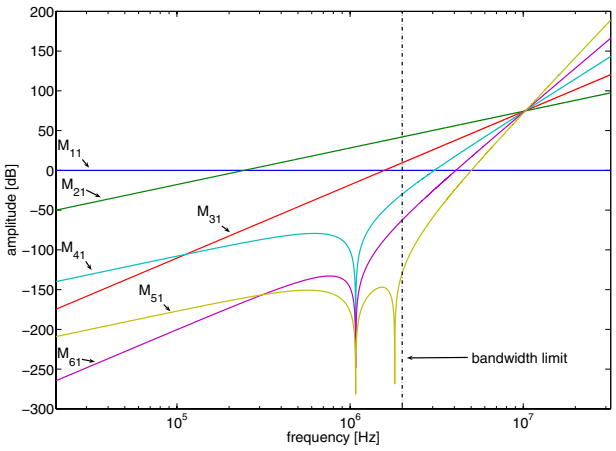

Fig. 3. $OSR = 16$,transfer functions ratios Modulus without scaling

From the $M21$ expression in table I, the Unity Gain Frequency (UGF) corresponding to the 2^{nd} stage noise-shaping depends on a_1 coefficient $f_{0dB} = \frac{a_1 f_s}{2\pi}$. Thus by increasing the value of the a_1 coefficient, one can shift this frequency out-of-band and improve the in-band noise-shaping. We cannot change only the value of a_1 without modifying the STF and NTF. However reconsidering the motivation of the scaling phase to allow a larger first integrator output swing, the f_1 coefficient can be decreased. Therefore the value of a_1 increases without modifying the overall behavior of the modulator. The UGF is thus moved close to the band limit.

However this modification could be insufficient to completely shift the unity gain frequency out of the band-width. This can be done only by increasing the sampling rate of the converter. As the architecture specifications are changed, the coefficients of integration must be completely recomputed, including scaling step. As depicted in fig.4, doubling the OSR and minimizing f_1 during the scaling step, moves the noise of the 2^{nd} and 3^{rd} stages out of the band-width.

III. NOISE OF THE INTEGRATION STAGE

To perform the integration function the differential active RC of figure 5 is used.

From the Kirchoff's current law, the expression of the

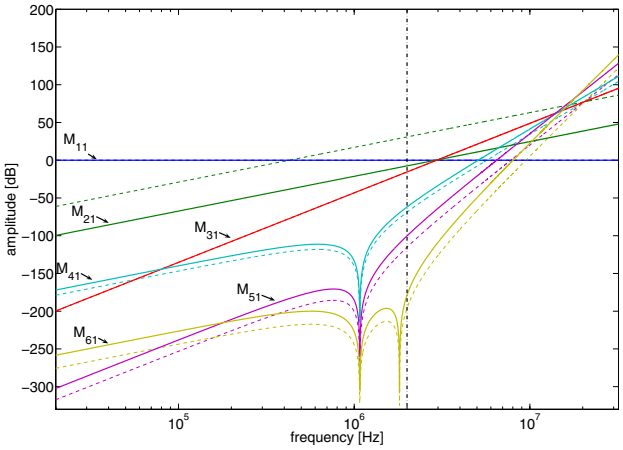

Fig. 4. transfer functions ratio modulus for $OSR = 32$ before (dashed) and after scaling

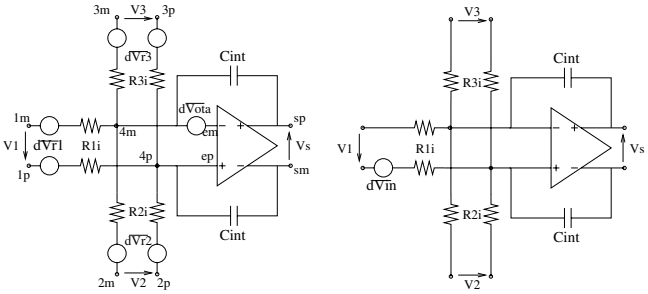

Fig. 5. Active RC Integrator and its equivalent noise source

equivalent noise source on the positive input can be derived:

$$\begin{aligned} d\overline{v_{in}}^2 &= d\overline{v_{r1p}}^2 + d\overline{v_{r1m}}^2 + \frac{G2^2}{G1^2}\left(d\overline{v_{r2p}}^2 + d\overline{v_{r2m}}^2\right) \\ &+ \frac{G3^2}{G1^2}\left(d\overline{v_{r3p}}^2 + d\overline{v_{r3m}}^2\right) \\ &+ \frac{(G1+G2+G3)^2 + (2\pi f C_{int})^2}{G1^2} d\overline{v_{ota}}^2 \end{aligned} \quad (3)$$

The resistive and capacitive elements of the stage are used to implement the integration coefficients according to following relations:

$$\begin{aligned} a_i f_s = \frac{1}{R1 C_{int}} &\iff R1 = \frac{1}{G1} = \frac{1}{2 a_i\ OSR\ BW\ C_{int}} \\ k_i f_s = \frac{1}{R2 C_{int}} &\iff R2 = \frac{1}{G2} = \frac{1}{2 k_i\ OSR\ BW\ C_{int}} \\ l_i f_s = \frac{1}{R3 C_{int}} &\iff R3 = \frac{1}{G3} = \frac{1}{2 l_i\ OSR\ BW\ C_{int}} \end{aligned} \quad (4)$$

As the noise spectral density of a resistance is:

$$d\overline{v_R}^2 = 4 k_B T R \quad (5)$$

by substitution from (4) and (5) into (3) a relation between the input noise spectral density of the integrator, the integration capacitance and the architecture coefficients is obtained :

$$\begin{aligned} d\overline{v_{in}}^2 &= 8 k_B T R1 + \frac{R1^2}{R2^2}(8 k_B T R2) + \frac{R1^2}{R3^2}(8 k_B T R3) \\ &+ \frac{(G1+G2+G3)^2 + (2\pi f C_{int})^2}{G1^2} d\overline{v_{ota}}^2 \\ d\overline{v_{in}}^2 &= \frac{4 k_B T}{a_i\ OSR\ BW\ C_{int}}\left(1 + \frac{k_i}{a_i} + \frac{l_i}{a_i}\right) \\ &+ \left(\frac{(a_i + k_i + l_i)^2}{a_i^2} + \left(\frac{\pi f}{a_i\ OSR\ BW}\right)^2\right) d\overline{v_{ota}}^2 \end{aligned} \quad (6)$$

IV. Noise distribution on integration stages

The overall noise power at the modulator input is known from the targeted Signal to Noise Ratio (SNR) and from the maximum amplitude at the modulator input:

$$Pnoise = \frac{P_{signal}}{SNR} = \frac{amp_{max}^2}{2\ SNR} \quad (7)$$

It corresponds to the sum of each stage noise contribution as calculated in (2). In the case of thermal noise $\overline{U_i}^2 = d\overline{v_{in,i}}^2$ are frequency independent. Thus by integrating the M_{i1} over the bandwidth, the noise contribution is given by:

$$P_{noise,i} = d\overline{v_{in,i}}^2 \int^{BW} M_{i1}^2 df = m_{i1} d\overline{v_{in,i}}^2 \quad (8)$$

A part of the overall noise is allocated to the input of each stage

$$P_{noise,i} = b_i P_{noise}, \sum_{i=1}^{5} b_i = 1 \quad (9)$$

Knowing the acceptable noise power at the input of each stage, the integration capacitance can be determined from (6), (7) and (8):

$$C_{int,i} = \frac{m_{i1}}{b_i} \frac{8 k_B T\ SNR}{a_i\ OSR\ BW\ amp_{max}^2}\left(1 + \frac{k_i}{a_i} + \frac{l_i}{a_i}\right) \quad (10)$$

Therefore the problem is to find the weighting coefficients b_i which minimize the overall capacitance $C_{tot} = \sum_i C_{int,i}$.

To show the influence of the noise distribution on the overall capacitance, consider the 2 following cases:

a) uniform noise distribution on all stages

$$b_i = 1/n$$

b) using modulation coefficient m_{i1} from (8), the overall noise is distributed as:

$$b_i = \frac{m_{i1}}{\sum_i m_{i1}}$$

The integration capacitances are calculated from (10), for the 2 distributions and several targeted resolutions. The overall capacitance is presented in table II.

In the case a), the noise quantity allocated to the first integrator is too low. Since resistances must have a low value to generate low noise, this implies that the capacitance has to be raised to fulfill the desired integration constant. In the other stages, whereas the resistor noise could be strongly attenuated by the modulator loop, the allocated part is too

$ENOB[bit]$	distribution		
	a)	b)	optimum
12.5	7.07	2.95	2.08
13.5	28.3	11.8	8.31
14.5	113	47.1	33.24
15.5	452	188	133

TABLE II

OVERALL CAPACITANCE IN pF FOR VARIOUS TARGETED RESOLUTIONS

high. Resistances could be larger and generate more noise, which would result in a lower integration capacitance.

In the case b), we take advantage of the noise shaping to allocate higher noise to the first stage. Therefore resistors can take larger values and the capacitors decrease. The noise of the other stages is sufficiently attenuated so that resistances are large enough to maintain low capacitance.

However the optimum is not reached. If a small part of the first stage noise is reallocated to the other stages, we observed that the overall capacitance can be decreased. From the solution b), a distribution which leads to a minimal overall capacitance has been worked out. By successively redistributing the noise of a stage on the following ones, we manage to minimize the capacitive load of the circuit.

The results of this procedure, presented in last column of table II, show that the capacitive load in case b) has been decreased by 30%.

V. Simulation results

From (10) and the optimal distribution obtained, the passive element values of active RC integrators were calculated. To validate the method, the modulator was described using VHDL-AMS language and simulated. A macromodel was used for the OTA in combination with a spice level model for resistors and capacitors. Thus the resistive noise is accurately modeled. Linear noise analysis was performed which matches the expected value given by (8).

From the obtained resistances and capacitances the synthesis of the OTA was performed using OCEANE tool [13]. The biasing current is adjusted to keep the $1/f$ noise below the thermal noise.

Using the same simulation environment, the OTA netlist substituting for the macromodel, we could estimate the power consumption of the modulator's loop filter. To achieve 13bit SNR, the analog part would consume about 50mW. The Power Spectral Density is depicted fig.6, for a dual-tone input signal in the bandwidth of half the peak SNR amplitude each. The SIgnal to Noise And Distortion ratio (SINAD) is measured at 96dB. The overall quantization and distortion noise is far below the thermal noise at -80dBFS.

VI. Conclusion

In a $\Sigma\Delta$ modulator, the noise of circuitry can take advantage of the noise-shaping loop of the quantization noise. The architecture coefficients have an influence on each stage noise rejection. In the case of an active RC integrator, we showed the relation between the architecture parameters, the targeted SNR and the integration capacitances. A method was presented to find out the minimal overall integration capacitance. The use of an automatic sizing tool enables to rapidly design the electric components and have an estimation of the architecture performances. This method was used for the design of a 13bit converter, consuming 50mW in the analog loop filter part.

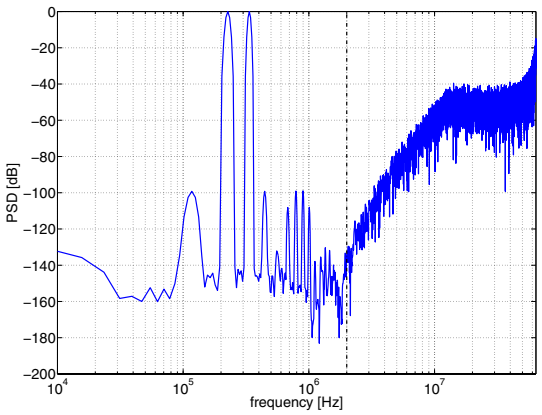

Fig. 6. PSD at the converter output, SINAD=96dB

Acknowledgment

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