A 500-MHz ΣΔ Phase-Interpolation Direct Digital Synthesizer

Thomas Finateu(1), Ivan Miro-Panades(1), Fabrice Boissières(1), Jean-Baptiste Bégueret(2), Yann Deval(2), Didier Belot(1), Franck Badets(1)
(1) STMicroelectronics, 850 rue Jean Monnet, F-38926 Crolles Cedex, France
(2) IMS Laboratory, University of Bordeaux 1, 351 cours de la Libération, F-33405 Talence Cedex, France
thomas.finateu@st.com

***Abstract*-A ΣΔ phase-interpolation direct digital synthesizer (DDS) is presented. This DDS generates frequencies from 400 MHz up to 500 MHz. Phase interpolation uses dual slope integration on a single capacitor and current is provided by a digital to analog converter (DAC). The ΣΔ enables high frequency resolution and shapes quantization noise. The DDS has been integrated on a 65-nm CMOS STMicroelectronics technology. The power consumption is about 29 mW without buffers under 1.2 V for a 500-MHz operating frequency.**

I. INTRODUCTION

Direct digital synthesizer (DDS) brings a lot of interesting features for frequency synthesis. It provides fine frequency resolution suitable for state of the art digital communication systems. Moreover, digital architecture makes DDS highly configurable. On top of that, digital circuitry allows fast settling time and fast frequency hopping performance.

Low power applications such as wireless sensor network are switched off most of the time. Fast settling time is required to maximize power efficiency. Hence, DDS is well suited to be implemented into wireless sensor network.

A conventional DDS [1] consists of a phase accumulator (PA_{CC}), a phase to amplitude ROM, and a digital to analog converter (DAC) as depicted in Fig. 1. The PA_{CC} converts a frequency data P into a phase data φ. Then, a look-up table translates phase data to amplitude data A. DDS spurious level is due to phase to amplitude truncation. Increasing PA_{CC} and ROM bit depths decreases spurious level while on the other hand increases power dissipation and ROM access time.

Solutions have been proposed to compress ROM capacity [1], [2]. Nevertheless, output signal frequency is still limited at a maximum of 1/3 or 1/4 of the clock frequency to keep the filter simple.

Phase-interpolation DDS as [3], [4], [5] suppress ROM as described in Fig. 2. The PA_{CC} delivers phase data φ to a delay generator. The delay generator delays the output of a quantity proportional to the phase error just before PA_{CC} overflow (Ov). By definition, DDS output signal frequency could not exceed one half of the clock frequency. Indeed, at least one clock period is used to determine the phase error, and another is required to interpolate the DDS output phase.

Hence, DDS still has constraints to reach higher frequencies due to non-negligible frequency ratio between clock and output signal frequencies. This is a fundamental drawback when trying to meet RF communication system requirements.

The proposed ΣΔ phase-interpolation DDS allows a high-speed output frequency with low power consumption.

II. ΣΔ PHASE-INTERPOLATION DDS ARCHITECTURE

A. Principle of the Architecture

Fig. 3 details more precisely this new DDS based on a clock phase interpolation. It is composed of a digitally controlled phase interpolator (PI) driven by a PA_{CC}. PI step is equal to $2.\pi/2^{NPA}$ where N_{PA} is the PA_{CC} number of bits. At each clock rising edge, PA_{CC} add a constant value P to its output. Thus, the PI delays clock rising edge of a phase provided by PA_{CC}.

The chronogram of Fig. 4 describes a phase interpolation with N_{PA} equal to 3 and P equal to 1. PA_{CC} accumulates the constant value P every CLK rising edge. Then PI delays CLK rising edge of PA_{CC} output phase φ_{ACC}.

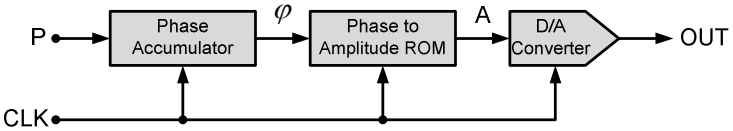

Fig. 1. Block diagram of a conventional DDS.

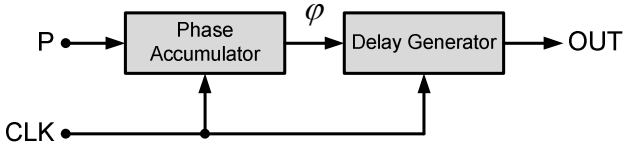

Fig. 2. Block digram of a phase-interpolation DDS.

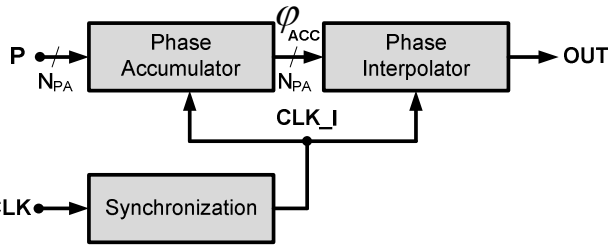

Fig. 3. Block diagram of the proposed phase-interpolaton DDS.

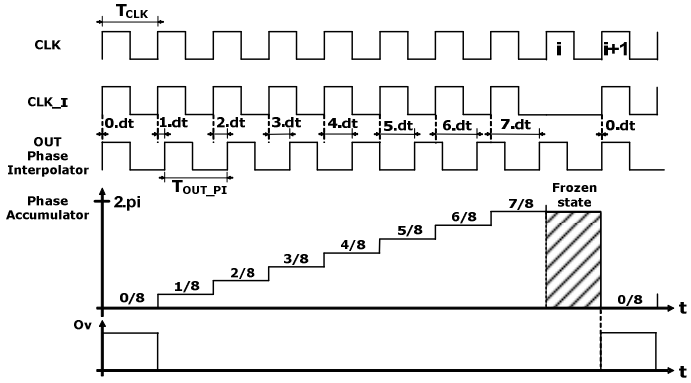

Fig. 4. Chronogram of the proposed phase-interpolation DDS.

When an Overflow (Ov) is generated by PA_{CC}, PI output can be delayed either from CLK(i) of a phase $\varphi_{ACC}+2.\pi$ or from CLK(i+1) of a phase φ_{ACC}. To counteract modulo $2.\pi$ ambiguity, CLK_I is generated from CLK thanks to PA_{CC} output and removes CLK(i) high level.

Thus, the synthesized period can be written as (1).

$$T_{OUT\_PI} = T_{CLK} + dt \tag{1}$$

The time increment dt is given by

$$\frac{dt}{T_{CLK}} = \frac{\varphi_{ACC}}{2 \cdot \pi} = \frac{P}{2^{N_{PA}}} \tag{2}$$

The DDS output frequency is given by (3) and is obtained by combining (1) and (2).

$$f_{OUT\_PI} = \frac{f_{CLK}}{1 + \frac{P}{2^{N_{PA}}}} \tag{3}$$

B. ΣΔ Benefits in Phase-Interpolation DDS

Increasing frequency resolution can be done either by adding PI bits, or by supplying P through a ΣΔ. Using a ΣΔ avoids increasing PI power consumption. Furthermore, ΣΔ rejects quantization noise out of signal band. Noise transfer function depends of ΣΔ sampling frequency. The higher is the sampling frequency, the higher is the out of band rejection, and the easier is an eventual filtering. The ΣΔ phase-interpolation DDS is depicted on Fig. 5. Thanks to the ΣΔ, P can be considered as a fractional in duration, with P_{PA} the integer value, and P_{SD} the fractional value. P_{SD} is a signed value and varies between -2^{NSD} and $+2^{NSD}$. The chosen ΣΔ is a 2-threshold quantizer MASH11 [6] whose output P_{OUT_SD} is between -3 and 3. Thus, (3) becomes (4).

$$f_{OUT\_PI} = \frac{f_{CLK}}{1 + \frac{P_{PA} + \frac{P_{SD}}{2^{N_{SD}-1}}}{2^{N_{PA}}}} \tag{4}$$

The frequency resolution Δf_{OUT_PI} is given by the frequency difference between 2 consecutive P values.

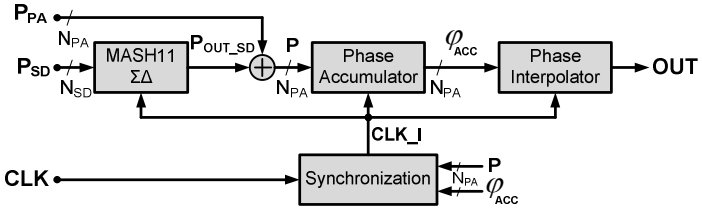

Fig. 5. Block diagram of the ΣΔ phase-interpolation DDS.

III. ΣΔ PHASE-INTERPOLATION DDS DESIGN

Phase interpolation consists of dual-slope integration on a single capacitor (Fig. 6) to avoid capacitor mismatch and minimize silicon area. Interpolating a clock thanks to a current integration requires several steps into a single clock period as shown by the state machine on Fig. 8. Here is the process: first, the capacitor CAP is discharged, then a variable current loads CAP, following by a constant current load. Finally if an overflow occurs, another reset is generated to suppress $2.\pi$ ambiguity. In order to realize all these steps in a single clock period, the state machine has to be driven by a clock frequency four times higher. Interpolation of a 500-MHz clock is done using a 2-GHz state machine clock. The variable slope is given by (5) where K corresponds to PA_{CC} output value during variable state V and varies between 0 and 2^{NPA} - 1.

$$V_{VAR} = \int_0^{T_{CLK}} \frac{I_{VAR}}{C} \cdot dt = \int_0^{T_{CLK}} \frac{K \cdot I_0}{C} \cdot dt = K \cdot \frac{I_0}{C} \cdot T_{CLK} \tag{5}$$

A constant slope is then generated with all DAC current sources switched on, as given by

$$V_{CST} = \int_0^{\Delta T_i} \frac{I_{CST}}{C} \cdot dt = \int_0^{\Delta T_i} \frac{\left(2^{N_{PA}} - 1\right) \cdot I_0}{C} \cdot dt = \left(2^{N_{PA}} - 1\right) \cdot \frac{I_0}{C} \cdot \Delta T_i \tag{6}$$

The capacitor voltage crosses a reference voltage V_{REF} at a time $T_{CLK} + \Delta T_i$, with V_{REF} ideally equal to

$$V_{REF} = \frac{\left(2^{N_{PA}} - 1\right) \cdot I_0}{C} \cdot T_{CLK} \tag{7}$$

Combining (5), (6), and (7) leads to (8).

$$\Delta T_i = \frac{\left(2^{N_{PA}} - 1\right) - K}{2^{N_{PA}} - 1} \cdot T_{CLK} \tag{8}$$

Hence, ΔT_i represents the interpolated time and is limited to a CLK period. As N_{PA} bits cover $2.\pi$ at CLK frequency, N_{PA} represents $\pi/2$ at CLK_I frequency, and finally $N_{PA}+2$ represents $2.\pi$ at CLK_I frequency. Moreover, A self-adjusting PI is guaranteed if V_{REF} is always greater than (8) for all process, voltage, and temperature deviation. A voltage V_{REF} greater than $V_{VAR}+V_{CST}$ introduces only a constant phase at PI output.

Fig 9 illustrastes the phase interpolation with N_{PA} equal to 3 and P equal to 3. The signal R drives DAC current sources made up by PMOS transistors (Fig. 6). When R equals 6 (decimal value of the bit vector), the 2 most significant switches are connected to ground and the least significant switch is connected to the

capacitor. The variable state V "without correction" is an image of a conventional PA_{CC} output. However, after PA_{CC} overflow (Reset2 state), interpolated phase is not correct because a shorten period T_{ERROR} is synthesized instead of T_{OUT_PI}. The solution is to modify PA_{CC} design as shown in Fig. 7. During Reset2 state, the signal SEL_ADD is set to '1', adding one to P value. Interpolated phase is corrected and the DDS generates T_{OUT_PI} period.

Finally, DDS output frequency is given by

$$f_{OUT\_PI} = \frac{f_{CLK}}{P_{PA} + \frac{P_{SD}}{2^{N_{SD}-1}}} \qquad (9)$$
$$1 + \frac{}{(2^{N_{PA}} - 1)\cdot 4}$$

IV. Experimental Results

The layout is depicted in Fig. 10. The chip was packaged in a TQFP32 and measured on board. A JTAG has been implemented mainly to limit number of pads and to configure PA_{CC} and ΣΔ input bits. Besides, the 2-GHz state machine, the 500-MHz 8-bit PA_{CC}, the 500-MHz 14-bit ΣΔ, and the JTAG have been placed and routed using standard cells. All other blocks are full custom. The overall active area is 0.1 mm^2. This DDS operates with a maximum clock frequency of about 2.8 GHz.

A 2-GHz clock is provided at DDS input by a Rohde & Schwarz SMT06. Thus, Fig. 11 depicts the clock phase noise and the DDS output phase noise. The measured DDS frequency is 467.389655-MHz with P_{PA}=71 and P_{SD}=1365. The DDS frequency is well predicted by (9). DDS floor noise is mainly due to the comparator. The ΣΔ noise shaping is visible from 10 MHz up to 40 MHz.

Fig. 12 depicts the DDS output spectrum at a frequency about 496 MHz. Spurious are due to DAC mismatch and redundancy to describe the trigonometric circle. Stronger is the DAC mismatch, higher is spurious level. However, spurious level remains under -65 dBc, excluding the harmonics.

A frequency resolution better than 60 Hz is achieved as shown on Fig. 13.

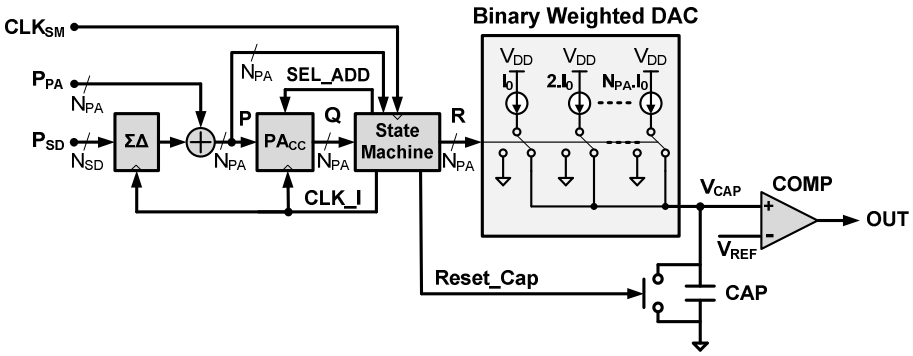

Fig. 6. Detailled block diagram of the ΣΔ phase-interpolation DDS.

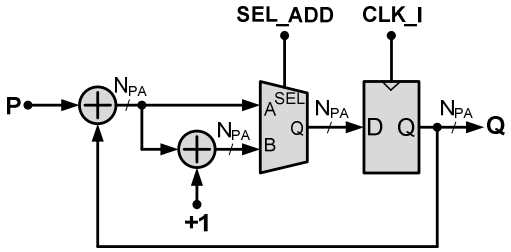

Fig. 7. Block diagram of the custom phase accumulator (PA_{CC}).

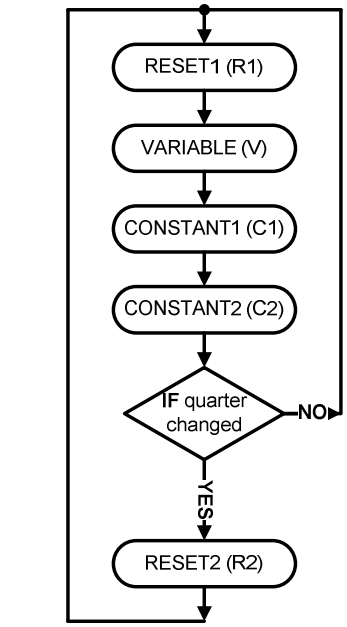

Fig. 8. Block diagram of the state machine.

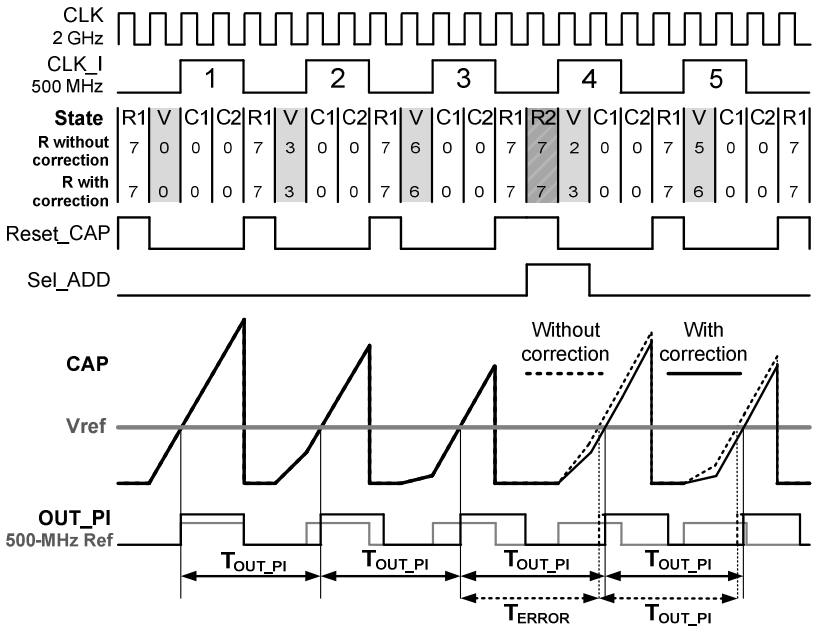

Fig. 9. Chronogram of the designed phase-interpolation DDS.

V. Conclusion

A ΣΔ phase-interpolation direct digital synthesizer has been presented. The phase interpolation allows spurious reduction whereas ΣΔ enables high frequency resolution. The DDS generates frequencies from 400 MHz up to 500 MHz with a 60-Hz resolution. This DDS still presents some spurious. However, the use of thermometric DAC and dynamic element matching could considerably reduce spurious level.

The ΣΔ phase-interpolation DDS occupies 0.1-mm^2 active area on a 65-nm CMOS STMicroelectronics technology. The power dissipation is about 29 mW under 1.2-V battery.

Acknowledgment

Authors thank Stéphane Le Tual and Stéphane Villiers from STMicroelectronics for providing DAC design and layout.

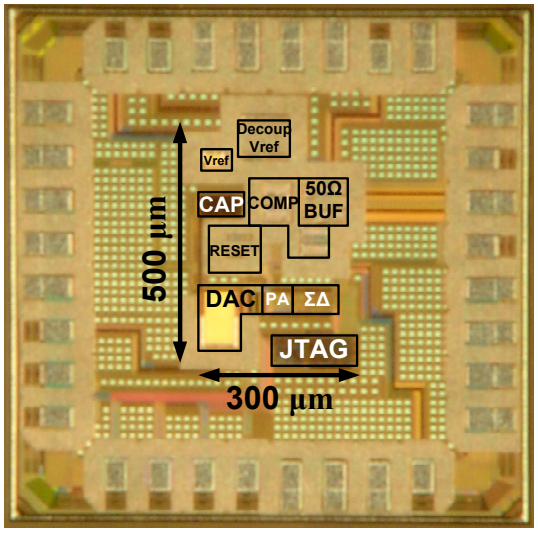

Fig. 10. Chip micrograph of the ΣΔ phase-interpolation DDS.

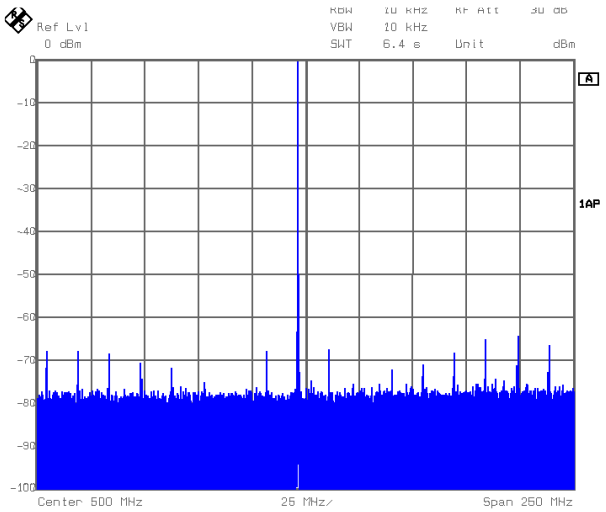

Fig. 12. DDS output spectrum for P_{PA}=8 and P_{SD}=-31.

References

[1] J. Vankka, *Digital Synthesizers and Transmitters for Software Radio.* Springer, 2005, chapter 4: Direct Digital Synthesizers.

[2] H. T. Nicholas, H. Samueli, "A 150-MHz Direct Digital Frequency Synthesizer in 1.25-µm CMOS with -90-dBc Spurious Performance," International Journal of Solid-State Circuits, vol. 26, Dec. 1991, pp. 1959-1969.

[3] F. Badets, D. Belot, "A 100 MHz DDS with synchronous oscillator-based phase interpolator," International Solid-State Circuits Conference (ISSCC), Feb. 2003, pp. 410- 503.

[4] H. Nosaka, Y. Yamaguchi, A. Yamagishi, H. Fukuyama, M. Muraguchi, "A Low-Power Direct Digital Synthesizer Using a Self-Adjusting Phase-Interpolation Technique," International Journal of Solid-State Circuits, Vol. 36, Aug. 2001, pp. 1281- 1285.

[5] H. C. Chen, J. S. Chiang, "A Low-Jitter Phase-Interpolation DDS Using Dual-Slope Integration," IEICE Electronics Express, Vol. 1, Sep. 2004, No. 12, pp. 333-338.

[6] S. R. Norsworthy, *Delta-Sigma Data Converters: Theory, Design, and Simulation*, Wiley, 1996. Chapter 6: The design of cascaded ΔΣ ADCs.

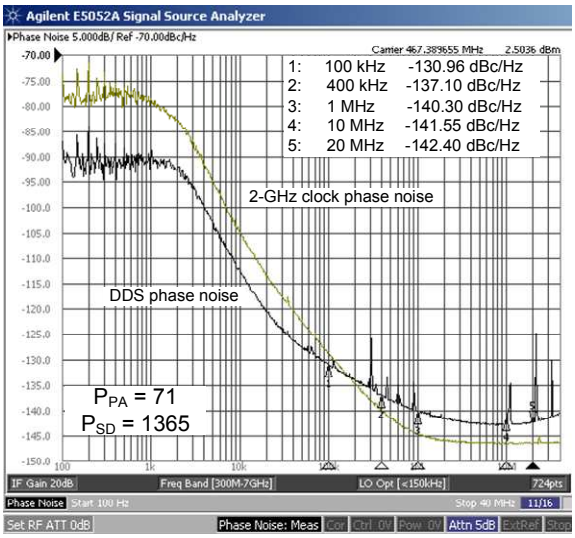

Fig. 11. Clock and DDS output phase noise for P_{PA}=71 and P_{SD}=1365.

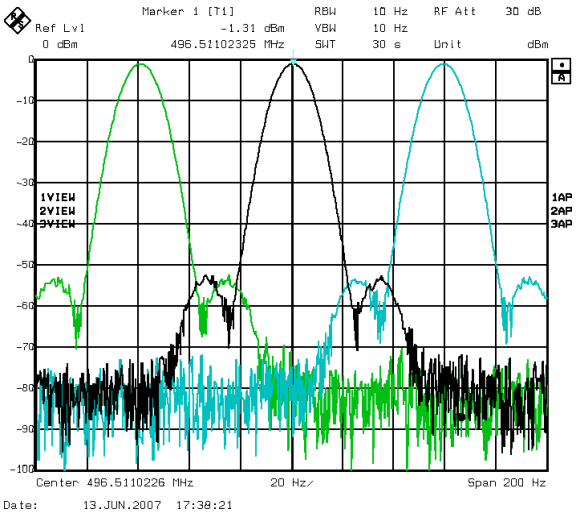

Fig. 13. DDS frequency resolution for P_{PA}=7 and P_{SD}=1366,1365 and 1364.