Automatic Model Refinement of GmC Integrators for High-Level Simulation of Continuous-Time Sigma-Delta Modulators

Michel Vasilevski, Hassan Aboushady, Marie-Minerve Louerat
Laboratoire LIP6/SOC, University of Paris VI, Pierre et Marie Curie, France

***Abstract*—A ΣΔ GmC integrator refinement flow is presented. The classically simplified GmC integrator small-signal model was upgraded to be extremely accurate by considering the complete transistor small-signal model. A circuit-level knowledge-based tool was used to execute the designer defined sizing procedure and to extract small signal parameters. By associating the symbolic transfer function to small-signal parameters, the flow, entirely implemented with C++, is able to compute poles and zeros to permit precise behavioral simulations. A 2^{nd} order ΣΔ modulator was chosen to visualize performance degradations while the specifications were not achievable.**

I. Introduction

The essential target of simulation is evaluation of performances. When measuring non-linear devices such as ΣΔ modulators, a time-domain analysis is required. Performances are extracted through spectral analysis, requiring a sufficient number of simulation samples to be accurate enough. Running those simulations at transistor-level is time consuming. Designers have to deal with levels of abstraction to handle the trade-off between simulation speed and accuracy of results. That's why a great challenge is to refine behavioral models with a large amount of non-idealities.

ΣΔ modulators are well known for their performances. They are used in high resolution audio and wireless applications. Continuous-time modulators consume low power and operates at high sampling rate. Many publications have presented non-idealities modeling either in the discrete-time case [1] [2] [3] [4] or the continuous-time one [5] [6] [7]. They model poles/zeros limitations, clock jitter, noise, saturation, harmonic distortion, other non-linearities. Characterization of these non-idealities is still often based on circuit-level simulation. Expressing non-idealities as function of circuit small signal parameters is always valuable since it permits automatic model refinement and architecture exploration [8].

Focusing on poles/zeros characterization, symbolic analysis [2] [9] has proved its worth to refine behavioral transfer function. This way, technology independent functions can describe a circuit. By choosing a technology, small-signal parameters of the circuit allow to finally determine the values of poles and zeros. Such extraction is generally simulation-based [9]. There are many variants, for example, [7] introduced curve fitting also based on simulation.

In this paper, we investigated continuous-time ΣΔ GmC integrators. First, we present a precise small-signal model of a GmC integrator. Then, a circuit-level knowledge-based approach [10] is introduced for transistor-sizing and small-signal parameters extraction. Finally, we speak about the entirely automated GmC transfer function refinement flow that was built.

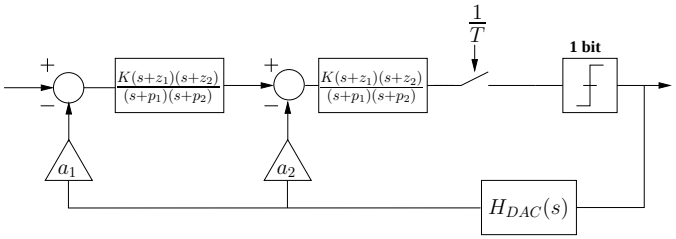

Fig. 1. 2^{nd} order Sigma-Delta modulator.

II. GmC small signal model

When designing an integrator for a ΣΔ modulator, the transfer function has to satisfy:

$$H(s) = \frac{A_{int} f_s}{s} \tag{1}$$

A_{int} is integrator desired gain and f_s is ΣΔ sampling frequency. To check the correctness of the design, the transition frequency (f_T) is computed:

$$\frac{A_{int} f_s}{s} = 1 \quad \Rightarrow \quad f_T = \frac{A_{int} f_s}{2\pi} \tag{2}$$

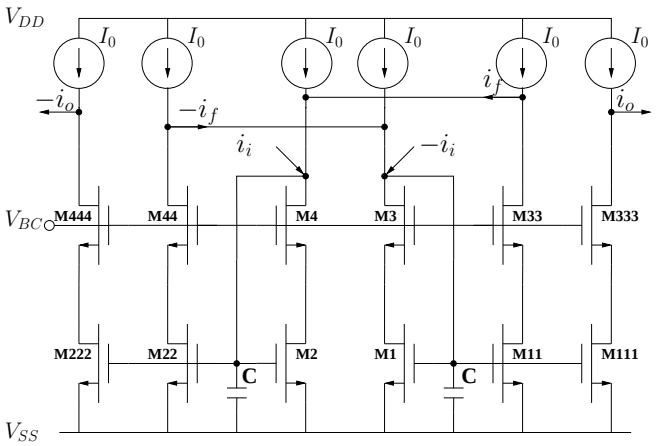

Fig. 2. Differential current-mode integrator.

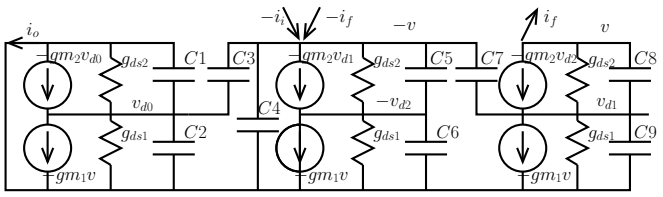

Fig. 3. Small-signal GMC integrator model.

Ignoring parasitic capacitances and output conductances, the transfer function of a GmC integrator, presented in fig.2, is:

$$H(s) = \frac{g_m}{sC} \quad (3)$$

Many publications [11] [12] [13] presented a small-signal model built from a simplified GMC integrator. This model has such transfer function:

$$H(s) = A_0 \frac{(1 - \frac{s}{z_1})}{(1 + \frac{s}{p_1})} \quad (4)$$

With,

$$z_1 = \frac{(g_m - g_{ds})}{2C_{gd}} \text{ , } p_1 = \frac{2g_{ds}}{(C + 4C_{gd})} \text{ and } A_0 = \frac{g_m - g_{ds}}{2g_{ds}}$$

This model reveals one pole and one zero, whereas a SPICE level AC analysis reveals two poles and two zeros. The difference comes from simplifications that were made: the model is non-cascoded and supposes that output current i_o is identical to feedback current i_f thanks to current mirror operation.

We chose to upgrade the model (equation (4) by taking into account cascoding and including every parasitic capacitances of the complete small-signal transistor-model in order to avoid errors when another technology is selected. This new small-signal model is presented in figure 3. From left to right, we represented small-signal equivalent model of (M111,M333), then (M1,M3) finally (M11,M33) couple of transistors. Note that every output conductances, transconductances and parasitic capacitances of the same line are equal. They are respectively called g_{ds1},g_{m1},C_{xx1} for the bottom line of transistors (M1,M11,M111) and g_{ds2},g_{m2},C_{xx2} for the upper line (M3,M33,M333). Moreover we merged parallel capacitances in the figure 3 to be more readable:

$$\begin{aligned}
C1 &= C_{ds2} \\
C2 &= C_{sb2} + C_{ds1} + C_{db1} + C_{sg2} \\
C3 &= C_{dg1} \\
C4 &= C + 3C_{gs1} + 3C_{gb1} + 2C_{db2} + 2C_{dg2} \\
C5 &= C_{ds2} + C_{dg1} \\
C6 &= C_{sb2} + C_{ds1} + C_{db1} + C_{sg2} \\
C7 &= C_{dg1} \\
C8 &= C_{ds2} \\
C9 &= C_{sb2} + C_{ds1} + C_{db1} + C_{sg2}
\end{aligned}$$

CAIRO+ [10] is a tool that was developed in LIP6 laboratory. It is a C++ based language that allows to describe a transistor-level hierarchical netlist and to implement the sizing procedure of the designed circuit. Thereby, the designer implements how to size each transistors using system level specifications. It includes the inverted BSIM3v3 equations to make accurate transistor-sizing, producing a sized netlist As CAIRO+ is based on the DC operating point computation, the small-signal parameters of each transistors are available. This tool was used to get automatically small signal parameters of the GmC integrator circuit without running transistor level simulations. Thanks to automatic small signal parameters extraction, a precise transfer function was computed depending on the technology and system level specifications.

III. Automatic characterization flow

The system level description is implemented with a C++ based behavioral modeling language named SystemC-AMS 0.15 RC5 [14] using the Synchronous Data Flow (SDF) model of computation (MOC). It can be compared to Matlab level of abstraction. The target was to make an easy link with CAIRO+, since such two languages are C++ based. Maple, a symbolic tool, computed the transfer function of the GMC integrator. We let every small-signal parameters as unknown variables. So the result can be implemented to be used in a characterization

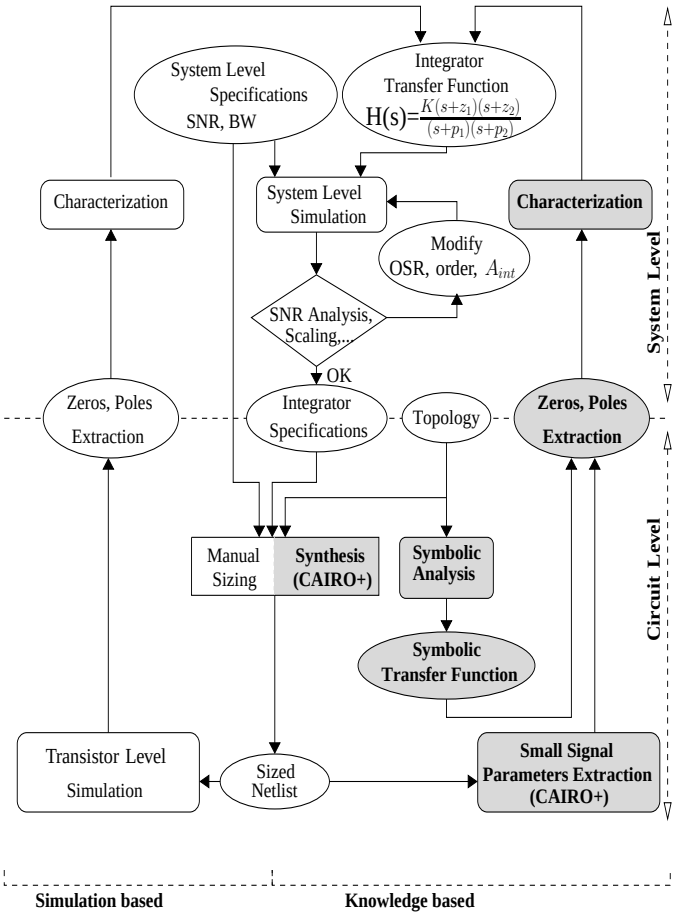

Fig. 4. Integrator characterization flow.

flow depending on system-level parameters, that is presented in figure 4.

Let us describe the figure from upper to bottom side.
First, a system-level tuning is illustrated, using SNR analysis or scaling process thanks to a system-level time-domain simulation implemented with SystemC-AMS. At this point, the $\Sigma\Delta$ integrators transfer function is reduced to : $\frac{A_{int}f_s}{s}$. This phase permits to determine the optimized integrator gain A_{int}, the $\Sigma\Delta$ optimal input amplitude ($A_{\Sigma\Delta}$). The system-level specification (BW) and and resulting system-level parameters required for transistor sizing of the integrator, called "integrator specifications" (such as OSR, $A_{\Sigma\Delta}$: optimal input amplitude, A_{int} : integrator gain, resolution) are passed to the transistor sizing stage.
Then, two possible ways for characterizing the flow are displayed : simulation or knowledge-based (dark boxes). The target is to extract zeros and poles to refine the integrator transfer function. One way performs zeros/poles analysis by a transistor-level simulation. The second way computes the symbolic transfer function thanks to a tool like Maple or Maxima. Then small-signal values are provided by CAIRO+. They are finally injected in the symbolic transfer function to compute the values of poles and zeros. It is important to understand that for the moment, the automatic characterization is depending of the integrator topology, here is presented the GmC integrator topology. In fact, the small-signal topology analysis computed by a symbolic analyzer has to be introduced by the designer for each integrator topology. Finally, the characterized integrator transfer function refines the behavioral model of the $\Sigma\Delta$ integrators and a more precise simulation can be performed.

IV. Results

In this section, we illustrate how the presented characterization method can be used to study the feasibility of specifications, for a 2^{nd} order CT $\Sigma\Delta$ modulator based on the differential current-mode GmC integrator of Fig. 2. Table I describes the 2^{nd} order $\Sigma\Delta$ specifications. A_{int} is the integrator gain that was scaled to 1/3 when using a Return-to-Zero DAC. $A_{\Sigma\Delta}$ is the input signal amplitude at which maximum SNR is achieved. Those specifications were set into system level models of the $\Sigma\Delta$ modulator.

TABLE I
SPECIFICATIONS OF THE 2^{nd} ORDER $\Sigma\Delta$ MODULATOR.

SNR	$> 60dB$
OSR	64
A_{int}	0.33
$A_{\Sigma\Delta}$	0.56

TABLE II
INTEGRATORS CIRCUIT CHARACTERISTICS, COMPARING TWO DIFFERENT INITIAL TRANSISTOR LENGTH ($0.13\mu m$ CMOS PROCESS) WITH VDD=1.2V.

BW	200 kHz	200 kHz
W1/L1	4.6/10	1.2/3
W3/L3	37/9	0.47/0.18
I_0	7.6 μA	5.6 μA
Desired f_T	1.36 MHz	1.36 MHz
Measured f_T	1.29 MHz	1.35 MHz
C	3.6 pF	3.8pF
Measured SNR	47.4 dB	68.4 dB

Figure 5 presents frequency response of the GmC integrator based on different models : ideal, SPICE (transistor level), complete characterized Zeros/Poles and simplified characterized Zeros/Poles. The GmC integrator was designed for a 200kHz bandwidth in a 0.13μm process, using a 1.2V supply voltage. First, we can confirm the exact matching of the complete characterized model compared to the SPICE model. This figure also reveals how a simplified model would have approved the sizing procedure since it did not detect the presence of a second pole near fT. Precise modeling is useful in guiding the designer to reduce the transistor lenghts (L) in order to push the second pole to higher frequencies.

Figure 6 presents the frequency response of a GmC integrator designed for 200kHz in a 0.13μm process, after reducing the transistor lengths. Table II contains SNR simulation results based on a time-domain SystemC-AMS simulation using complete characterized Zeros/Poles integrator models. These results show the improvement in the $\Sigma\Delta$ SNR after reducing the transistor lengths.

Table III presents some simulation results after the design

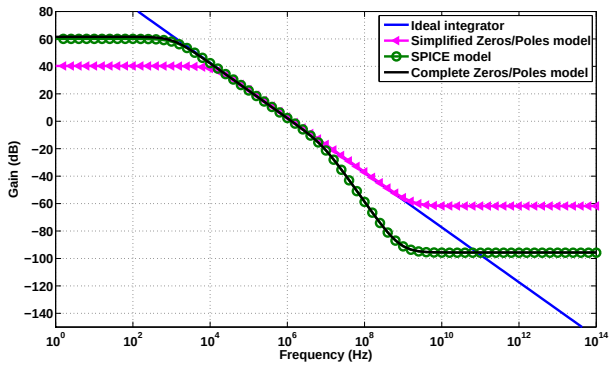

Fig. 5. Frequency response of a $\Sigma\Delta$ GmC integrator automatically designed for BW=200kHz, comparing small-signal , SPICE to ideal model, revealing a 2^{nd} pole because of transitor high length (0.13μm process).

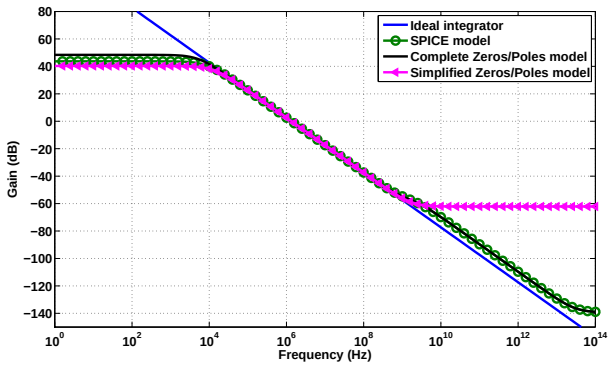

Fig. 6. Frequency response of a $\Sigma\Delta$ GmC integrator automatically designed for BW=200kHz, comparing small-signal, SPICE to ideal model, after transistor length minimization (0.13μm process).

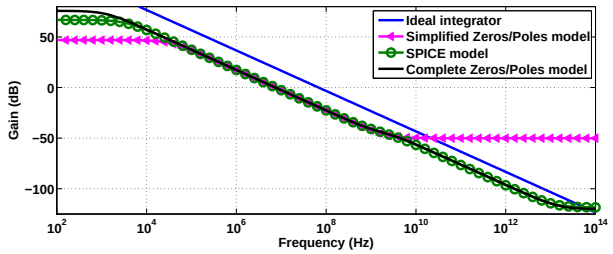

Fig. 7. Frequency response of a ΣΔ GmC integrator automatically designed for BW=10MHz, comparing small-signal, SPICE to ideal model, illustrating a case of technological limitation (0.25μm process).

and characterization of the GmC integrator for different ΣΔ bandwidths (BW) comparing 0.13μm (1.2V) and 0.25μm (1.8V) technologies. We specified minimal transistor lenghts to avoid a second pole effect. We picked up fT result after an AC simulation and compared it to the desired fT computed using equation (2). We can see how the sized GmC integrator circuit can limit the overall ΣΔ performances. In fact, for a 200 kHz bandwidth, the SNR is sufficient for the targeted specifications. For a 10MHz bandwidth, the capacitance sizing procedure returns 0pF because fT cannot be reached, the first pole is resulting from input parasitic capacitances. AC simulations illustrate that effect in Fig. 7 for the 0.25μm process. In Figure 8, we plotted the 2^{nd} order ΣΔ modulator output spectrum for different bandwidths : 200kHz, 10MHz, with 0.13μm and 0.25μm technologies. Each spectrum correspond to a case listed in Table II and Table III. We can see the deterioration of the spectrum when increasing the bandwidth and also when the transistor length is too high.

V. Conclusion

An upgraded GmC integrator small-signal model was described. It is used to compute a symbolic transfer-function that is combined with small-signal parameters to produce poles and zeros of the circuit. Small-signal parameters were automatically extracted by a circuit-level knowledge-based synthesis tool that performs transistor-level sizing and characterization. The results presented the accuracy of the model that was computed regarding to a SPICE AC simulation result.

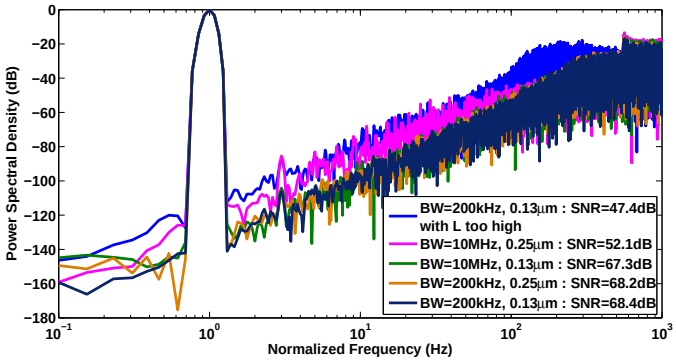

Fig. 8. 2^{nd} order ΣΔ modulator output spectrum for different bandwidths in 0.13μm and 0.25μm technologies with constant OSR=64.

TABLE III
Integrators circuit characteristics comparing 0.25μm (Vdd=1.8V) to 0.13μm CMOS process (Vdd=1.2V), L minimized.

Technology	0.13μm	0.25μm	0.13μm	0.25μm
BW	200kHz	200kHz	10MHz	10Mhz
W1/L1	1.2/3	1.8/10	56/3	67/10
W3/L3	0.47/0.18	0.56/1.2	12/0.13	3.8/0.25
I_0	5.6μA	1.5μA	280μA	73μA
Desired f_T	1.36MHz	1.36MHz	67.9MHz	67.9MHz
Measured f_T	1.35MHz	1.36MHz	55.3MHz	7.42MHz
C	3.8pF	0.87pF	0pF	0pF
Measured SNR (dB)	68.4dB	68.2dB	67.3dB	52.1dB

They showed how the refinement flow permits to perform specification feasibility analysis.

References

[1] P. Malcovati, S. Brigati, F. Francesconi, F. Maloberti, P. Cusinato, and A. Baschirotto, "Behavioral Modeling Of Switched-Capacitor Sigma-Delta Modulators," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, vol. 50, pp. 352–364, 2003.

[2] D. Aksin and F. Maloberti, "Symbolic Small-Signal Analysis (SSA) Tool," in *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, 2005, pp. 3007–3010 Vol. 3.

[3] A. Fornasari, P. Malcovati, and F. Maloberti, "Improved Modeling Of Sigma-Delta Modulator Non-Idealities In Simulink," in *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, 2005, pp. 5982–5985 Vol. 6.

[4] C.-I. Lao, S.-P. U, and R. Martins, "Bandpass Sigma-Delta Modulator SIMULINK Non-Idealities Model With Behavior Simulation," in *ASIC, 2003. Proceedings. 5th International Conference on*, vol. 1, 2003, pp. 685–688 Vol.1.

[5] G. Gielen, K. Francken, E. Martens, and M. Vogels, "An Analytical Integration Method For The Simulation Of Continuous-Time ΣΔ Modulators," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 23, pp. 389–399, 2004.

[6] J. Ruiz-Amaya, J. de la Rosa, F. Medeiro, F. Fernandez, R. del Rio, B. Perez-Verdu, and A. Rodriguez-Vazquez, "MATLAB/SIMULINK-Based High-Level Synthesis Of Discrete-Time And Continuous-Time ΣΔ Modulators," in *Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings*, vol. 3, 2004, pp. 150–155 Vol.3.

[7] M. El-Nozahi and Y. Massoud, "An Integrated Circuit/Behavioral Simulation Framework For Continuous-time Sigma-Delta ADCs." Philadelphia, PA, USA: ACM, 2006, pp. 353–356.

[8] E. Martens and G. Gielen, "Analyzing Continuous-Time ΣΔ Modulators With Generic Behavioral Models," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 25, pp. 924–932, 2006.

[9] H. Zhang and A. Doboli, "Fast Time-Domain Symbolic Simulation For Synthesis Of Sigma-Delta Analog-Digital Converters," in *Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on*, vol. 5, 2004, pp. V–125–V–128 Vol.5.

[10] H. Aboushady, L. de Lamarre, N. Beilleau, and M. Louerat, "Automatic synthesis and simulation of continuous-time $\sigma\delta$ modulators," in *Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings*, vol. 1, 2004, pp. 674–675 Vol.1.

[11] H. Aboushady and M.-M. Louerat, "Low-Power Design Of Low-Voltage Current-Mode Integrators For Continuous-Time Sigma-Delta Modulators," in *Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on*, vol. 1, 2001, pp. 276–279 vol. 1.

[12] S. Smith and E. Sanchez-Sinencio, "Low Voltage Integrators For High-Frequency CMOS Filters Using Current Mode Techniques," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 43, pp. 39–48, 1996.

[13] R. Zele and D. Allstot, "Low-Power CMOS Continuous-Time Filters," *Solid-State Circuits, IEEE Journal of*, vol. 31, pp. 157–168, 1996.

[14] A. Vachoux, C. Grimm, and K. Einwich, "Extending SystemC to Support Mixed Discrete-Continuous System Modeling and Simulation," *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, 2005.