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-- Additionneur 4 bits avec report entrant et sortant

ENTITY adder IS
  PORT (
    i0      : IN  BIT_VECTOR(3 DOWNTO 0);
    i1      : IN  BIT_VECTOR(3 DOWNTO 0);
    q       : OUT BIT_VECTOR(3 DOWNTO 0);
    cin     : IN  BIT;
    cout    : OUT BIT;
    vdd     : IN  BIT;
    vss     : IN  BIT
  );
END adder;

ARCHITECTURE vbe OF adder IS

  SIGNAL carry : BIT_VECTOR(4 DOWNTO 0) ;

BEGIN

  carry(0) <= cin;
  carry(4 DOWNTO 1) <= ( ( i1(3 DOWNTO 0)      AND i0(3 DOWNTO 0) )      OR
                        ( i0(3 DOWNTO 0)      AND carry(3 DOWNTO 0) ) OR
                        ( carry(3 DOWNTO 0) AND i1(3 DOWNTO 0) )      ) ;
  q        <= i0 XOR i1 XOR carry(3 DOWNTO 0) ;
  cout     <= carry(2);

END;

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