Outline

- Introduction
- Architecture of a RISC Processor
- Implementation

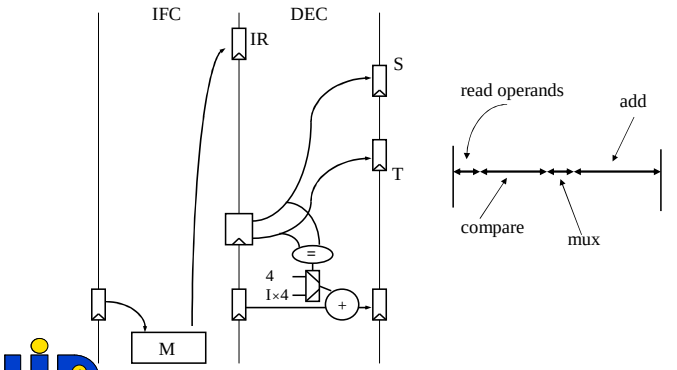
Implementation

Implementation of DEC cycle

- Next instruction address calculation

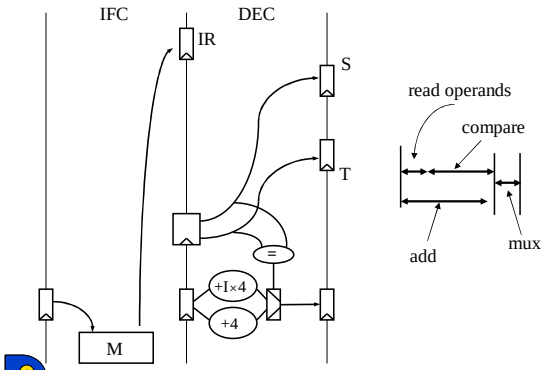
Implementation

Example : Beq rs, rt, label



Implementation

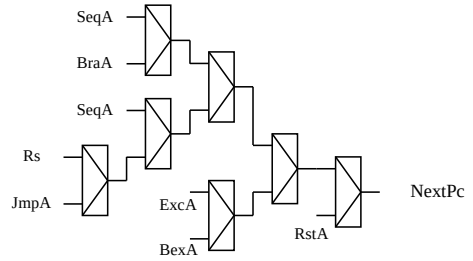
Example : Beq rs, rt, label



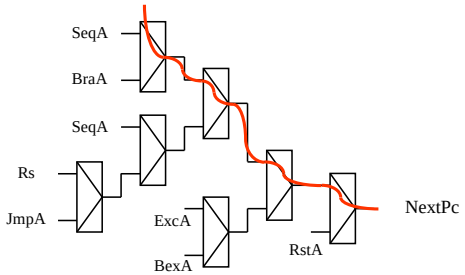
Next instruction address

- Sequential address (SeqA)
- Branch target address (BraA)
- Jump address (JmpA)
- Source register (Rs)
- **0xBFC0 0000** (RstA)
- **0xBFC0 0180**(BexA)
- **0x8000 0080** (ExcA)

Next instruction address



Next instruction address



Next instruction address

- Sequential address (SeqA)

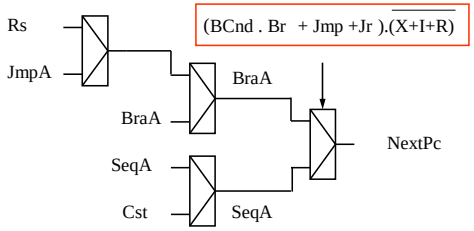
Branch failure

Sequential instruction

- Branch target address (BraA)

	Beq	Bne	Bltz	Bgez	Blez	Bgtz
Condition	Rs = Rt	Rs ≠ Rt	Rs < 0	Rs ≥ 0	Rs ≤ 0	Rs > 0
True	BraA	BraA	BraA	BraA	BraA	BraA
False	SeqA	SeqA	SeqA	SeqA	SeqA	SeqA

Next instruction address



Next instruction address

- Sequential address (SeqA)
- Branch target address (BraA)

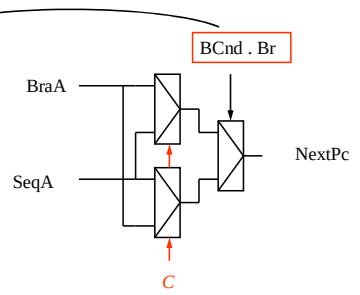
Branch failure

Sequential instruction

	Beq	Bne	Bltz	Bgez	Blez	Bgtz
Condition	Rs = Rt	Rs = Rt	Rs < 0	Rs < 0	Rs ≤ 0	Rs ≤ 0
True	BraA	SeqA	BraA	SeqA	BraA	SeqA
False	SeqA	BraA	SeqA	BraA	SeqA	BraA

Next instruction address

Rs = Rt si Beq, Bne
Rs < 0 si Bltz, Bgez
Rs ≤0 si Blez, Bgtz



C = 1 si Beq, Bltz, Blez
C = 0 si Bne, Bgez, Bgtz

Next instruction address

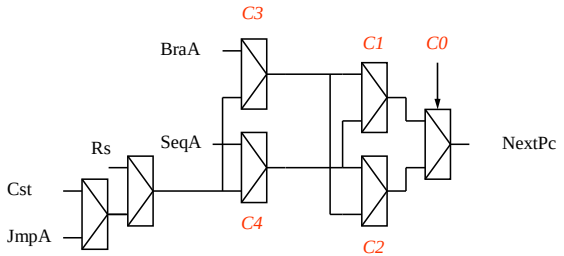
- Sequential address (SeqA)
- Branch target address (BraA)

Branch failure

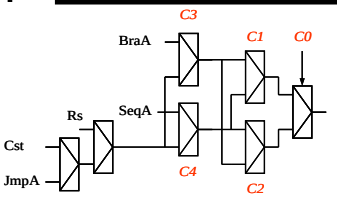
Sequential instruction

	Beq	Bne	Bltz	Bgez	Blez	Bgtz	
Condition	Rs = Rt	Rs = Rt	Rs < 0	Rs < 0	Rs ≤ 0	Rs ≤ 0	Rs = 0 Rs < 0
True	BraA	SeqA	BraA	SeqA	BraA	SeqA	
False	SeqA	BraA	SeqA	BraA	SeqA	BraA	

Next instruction address



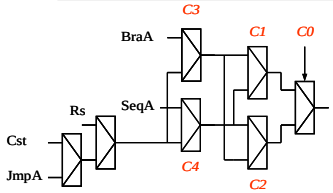
Next instruction address



	C0		C1	C2		C3	C4
Beq T	1		1	1		1	1
Beq F	0		1	1		1	1
Bne T	0		0	0		1	1
Bne F	1		0	0		1	1
Bltz T	-		1	0		1	1
Bltz F	-		0	1		1	1
Blez T	1	Si Rs=Rt	1	0	Si Rs<0	1	1
Blez F	0		0	1		1	1
Bgtz T	0		0	1		1	1
Bgtz F	1		1	0		1	1
Bgez T	-		0	1		1	1
Bgez F	-		1	0		1	1
Jr	-		-	-		0	0
J	-		-	-		0	0
Seq	-		1	0		-	1
XIR	-		-	-		0	0

Blez, Bgtz n'utilisent pas Rt (Rt = 0)

Next instruction address



$C3 = (Bch \quad).\overline{XIR}$

$C4 = (Bch+Seq).\overline{XIR}$

$C2 = (Bltz+Bltzal+Bgez+Bgezal+ Blez+Bgtz) \overline{(Rs<0)}$

$C1 = (Bltz+Bltzal+Bgez+Bgezal+ Blez+Bgtz) (Rs<0)+Seq$

$C0 = (Rs=Rt)$

	C0		C1	C2		C3	C4
Beq T	1		1	1		1	1
Beq F	0		1	1		1	1
Bne T	0		0	0		1	1
Bne F	1		0	0		1	1
Bltz T	-		1	0		1	1
Bltz F	-		0	1		1	1
Blez T	1	Si Rs=Rt	1	0	Si Rs<0	1	1
Blez F	0		0	1		1	1
Bgtz T	0		0	1		1	1
Bgtz F	1		1	0		1	1
Bgez T	-		0	1		1	1
Bgez F	-		1	0		1	1
Jr	-		-	-		0	0
J	-		-	-		0	0
Seq	-		1	0		-	1
XIR	-		-	-		0	0