Implementation

- RISC vs. CISC concept
- Concept of pipeline
- An implementation of Mips
- Pipeline's problems

Implementation

How to mesure the performance ? Execution time

Clock frequency

Number of cycles per instruction (CPI)

$$\text{Performance} = \frac{\text{Clock Frequency}}{\text{CPI}}$$

Implementation

Objectives

Execute each instruction in one cycle

CPI = 1 cycle/inst.

Which hardware is required ?

Implementation

	Add
Read instruction	✓
Decode	✓
Read operands	✓ Rs, Rt
Make an operation	✓ +
Save the result	✓ Rd
Compute next inst. addr.	✓ next seq. addr.

Implementation

	Add	Lw	
Read instruction	✓	✓	
Decode	✓	✓	
Read operands	✓	✓	I , Rs
Make an operation	✓	✓	+
Memory access	o	✓	Read
Save the result	✓	✓	
Compute next inst. addr.	✓	✓	

Implementation

	Add	Lw	Sw	Jr
Read instruction	✓	✓	✓	✓
Decode	✓	✓	✓	✓
Read operands	✓	✓	✓	✓
Make an operation	✓	✓	✓	o
Memory access	o	✓	✓	o
Save the result	✓	✓	o	o
Compute next inst. addr.	✓	✓	✓	✓

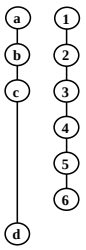
Implementation

All the instructions have the same execution scheme

- Read instruction
- Decode
- Read operands
- Make an operation
- Memory access
- Save the result
- Compute next inst. addr.

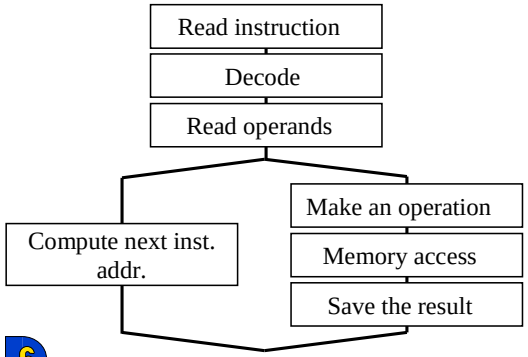
Implementation

In which order ?

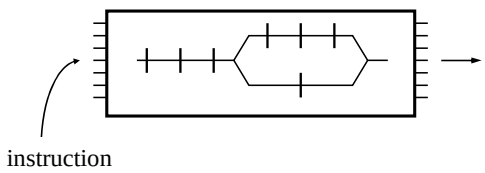


- Read instruction
- Decode
- Read operands
- Make an operation
- Memory access
- Save the result
- Compute next inst. addr.

Implementation

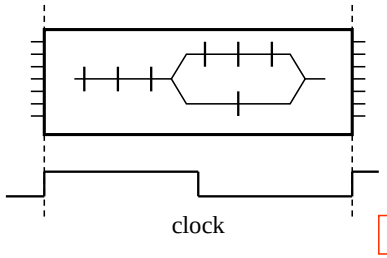


Implementation



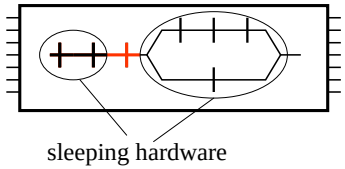
Implementation

Objective : One instruction = One cycle ?

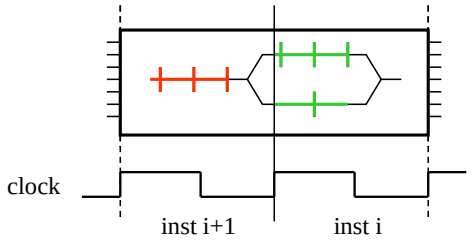


clock period ?

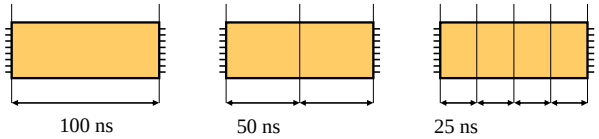
Implementation



Implementation



Implementation



10 M inst./s 20 M inst./s 40 M inst./s

Implementation

Is there any limitation ?

NO !

Implementation

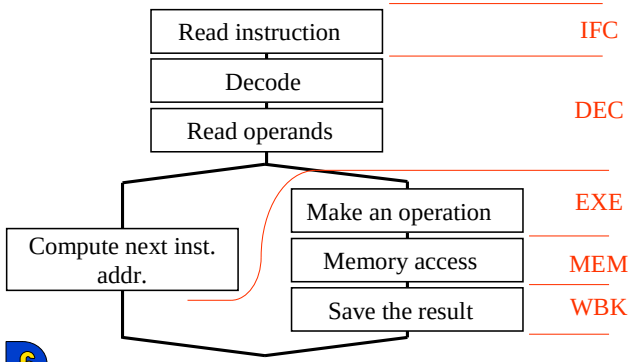
Pipeline rules :

- Pipeline stages must be separated by registers
- Pipeline must be as balanced as possible (all stages must have the same length)

Implementation

- RISC vs. CISC concept
- Concept of pipeline
- An implementation of Mips
- Pipeline's problems

Implementation



Implementation

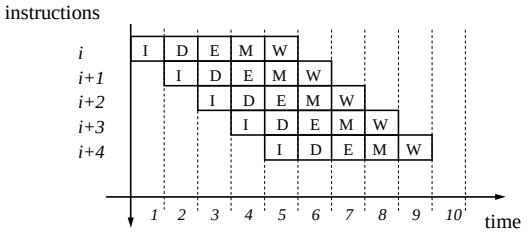
IFC
DEC
EXE
MEM
WBK

There is no relationship between pipeline stages and operations

The balance of a pipeline may change in the time

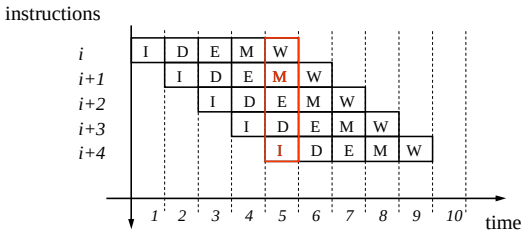
Implementation

At a given time, several instructions are executed inside a pipeline processor



Implementation

At each cycle there are 2 accesses to the memory



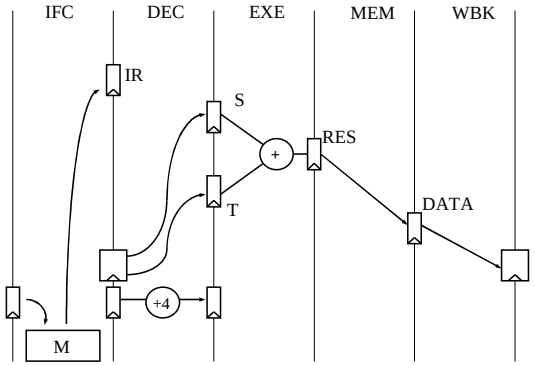
Implementation

Pipeline rules :

- Each piece of hardware must “belong” to a UNIQUE pipeline cycle

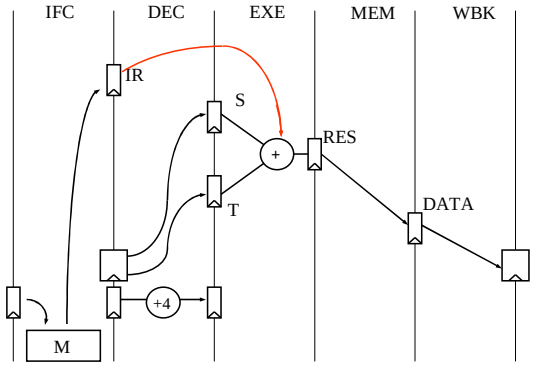
Implementation

Example : Add rd, rs, rt

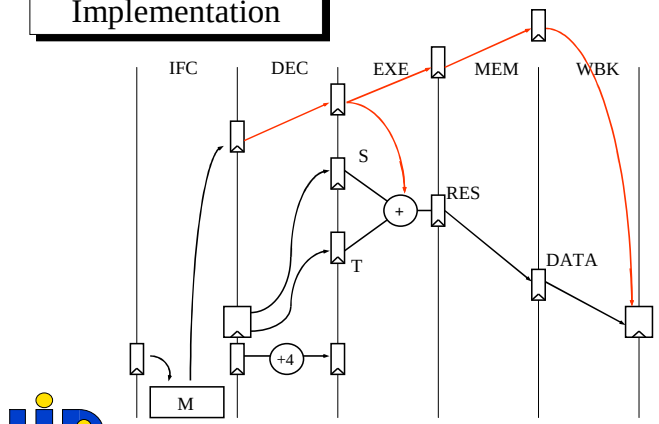


Implementation

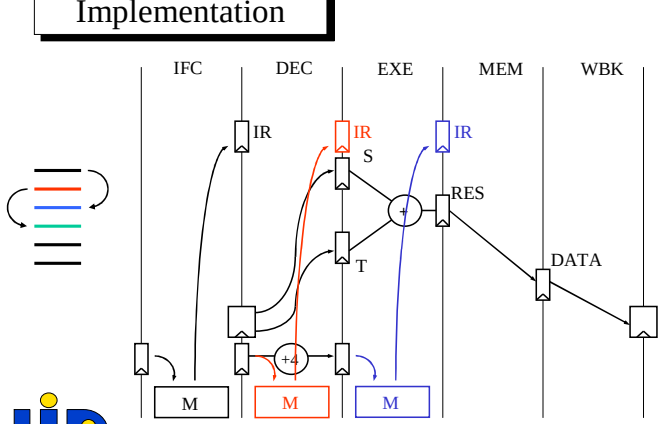
Example : Add rd, rs, rt



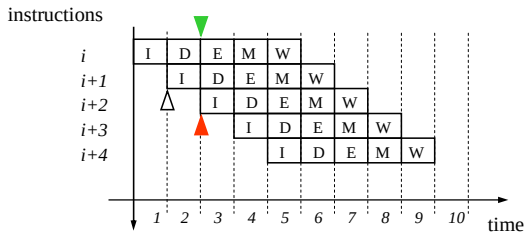
Implementation



Implementation



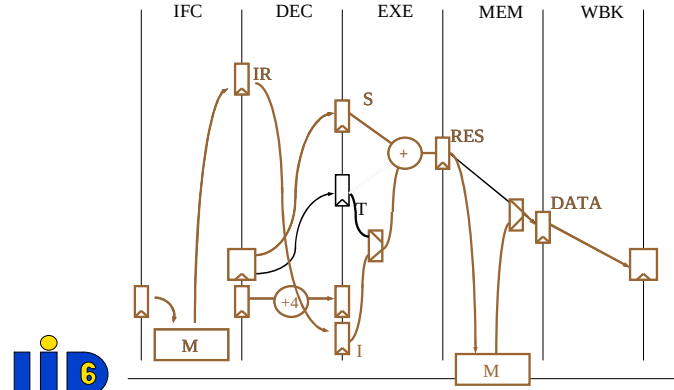
Implementation



In a pipeline processor the addr. calculated by the instr. *i* is the addr. of instr. *i+n* (n>1)
(for Mips n = 2)

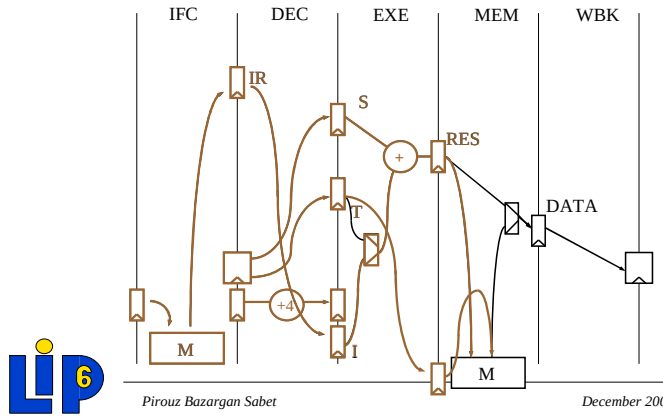
Implementation

Example : Lw rd, i(rs)



Implementation

Example : Sw rt, i(rs)



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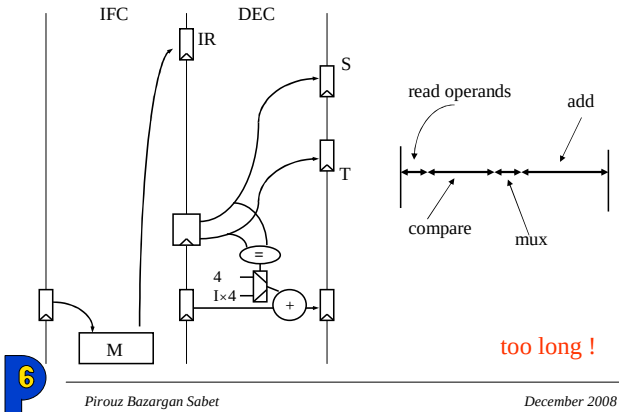
Implementation

Example : Beq rs, rt, label



too long !

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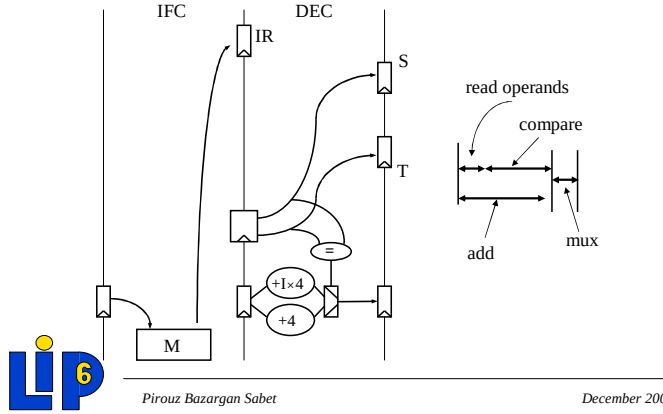
Implementation

Example : Beq rs, rt, label



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