

Implementation

- ❏ RISC vs. CISC concept
- ❏ Concept of pipeline
- ❏ An implementation of Mips
- ❏ Pipeline's problems



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December 2008

Implementation

Problem with branches



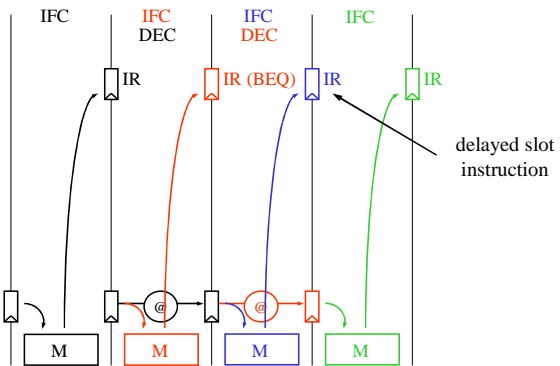
The instruction that follows a branch is always fetched from the memory



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Solutions :

- Avoid the execution of the delayed slot instruction
 - ⇒ Hardware control
- Let the instruction be executed
 - ⇒ Difficulties in assembly language

in contradiction with the RISC concept



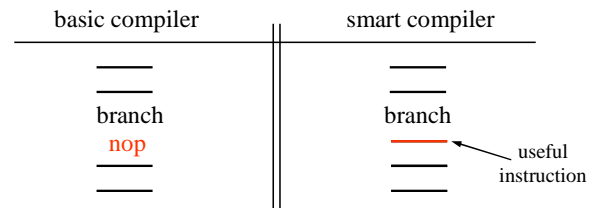
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The delayed slot instruction is always executed

The compiler has to be tuned to the processor and put an instruction after each branch



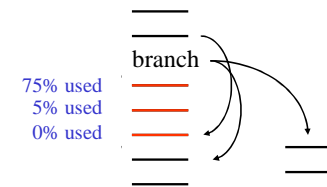
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The later the next instruction address is calculated

➡ greater number of delayed slots



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The problem of data dependency

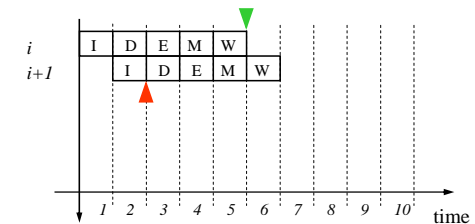


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Add r3, r2, r1
 Add r4, r3, r5



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Implementation

Solutions :

- Try to resolve the problem inside the hardware
 - ⇒ Hardware control
- Let the compiler avoid the problem
 - ⇒ Difficulties inside the compiler



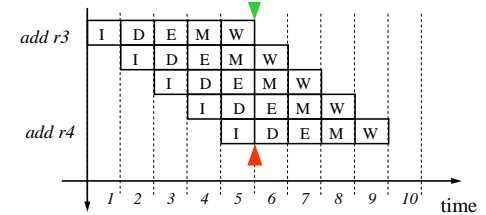
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Add r3, r2, r1

Add r4, r3, r5



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Implementation

Let the compiler avoid the problem

Add r3, r2, r1

nop
nop
nop

Add r4, r3, r5

—
—
—

Low performance



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Implementation

Solutions :

- Try to resolve the problem inside the hardware
 - ⇒ Hardware control
- Let the compiler avoid the problem
 - ⇒ Difficulties inside the compiler

in contradiction with the RISC concept but higher performance

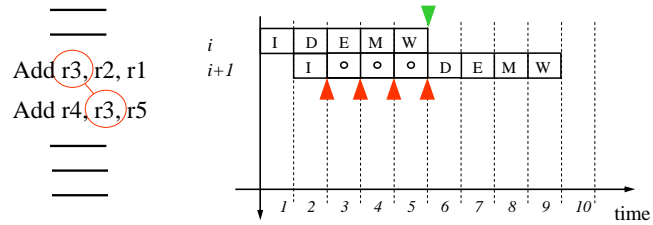


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Try to resolve the problem inside the hardware



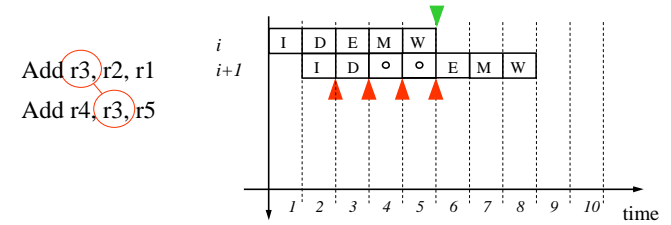
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Are 3 wait cycles really necessary ?

Data usage



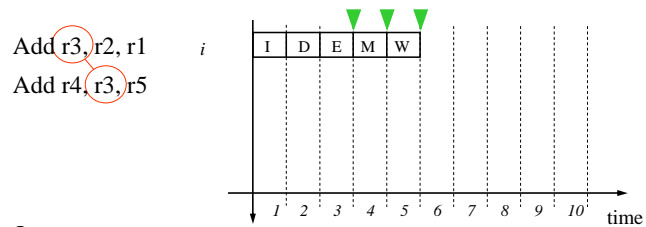
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Are 3 wait cycles really necessary ?

Data availability

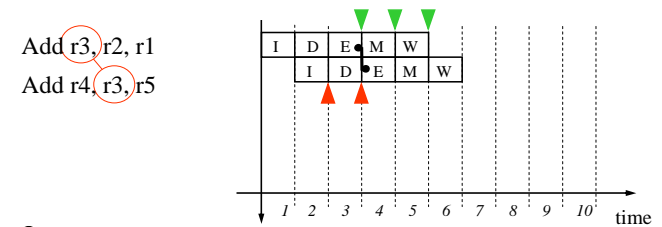


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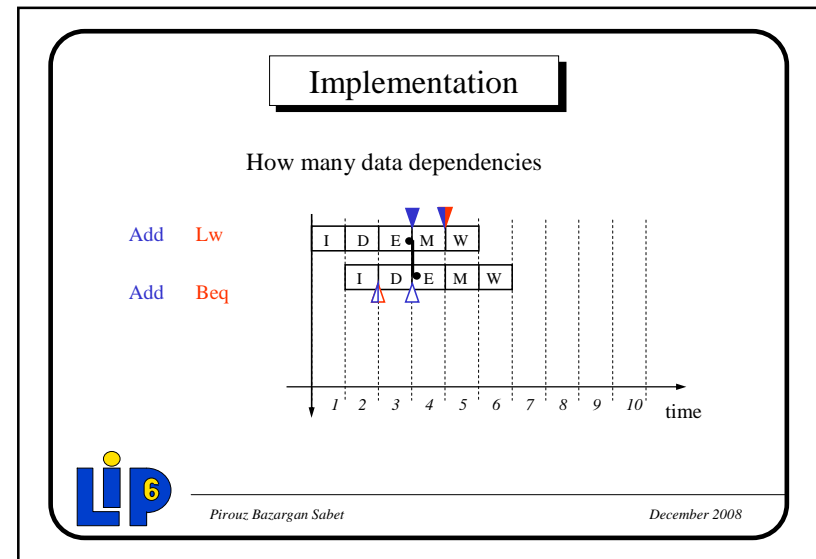
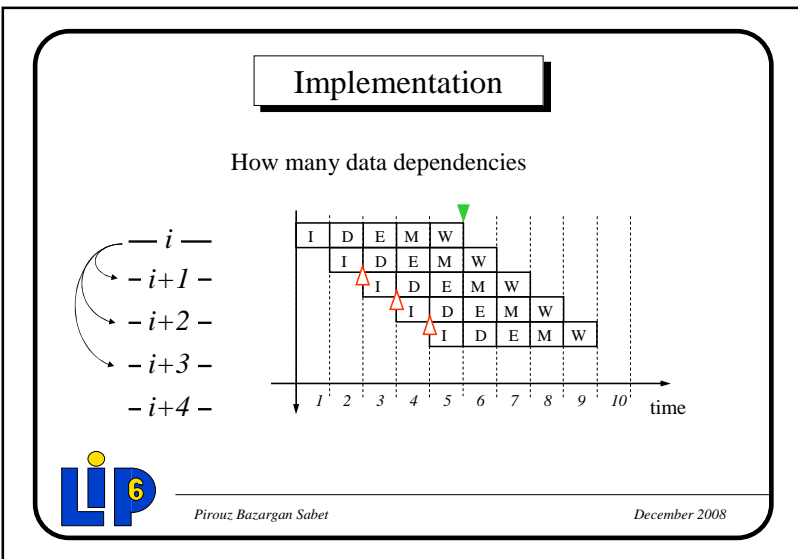
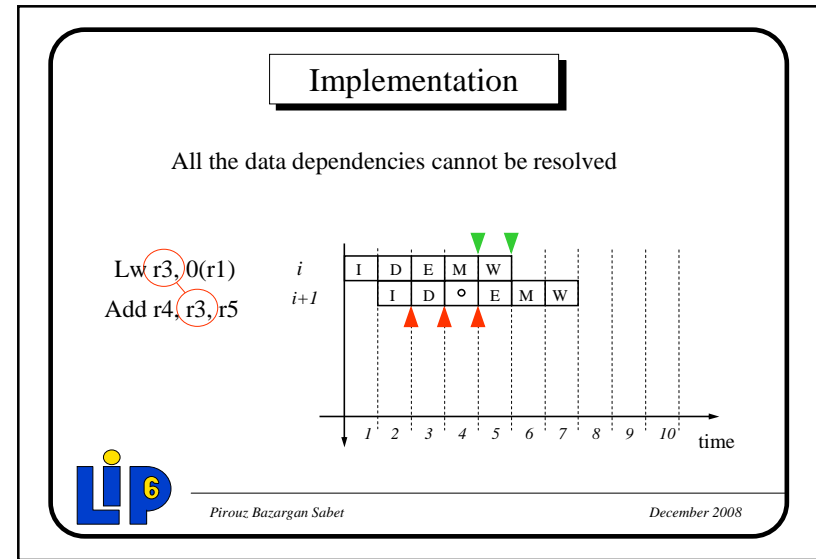
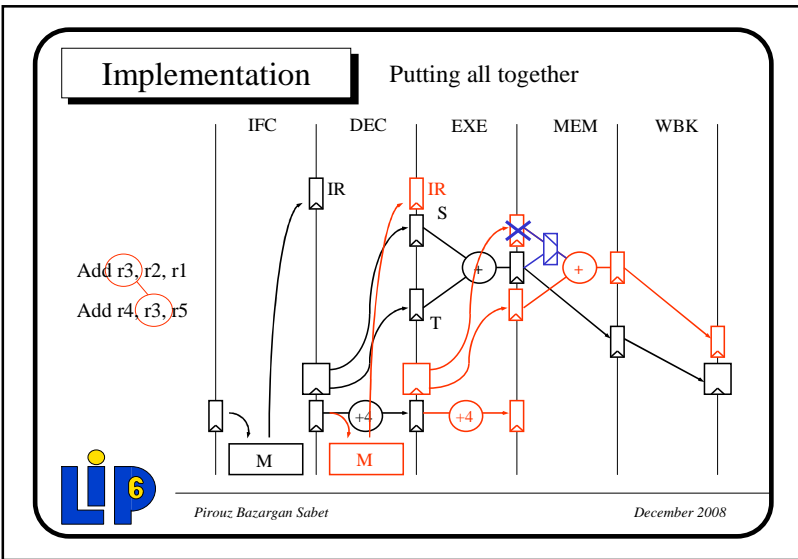
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Putting all together



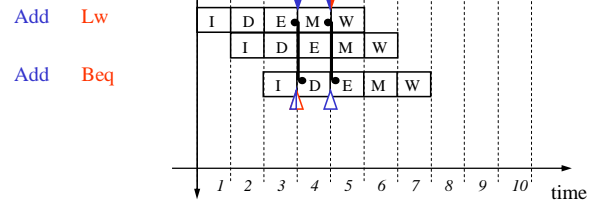
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How many data dependencies

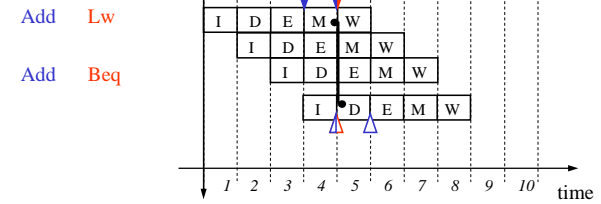


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How many data dependencies



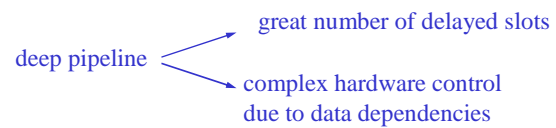
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Is there any limitation to deep pipelines ?

2 limitations



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