

Outline

- ❏ Introduction
- ❏ **Architecture of a RISC Processor**
- ❏ Implementation



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Architecture

- ❏ Software visible registers
- ❏ Memory Addressing
- ❏ The instruction set
- ❏ **The exception / reset mechanism**



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Exception / Reset

Exception / Interrupt / Reset mechanism :

- **Reset mechanism**
- Interrupt mechanism
- Exception mechanism



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Exception / Reset

Reset

Re-initialize the system (the processor and all the other components of the system)

- Abort the execution of the current program
- All the data are lost
- Re-initialize the software (including the OS)



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Exception / Reset

Reset Abort the current program
Jump to the Reset Handler

- Initialize the address of the next instruction : `0xBFC0 0000`
- Initialize the Status Register :

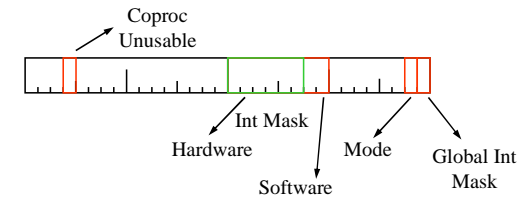


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Exception / Reset

Status Register



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Exception / Reset

Reset Abort the current program
Jump to the Reset Handler

- Initialize the address of the next instruction : `0xBFC0 0000`
- Initialize the Status Register : `0x0000 0000`



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Exception / Reset

Exception / Interrupt / Reset mechanism :

- Reset mechanism
- Interrupt mechanism
- Exception mechanism



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Exception / Reset

Exception vs. Interrupt

Interrupts are events that require the processor to perform some operation

Interrupts are normal events during the life of a program

Exceptions are events that denote a malfunction in the program

Exceptions are abnormal events during the life of a program

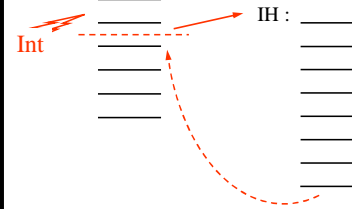


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Exception / Reset

Interrupt



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Exception / Reset

Interrupt Stop executing the current program
 Execute the Interrupt Handler
 Resume the interrupted program

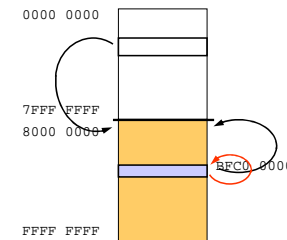
- Initialize the address of the next instruction :
 0x8000 0080



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Exception / Reset



What happens if an interrupt occurs during the boot ?

→ Goto 0x8000 0080

If the Os is not yet loaded ?

→ Goto 0xBFC0 0180



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Exception / Reset

- Status Register

The diagram shows a horizontal bar representing the Status Register. It is divided into several sections:

- Coproc Unusable**: A small red box at the top left.
- Boot Exception Vector**: A red box below the bar.
- Hardware**: A green box below the bar.
- Software**: A green box below the bar.
- Int Mask**: A green box below the bar.
- Mode**: A red box below the bar.
- Global Int Mask**: A red box below the bar.

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Exception / Reset

Reset Abort the current program
 Jump to the Reset Handler

- Initialize the address of the next instruction : **0xBFC0 0000**
- Initialize the Status Register : **0x0040 0000**

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Exception / Reset

Interrupt Stop executing the current program
 Execute the Interrupt Handler
 Resume the interrupted program

- Initialize the address of the next instruction :

if <i>BootExcVect</i> = 0	0x8000 0080
if <i>BootExcVect</i> = 1	0xBFC0 0180
- Set the SR : Mode (Kernel)

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Exception / Reset

The diagram illustrates the state during an interrupt. A vertical stack of memory locations is shown on the left. An interrupt signal (**Int**) points to a specific location. An interrupt handler box (**IH**) is shown to the right. A blue arrow labeled "Save the context" points from the memory stack to the IH box. Another blue arrow labeled "Restore the context" points from the IH box back to the memory stack. A red dashed arrow labeled "Int" points from the stack to the IH box.

Do not accept a new interrupt until the context is saved

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Exception / Reset

Interrupt Stop executing the current program
 Execute the Interrupt Handler
 Resume the interrupted program

- Initialize the address of the next instruction :
 if *BootExcVect* = 0 **0x8000 0080**
 if *BootExcVect* = 1 **0xBFC0 0180**

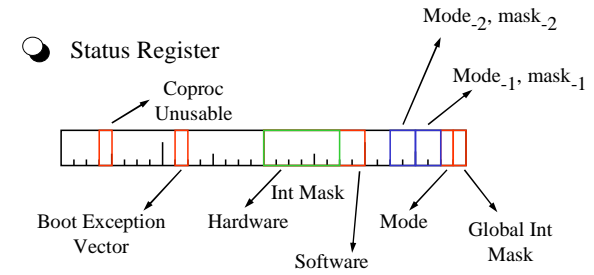
- Save the current Mode and Mask
- Set the SR : Mode (Kernel) , set the Global Int Mask



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Exception / Reset



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Exception / Reset

Interrupt Stop executing the current program
 Execute the Interrupt Handler
 Resume the interrupted program

- Initialize the address of the next instruction :
 if *BootExcVect* = 0 **0x8000 0080**
 if *BootExcVect* = 1 **0xBFC0 0180**

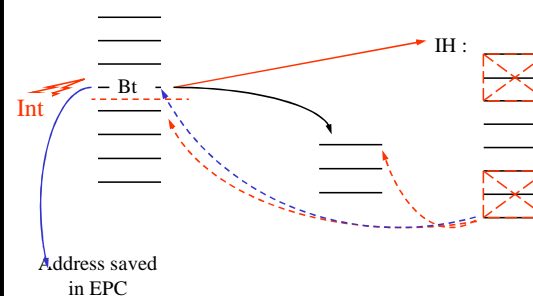
- Save the return address in EPC
- Save the current Mode and Mask
- Set the SR : Mode (Kernel) , set the Global Int Mask



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Exception / Reset



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Exception / Reset

- Cause Register

Branch Delayed Slot

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Exception / Reset

Interrupt Stop executing the current program
 Execute the Interrupt Handler
 Resume the interrupted program

- Initialize the address of the next instruction :
 if *BootExcVect* = 0 **0x8000 0080**
 if *BootExcVect* = 1 **0xBFC0 0180**
- Save the return address in EPC
- Save the current Mode and Mask
- Set the SR : Mode (Kernel) , set the Global Int Mask
- Set the Cause

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Exception / Reset

- Cause Register

Interrupt if set to 1

Branch Delayed Slot Hardware Software Exception code

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Exception / Reset

Reset Abort the current program
 Jump to the Reset Handler

- Initialize the address of the next instruction : **0xBFC0 0000**
- Initialize the Status Register : **0x0040 0000**
- Initialize the Cause Register : **0x0000 0000**

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Exception / Reset

Exception / Interrupt / Reset mechanism :

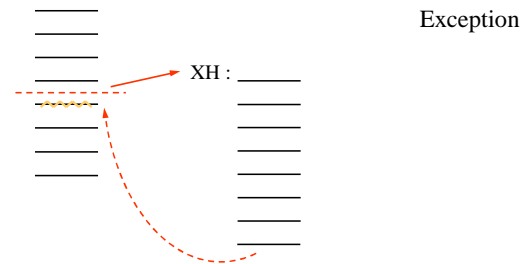
- Reset mechanism
- Interrupt mechanism
- Exception mechanism



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Exception / Reset



In most of the cases a faulty program is not resumed but killed



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Exception / Reset

Exception Stop executing the current program
Execute the Exception Handler
Resume the interrupted program

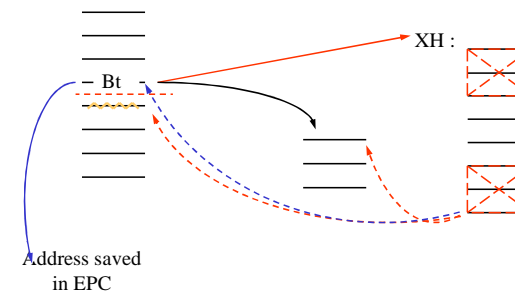
- Initialize the address of the next instruction :
0x8000 00800 or **0xBFC0 0180**
- Save the **faulty instruction's** address in EPC
- Save the current Mode and Mask
- Set the SR : Mode (Kernel) , set the Global Int Mask
- Set the Cause
- Set the BadVAddr



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Exception / Reset



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Exception / Reset

Exception causes

- Overflow
- Illegal read address (data or instruction)
- Illegal write address (data)
- Coprocessor unusable
- Unknown instruction
- Syscall
- Break
- Data bus error
- Instruction bus error



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Exception / Reset

Exception vs. Interrupt

Interrupts are events that require the processor to perform some operation

- Interrupts are asynchronous
- ⇒ no emergency

Exceptions are events that denote a malfunction in the program

An exception is an error
⇒ the faulty instruction should NOT be executed



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