Outline

- Introduction
- Architecture of a RISC Processor
- Implementation

Implementation

- RISC vs. CISC concept
- Concept of pipeline
- An implementation of Mips
- Pipeline's problems

Exception / Reset

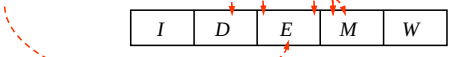
Implementation of the :

- Reset mechanism
- Interrupt mechanism
- Exception mechanism

Exception

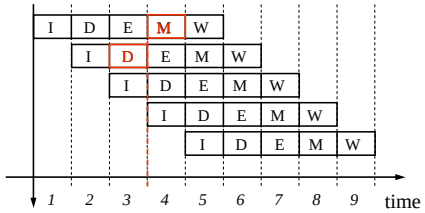
- Overflow
- Illegal read address
- Illegal write address
- Coporcessor unusable
- Unknown instruction
- Syscall
- Break
- Data bus error
- Instruction bus error

How stop the pipeline ?



Exception

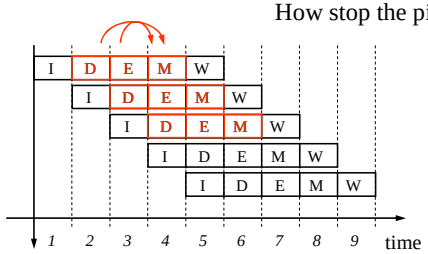
How stop the pipeline ?



Exceptions should be seen in the same order as the instructions (exact exception)

Exception

How stop the pipeline ?



Forward all the sources to the same cycle

Postpone the reaction to an exception

Exception

When stop the pipeline ?

Exceptions are events that denote a malfunction in the program

An exception is an error

⇨ the faulty instruction should NOT be executed

A faulty instruction should not modify the state of the system . . . from the software point of view

Protect software visible registers and the memory

Exception

When stop the pipeline ?

Exception

- Overflow
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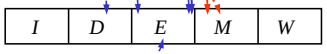
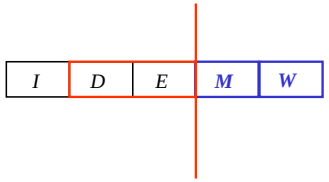
How stop the pipeline ?



Exception

When stop the pipeline ?



Exception

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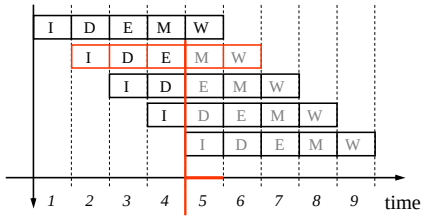
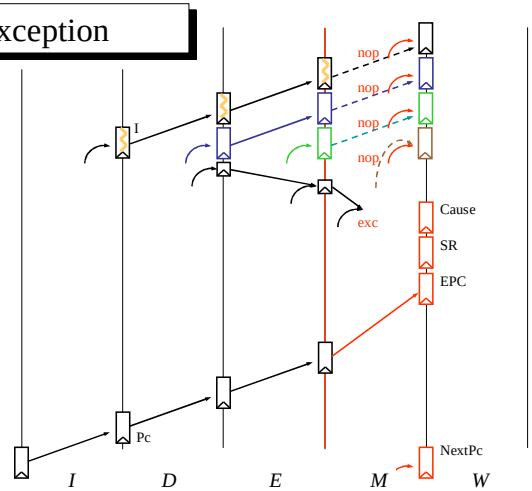
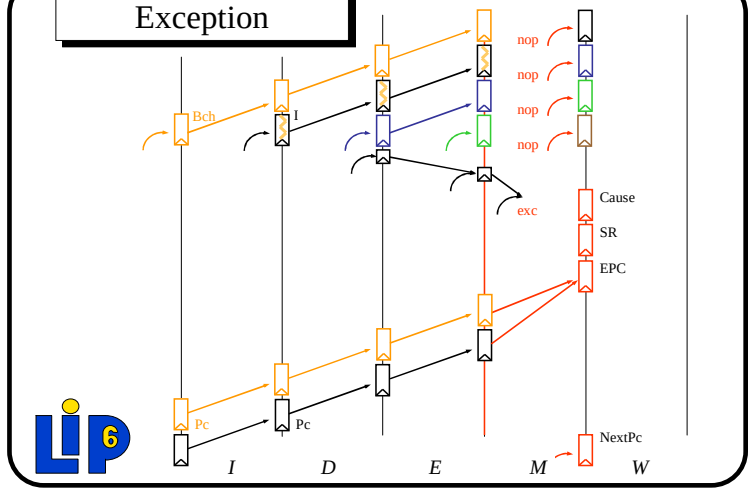


Exception



Exception



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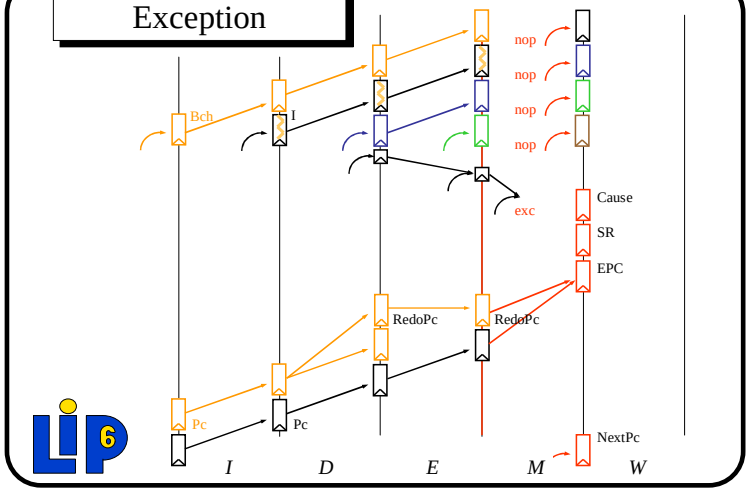


Exception / Reset

Implementation of the :

- Reset mechanism
- Interrupt mechanism
- Exception mechanism

Interrupt

When stop the pipeline ?

Interrupts are events that require the processor to perform some operation

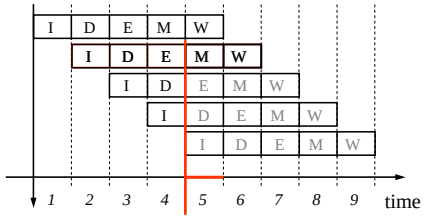
Interrupts are asynchronous
⇨ no emergency

Exceptions are events that denote a malfunction in the program

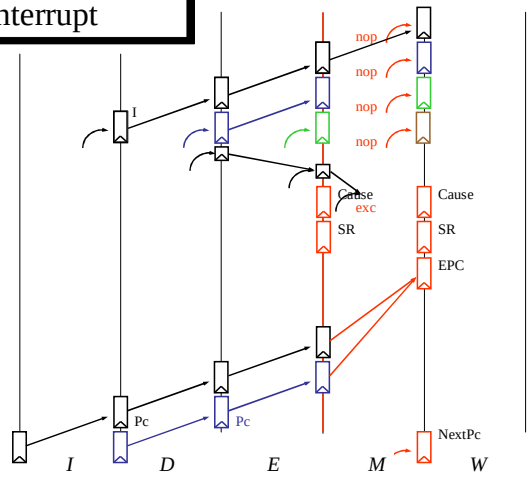
An exception is an error
⇨ the faulty instruction should NOT be executed

Interrupt

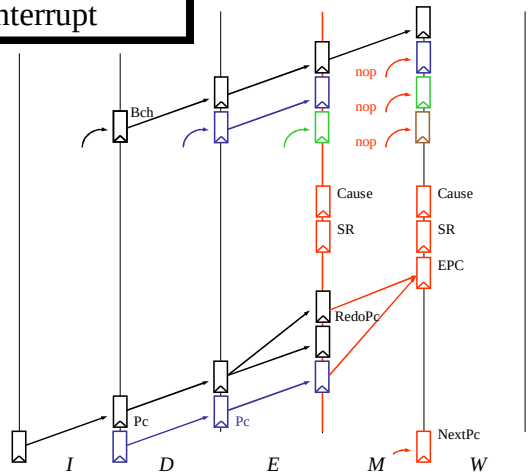
When stop the pipeline ?



Interrupt



Interrupt



Exception / Reset

Implementation of the :

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Reset

Reset — Abort the current program
Jump to the Reset Handler

- Initialize the address of the next instruction : `0xBFC0 0000`
- Initialize the Status Register : `0x0040 0000`
- Initialize the Cause Register : `0x0000 0000`

Reset