SocLib is an open IP-core library, with at least 4 implementations:

- CABA (Bit cycle accurate) in [SystemC]
- Tlm (Transaction level modeling) in SystemC
- Tlm/T (Transaction level modeling with time) in SystemC
- RTL (Register transfer layer) in Vhdl or Verilog

Many IPs are defined, in which:

- CPUs (PPC, OpenRisc, Mips, ...)
- Rams, Roms, ...
- Interconnection components (Micro-networks on chip (NoC) and Buses)
    - VCI
    - PI-Bus
- Dedicated components for application support
    - SpinLock oriented rams
    - MwMr controllers

It may be obtained on ?https://www-asim.lip6.fr/trac/soclib