– Curriculum Vitae –

Adrien Cassagne
Born on February 2, 1989 in Pau (64)
adrien.cassagne@lip6.fr
https://lip6.fr/adrien.cassagne/

French, Driving license
+33 1 44 27 65 61

Work Address
Laboratoire d'Informatique de Paris 6 (LIP6)
4 Place Jussieu, 75005 Paris, France
Office: 24-25/403

Current Work Activity

2021 to today **Associate Professor at Sorbonne University** (tenured position)
Computer science laboratory of Paris 6 (LIP6), Architecture and Software for System-on-a-Chip (ALSoC) team

- **Research topics:** Algorithm-architecture adequacy, Semi-auto. exploration, Vectorization
- **Teaching:** Architecture of computers, Operating systems, High performance computing
- **Keywords:** Parallelization, Optimization, SIMD, Embedded architectures, RISC-V

Academic Education

2017 - 2020 **PhD's degree in Computer Science at University of Bordeaux**
Inria / IMS labs

- **Title:** Optimization and Parallelization Methods for Software-Defined Radio [M]
- **Keywords:** Software-defined radio, Functional simulation, Error correcting codes, Software implementation, Optimization, Parallelization, Open source code
- **Jury:**

Lionel Lacassagne	(Full Prof.)	Sorbonne University - LIP6	*Member*
Matthieu Gautier	(Associate Prof.)	University of Rennes 1 - IRISA	*Member*
Michel Jezequel	(Full Prof.)	IMT Atlantique	*President*
Cédric Bastoul	(Full Prof.)	University of Strasbourg - Huawei Paris	*Member*
Camille Leroux	(Associate Prof.)	Bordeaux INP - IMS	*Co-supervisor*
Olivier Aumage	(Tenured Researcher)	Inria Bordeaux - Sud-Ouest	*Co-supervisor*
Christophe Jégo	(Full Prof.)	Bordeaux INP - IMS	*Co-director*
Denis Barthou	(Full Prof.)	Bordeaux INP - LaBRI	*Co-director*

2010 - 2013 **Master's degree in Computer Science at University of Bordeaux**

- **Specialty:** Network, System and Mobility
- **Option:** High Performance Computing
- **Master's thesis:** "Multi GPU Implementation of the Spectral Differences Method for a CFD Code"
  https://www.cerfacs.fr/~cfdbib/repository/WN_CFD_14_5.pdf (in french)

2008 - 2014 **Master's degree in Computer Science at EPSI Bordeaux Engineer School**

- **Specialty:** Computer Science and Information Systems
- **Option:** Software Engineering
- **Master's thesis:** "Study and Implementation of a Computational Method for Digital Simulations on Modern Architectures"
  https://lip6.fr/adrien.cassagne/docs/reports/memoire.pdf (in french)

Work Experience

2020 - 2021 *(1 year)*
Teaching Assistant at ENSEIRB-MATMECA Engineer School
IMS lab (Bordeaux)

- **Research topic:** Optimization of compute intensive algorithms related to the software-defined radio (focus on real time applications)
- **Teaching:** Architecture of computers, Operating systems, Network, Web-based technologies

2015 - 2017 *(2 years)*
High Performance Computing Engineer at Inria and IMS labs (Bordeaux)

- **Advisors:** Bertrand Le Gal, Denis Barthou
- **ANR NAND:** Development of an HPC Monte-Carlo simulation chain for error correcting codes
- **IdEx CPU:** Optimization of channel coding algorithms (decoders) on general purpose processors

2014 - 2015 *(1 year)*
High Performance Computing and System Engineer at CINES (french computing center at Montpellier)

- **Advisors:** Olivier Rouchon, Eric Boyer
- **European projects:** Involvement into the PRACE project (Partnership for Advanced Computing in Europe) with the implementation of an OpenMP/MPI hybrid approach on a CFD code (DOI: `10.13140/RG.2.2.19469.79849`)
- **Teaching:** Realization of the "Debug & Optimization" training
- **Support:** Involvement into the support activities for the Occigen supercomputer's users

Apr. 2013 - Jan. 2014 *(10 months)*
Master of Sc. Intern at CERFACS (Toulouse)

- **Advisors:** Isabelle D'Ast, Jean-François Boussuge, Guillaume Puigt, Nadège Villedieu
- **Topic:** Optimization of an high order method for the digital computational fluid dynamics [Ic1]

`http://gpuigt.free.fr/jaguar.html`

Fields of Expertise

Research themes

- Algorithm-architecture adequacy: design of parallel algorithms for multi-cores and SIMD processors
- Portable SIMD multi-ISA (SSE, AVX, AVX-512, Neon, RVV, ...) library
- Optimization of high performance computing codes
- Digital communication systems
- Channel coding (polar codes, turbo codes, LDPC codes)

Related Themes

- Domain specific languages
- Deployment and maintenance of scientific applications
- Reproducible science
- Software engineering

Parallel and Concurrent Programming

- SIMD instructions: SSE, AVX, AVX-512, NEON, SVE, RVV
- Multi-threads: OpenMP, threads POSIX, lock-free synchronizations, active waiting (spin-lock), passive waiting (conditions), tasks, software pipeline, fork-join model
- GPU: CUDA, OpenCL, OpenACC
- Multi-nodes: PVM, MPI, peer to peer blocking / non-blocking communications, collective blocking / non-blocking communications
- Middleware/Runtime : StarPU, AFF3CT

Tools

- Operating Systems: Linux, macOS & Windows
- Programing languages: C, C++, Fortran, Python, x86 / MIPS / ARM assembly, JavaScript
- Software: LaTeX, Git, Office, JabRef

Teaching Activities

Position	Year	Title	Institution	Target	# hours
Engineer	2014-2015	Debug & Optimization	CINES	PhD/Engineer	18.00 h
Engineer	2015-2016	Debug & Optimization	CINES	PhD/Engineer	18.00 h
Engineer	2016-2017	Debug & Optimization	CINES	PhD/Engineer	18.00 h
PhD student	2017-2018	Debug & Optimization	CINES	PhD/Engineer	18.00 h
		Project of imperative programming	ENSEIRB-MATMECA	Bachelor	25.00 h
		Introduction to networking	ENSEIRB-MATMECA	Bachelor	16.50 h
		TCP/IP applications	ENSEIRB-MATMECA	Master	16.67 h
PhD student	2019-2020	Structure of computers	ENSEIRB-MATMECA	Bachelor	20.00 h
Teaching ass.	2020-2021	Introduction to networking	ENSEIRB-MATMECA	Bachelor	16.50 h
		Structure of computers	ENSEIRB-MATMECA	Bachelor	40.00 h
		Architecture of computers	ENSEIRB-MATMECA	Bachelor	35.00 h
		Operating systems	ENSEIRB-MATMECA	Master	16.00 h
		TCP/IP network architecture	ENSEIRB-MATMECA	Master	27.50 h
		TCP/IP applications	ENSEIRB-MATMECA	Master	16.67 h
		Web development	ENSEIRB-MATMECA	Master	30.00 h
		Web project	ENSEIRB-MATMECA	Master	30.00 h
Ass. prof.	2021-2022	High performance computing	Polytech Sorbonne	Master	28.00 h
		System programming	Polytech Sorbonne	Bachelor	20.00 h
		Architecture of computers	Sorbonne University	Bachelor	38.50 h
		Hot topics	Sorbonne University	Master	2.00 h
		Operating systems	Sorbonne University	Bachelor	38.50 h
				Total:	488.84 h

Summary table of teachings.

Open Source Projects

• **MyIntrinsics++ (MIPP)**

Description: MIPP is a portable library, written in C++, which encapsulates SIMD instruction sets (SSE, AVX, AVX-512 et NEON). It is extensible to new instruction sets. The library supports floating-point and integer representations (8-bit, 16-bit, 32-bit & 64-bit). MIPP can be easily integrated by any compute intensive application.

`https://github.com/aff3ct/MIPP/`

• **A Fast Forward Error Correction Toolbox (AFF3CT)**

Description: AFF3CT is a C++ toolbox dedicated to the simulation of digital communication systems. This type of systems involves different treatments such as channel coding, digital modulation and noise noise models for example. These different processes have been optimized to run fast (with MIPP) and are packaged into the library. AFF3CT focuses on error-correcting codes and supports a wide variety: turbo codes (4G), polar codes (5G), LDPC codes (Wi-Fi, 5G), ...

`https://github.com/aff3ct/aff3ct/`

`https://aff3ct.github.io`

Lists of Publications

• Ph.D. Manuscript

[M] **A. Cassagne**, "Optimization and Parallelization Methods for Software-Defined Radio". 2020. URL: https://www.theses.fr/2020BORD0231.

• International Journals with Proceedings

[IJ3] **A. Cassagne**, O. Hartmann, M. Léonardon, K. He, C. Leroux, R. Tajan, O. Aumage, D. Barthou, T. Tonnellier, V. Pignoly, B. Le Gal and C. Jégo. "AFF3CT: A Fast Forward Error Correction Toolbox!". *Elsevier SoftwareX*, 2019. DOI: 10.1016/j.softx.2019.100345.

[IJ2] A. Ghaffari, M. Léonardon, **A. Cassagne**, C. Leroux and Y. Savaria. "Toward High Performance Implementation of 5G SCMA Algorithms". *IEEE Access*, 2019. DOI: 10.1109/ACCESS.2019.2891597. JCR indexed.

[IJ1] M. Léonardon, **A. Cassagne**, C. Leroux, C. Jégo, L-P. Hamelin and Y. Savaria. "Fast and Flexible Software Polar List Decoders". *Springer Journal of Signal Processing Systems (JSPS)*, 2019. DOI: 10.1007/s11265-018-1430-3. JCR indexed.

• International Workshops and Conferences with Proceedings

[IC5] **A. Cassagne**, M. Léonardon, R. Tajan, C. Leroux, C. Jégo, O. Aumage and D. Barthou. "A Flexible and Portable Real-time DVB-S2 Transceiver using Multicore and SIMD CPUs". *IEEE International Symposium on Topics in Coding (ISTC)*, Montréal, Canada, September 2021. DOI: 10.1109/ISTC49272.2021.9594063.

[IC4] **A. Cassagne**, O. Aumage, D. Barthou, C. Leroux and C. Jégo. "MIPP: A Portable C++ SIMD Wrapper and its use for Error Correction Coding in 5G Standard". *ACM Workshop on Programming Models for SIMD/Vector Processing (WPMVP)*, Vösendorf/Wien, Austria, February 2018. DOI: 10.1145/3178433.3178435.

[IC3] **A. Cassagne**, T. Tonnellier, C. Leroux, B. Le Gal, O. Aumage and D. Barthou. "Beyond Gbps Turbo Decoder on Multi-core CPUs". *IEEE International Symposium on Turbo Codes and Iterative Information Processing (ISTC)*, Brest, France, September 2016. DOI: 10.1109/ISTC.2016.7593092.

[IC2] **A. Cassagne**, O. Aumage, C. Leroux, D. Barthou and B. Le Gal. "Energy Consumption Analysis of Software Polar Decoders on Low Power Processors". *IEEE European Signal Processing Conference (EUSIPCO)*, Budapest, Hungary, August 2016. DOI: 10.1109/EUSIPCO.2016.7760327.

[IC1] **A. Cassagne**, B. Le Gal, C. Leroux, O. Aumage and D. Barthou. "An Efficient, Portable and Generic Library for Successive Cancellation Decoding of Polar Codes". *Springer International Workshop on Languages and Compilers for Parallel Computing (LCPC)*, Raleigh, NC, USA, September 2015. DOI: 10.1007/978-3-319-29778-1_19.

• Preprints

[P1] **A. Cassagne**, R. Tajan, O. Aumage, D. Barthou, C. Leroux and C. Jégo, "A DSEL for High Throughput and Low Latency Software-Defined Radio on Multicore CPUs". June 2022. DOI: 10.48550/arXiv.2206.06147.

• International Workshops and Conferences without Proceedings

[Ic2] **A. Cassagne**, O. Hartmann, M. Léonardon, T. Tonnellier, G. Delbergue, C. Leroux, R. Tajan, B. Le Gal, C. Jégo, O. Aumage and D. Barthou. "Fast Simulation and Prototyping with AFF3CT". *IEEE International Workshop on Signal Processing Systems (SiPS)*, Lorient, France, October 2017. DOI: 10.13140/RG.2.2.10295.42409/1.

[Ic1] **A. Cassagne**, J-F. Boussuge, G. Puigt, N. Villedieu, I. D'Ast and A. Genot. "JAGUAR: A New CFD Code Dedicated to Massively Parallel High-Order LES Computations on Complex Geometry". *3AF International Conference on Applied Aerodynamics (AERO 2015)*, Toulouse, France, March 2015. DOI: 10.6084/m9.figshare.12173466.v1.

• National Conferences without Proceedings

[NC1] **A. Cassagne**, M. Léonardon, O. Hartmann, T. Tonnellier, G. Delbergue, V. Giraud, C. Leroux, R. Tajan, B. Le Gal, C. Jégo, O. Aumage and D. Barthou. "AFF3CT : Un environnement de simulation pour le codage de canal". *GdR SoC2*, Bordeaux, France, June 2017. DOI: 10.13140/RG.2.2.13492.91520.