

# All-digital PLL array provides reliable distributed clock for SOCs

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**Abstract**— This brief addresses the problem of clock generation and distribution in globally synchronous locally synchronous chips. A novel architecture of clock generation based on network of coupled all-digital PLLs is proposed. Solutions are proposed to overcome the issues of stability and undesirable synchronized modes (modelocks) of high-order bidirectional PLL networks. The VLSI implementation of the network is discussed in CMOS65 nm technology and the simulation results prove the reliability of the global synchronization by the proposed method.

## I. INTRODUCTION

Difficulties of clock distribution inside MPSOCs in nanometer technologies in terms of reliability and power consumption efficiency are underlined in numerous recent studies [1][2]. In modern technologies, traditional clock distribution approaches (such as clock tree, clock grid and etc) suffer from uncertainty of increased propagation delays and supply noise. Moreover, the power consumption may be increased up to a half of the chip power budget in order to satisfy the timing constraints. Globally Asynchronous Locally Synchronous (GALS) timing approaches are proposed in several works as an alternative for Globally Synchronous Locally Synchronous (GSLs) approaches. The main drawback to overcome is the risk of metastability failure at interconnections between synchronous clock areas (SCA) and the global asynchronous system (NOC). Although this risk can be reduced, it can be never fully eliminated. Hence, GALS approaches are not suitable for critical applications such as cardiac stimulation chips, nuclear power plant control, automatic driving panels of vehicles and etc. To date, GSLs remains the only reliable solution for data exchanges inside a chip.

To get around these difficulties, recently, several alternative architectures of global clock generation have been proposed, having in common a distributed generation of the clock signal. This is generally achieved using an array of coupled oscillators, each oscillator being placed in the center of the local synchronous area. The oscillators are coupled in the domain of voltages/current (by injection locking) [3] or in the phase domain (PLL array)[5]. Such a distributed system guarantees a synchronisation between all neighboring synchronous areas of the chips. This eliminates the problem common to clock trees,

where a resynchronisation is needed between neighboring SCA locally synchronized by the tree leaves belonging to different branches.

A distributed clock generator must be closely integrated with the functional digital blocks of the chips, and this requirement is difficultly compatible with the analog nature of injection-coupled oscillator array, both because of the environment digital noise and because of the difficulties to establish a reliable automated design flow. To be a success, a distributed clock generator operation must be implemented with digital electronics. This is only achievable if the oscillators are coupled in the phase domain, i.e., the array represents a network of coupled phase locked loop. A feasibility of such a clock generator was demonstrated by Pratt et. al [5] and Gutnik et. al [6]. However, the implemented PLL network suffered from the same issues than the injection locking based architectures, since it was based on fully-analog PLLs.

In this work, a novel architecture of phase locked coupled oscillators based on All-Digital PLLs (ADPLLs) is proposed. Fundamental problems of coupled PLL underlined by Pratt [5], consisted in existence of undesirable synchronization modes (called modelocks), is solved in a simple and original way, by a dynamic reconfiguration of the network interconnection topology at the starting stage. The stability of high-order networks, which is one of the major drawbacks of PLL arrays, is also addressed. This paper is organized as follows: The proposed architecture, with discussion of stability and modelock issues, is presented in section II. The VLSI implementation of the network is presented in section III and the simulation results in CMOS 65 nm are presented in section IV.

## II. ARCHITECTURE

The overall architecture of the clock generation network is presented in Fig. 1. The network is composed of digital Phase-Frequency Detectors (PFD) and of filter/oscillator (FO) blocks (16 in this example), and the PFDs are placed on each border between two SCAs, measuring the error between each couple of neighboring oscillators. The PFD placed in upper left corner compares the phase of the input reference and the first oscillator in the network. Such a network, if properly designed, synchronises at the phase of the reference clock.

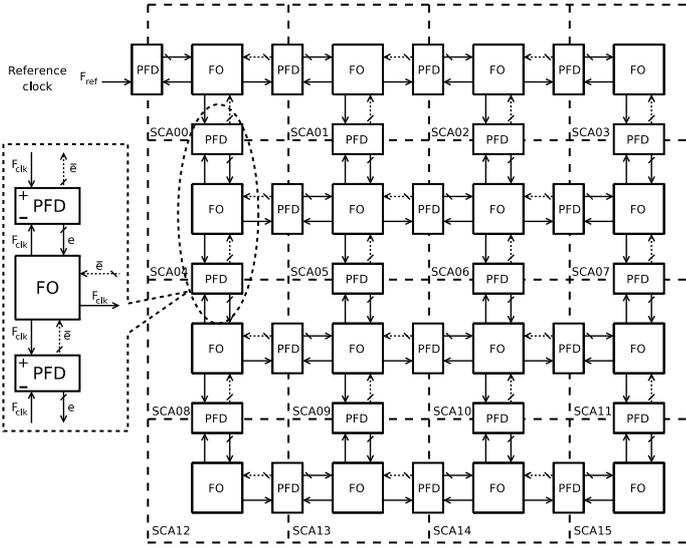


Fig. 1. Architecture of the ADPLL network.

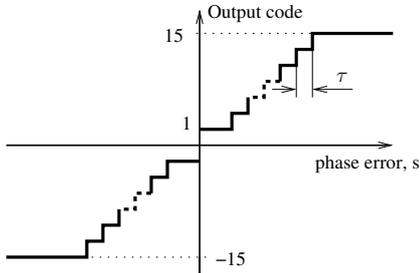


Fig. 2. Phase code relation of the PFD.

The PFDs have the phase-code characteristic presented in Fig. 2. The PFDs can be seen as analog-to-digital converter, easily implementable with digital circuits. The filter is a digital proportional-integral filter and the oscillator is a digitally controlled oscillator (DCO). The clock generator uses the DCO signal divided by  $N$  to sample the loop digital filter and to compare the phase of neighboring oscillators. The FO blocks receive the information from up to 4 the PFDs measuring the phase error between the local DCO and the neighbors; the number of FO inputs depends on its position in the network.

#### A. Modelock elimination

The work of Pratt [5] highlighted existence of non-desirable stable states of the PLL network called "modelocks", in which all oscillators have the same frequencies, but may have fixed non-zero phase shift with regard to their neighbors. This is due to cyclic (modular) nature of phase and to large number of degrees of freedom in the system. To suppress modelocks, Pratt recommends the use of a particular PFD with non-monotonous phase-voltage characteristic.

To allow the use of a conventional linear PFD (Fig. 2), we propose an alternative solution. It is known, that modelocks cannot appear if the propagation of information is unidirectional. Such a mode can be implemented if each node receives

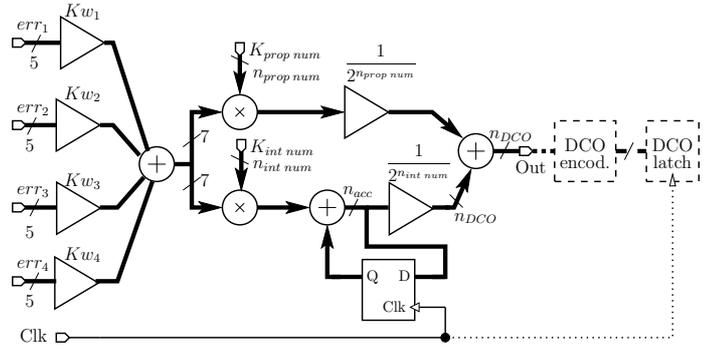


Fig. 3. Architecture of the designed filter.

the information about only the errors between, for instance, upper and left neighbors (cf. Fig. 1 without dotted links). Such a network topology excludes cycles of propagation of information, hence eliminates the possibility of modelocks. However, in such an operation mode the suppression of perturbations is weak, and, particularly, any perturbation appearing in early nodes will be propagated through all the network (cf. section IV), degrading the quality of clock in areas far from the reference point (the "root" node).

For this reason, we propose to implement two phases of network starting. During the first phase, the network operates in an unidirectional mode, converging after some time to a synchronous operation with zero average phase errors. This is achieved by programming the weight coefficients of the network ( $Kw_i$ , Fig. 3) by putting some of them to zero, hence disabling the corresponding link. After the network is synchronized, the reverse links are activated, and the network operates in a fully synchronous mode with distributed feedback (coupling) maintaining the synchronization. Such an operation scenario relaxes the requirement on the complexity for the PFD. The linear region of the phase-code characteristic must only cover the small error range, allowing an increase of the sensitivity (parameter  $\tau$  in Fig. 2) without increasing the number of bits (max. 4-5).

#### B. Stability of the network

The stability issues of stand-alone second-order PLLs have been well studied in literature. However, interconnecting several PLLs in a network increases the order of the system, making necessary a robust design procedure guaranteeing global stability. We developed a mathematical tool based on the control theory, allowing to synthesise the node loop filter guaranteeing that. The design procedure is inspired by the decentralized  $H_\infty$  control approach making use of the dissipative properties of the system [7]. The system is first represented as a loop including a sub-system of unidirectional chain of the network nodes  $\tilde{T}$ , and a sub-system  $M$  representing interconnections in the network (Fig. 4).  $ref$  represents the input phase of the reference,  $\epsilon$  represents the phase errors between neighbors which should converge to zero. In this way, the procedure of filter synthesis is done in two steps: firstly, the local stability (that of the matrix  $\tilde{T}$  is ensured, then the

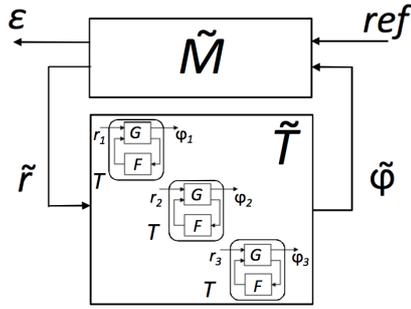


Fig. 4. Representation of the PLL network for stability study.

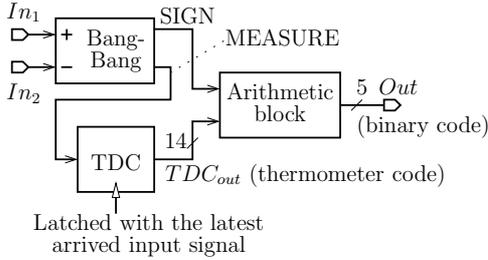


Fig. 5. Architecture of the designed PFD.

global stability is guaranteed. The procedure provides to the VLSI designers the range of stable filter coefficient values.

### III. VLSI IMPLEMENTATION

For VLSI implementation, the following specification were fixed: the technology is CMOS 65nm of ST Microelectronics, the nominal output DCO frequency is 1 GHz, the divided frequency is 250 MHz, the maximal tolerable phase error between the neighboring DCOs is below 10% of the period.

#### A. PFD

The architecture of the PFD includes a Bang-Bang phase detector (BB) measuring the sign of the phase error, a Time-To-Digital converter (TDC) generating a thermometer integer code corresponding to the value of the phase error in the time domain, and an arithmetic block generating a signed binary integer representation of the phase error from these two informations (Fig. 5).

The bang-bang phase detector architecture is inspired by [8]; it can be seen as a finite-state automaton [9]. The role of the BB phase detector is to detect the order at which the events come to its inputs, and to generate a sign of the phase error (the SIGN signal) and a pulse whose width represents the absolute value of the phase error (the MEASURE signal). The TDC converts the duration of the MEASURE signal into a digital code. This is done using a delay-line thermometer code time-to-digital converter architecture [10]. In our case, the TDC have 14 stages, allowing 14 levels of output. The delay of each stage is  $\tau$ , except for the first stage having a delay of approximately  $2\tau$  due to implementation reasons. The TDC output values start from 1 for errors below  $\tau$ , and go up to 15 for error greater than  $14\tau$ . After the processing

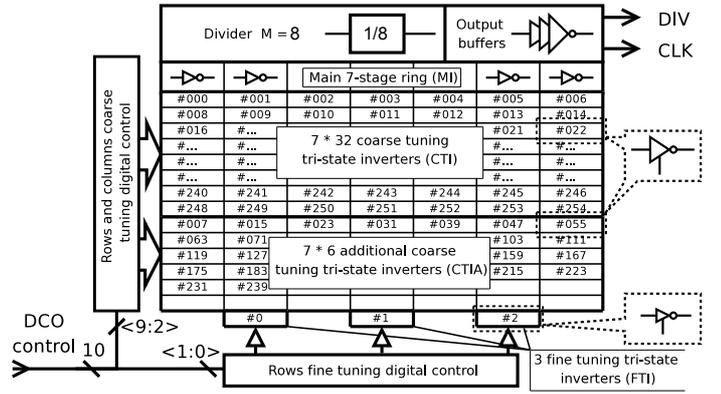


Fig. 6. Structure of DCO.

by the arithmetic block, the signed error value is in the range  $(-15, -1) \cup (1, 15)$  on 5 bits. In such a configuration, even for an error below the resolution of the TDC, its sign is detected, and a correct command can be generated for the DCO. The  $\tau$  being equal to 28 ps, the linear range of the PFD goes between  $\pm 420$  ps, which is roughly 1/5 of nominal period (2 ns).

#### B. DCO design

The summary of parameters of the implemented 1 GHz nominal (middle) frequency DCO is given in Fig. 6. The DCO's frequency resolution  $\Delta f$ , together with the clock frequency of the filter  $f_{clk\ flt}$ , determines the lower limit of the maximal phase error as  $2\pi\Delta f/f_{clk\ flt}$ , and the number of frequency step determines the operating frequency range. The implemented DCO structure includes a 7-stages ring oscillator and 266 tuning tri-state inverters connected in parallel to the stages of oscillator [8]. The oscillation frequency is controlled by the number of enabled tri-state inverters. The monotonicity of the frequency-code relation is the most critical DCO characteristic for the network stability; to avoid the impact of individual inverter delay mismatch, the frequency control algorithm is based on thermometer coding combined with binary coding for two LSBs. More details about this DCO implementation can be found in [4].

TABLE I  
MAIN CHARACTERISTICS OF THE DCO

Parameter	Value
DCO gain	800 kHz/LSB
Frequency range	571 MHz...1395 MHz
Phase noise	-86.12dBc/Hz @ 1MHz (10 bits)
Power consumption	15.678mW @ Fmax or $\sim 6$ mW/GHz

#### C. Filter

The filter architecture is given in Fig. 3. The filter's coefficients  $K_{prop}$  and  $K_{int}$  are calculated from the theoretical considerations involving the network stability (sec. II-B), but the main difficulties in the filter design concerns the timing constraints and the neutralisation of quantization effects.

1) *Timing*: An ADPLL is an auto-sampled system: the filter is sampled with the generated clock divided by 4. A comprehensive design approach assumes that the network is synchronized: the input events coming from the  $N$  neighbors of the given node come at close times (comparing to the divided clock period). In this case, the filter can be designed as a synchronous digital system, in which the input signal arrives at inputs with maximal delay of  $t_{err\ max}$  comparing to the clock event, where  $t_{err\ max}$  is the maximal phase error between neighboring oscillators.

The critical path in the digital part of a network node starts at the TDC register (Fig. 5) and ends at the output register of DCO encoder (Fig. 3, dotted lines). For the architecture we designed, this path is executed in 2.38 ns, i.e., below one clock period (4 ns).

2) *Quantization effects*: The filter receives integer values at the input, and must provide an integer value allowing to control the DCO. Fractional integral and proportional coefficients of the filter can be implemented if they are represented as  $K_{prop\ num}/2^{n_{prop\ den}}$  and  $K_{int\ num}/2^{n_{int\ den}}$  respectively (cf. Fig. 3). The integration path is implemented as a fixed-point accumulator, which outputs the rounded (integer) part of the accumulated value. The size  $n_{acc}$  of accumulator is  $n_{acc} = n_{int\ den} + n_{dco}$ , where  $n_{err}$  is the number of bit of the filter input,  $n_{dco}$  is the number of bit of the DCO input.

The proportional path corrects small errors when the network is in the locked synchronized state. For this reason, the value of the proportional coefficient can not be much less than 1, otherwise, after the integer divisions, small errors are rounded to zero and the proportional path is "deactivated", leading an instability of the overall network. This issue can be particularly critical when the bandwidth of the nodes has to be reduced, requiring small coefficients.

#### IV. VHDL SIMULATION RESULTS

This section presents the simulation results for a model written in VHDL, and parametrized so to have a behaviour close to that of the designed system. The initial frequency of the DCOs are randomly mismatched by 5%.

Upper 4 plots of the Fig. 7 present the behaviour of a 4x4 network, which starts in unidirectional mode, then switches to the bidirectional: all the phase errors converges to values in range  $\pm 2/-2$  (below 70 ps). To demonstrate the better immunity toward perturbations of the bidirectional mode, a perturbation is injected in the SCA5, by changing the initial frequency of its DCO by 3 % at  $t = 6.3\ \mu s$ . The phase error perturbation, observable on  $err_{5,6}$ , reduces as the distance from the perturbed node increases, and is nearly non-observable between SCA 11 and 15 ( $err_{11,15}$ ). The lower plot presents this error for a system with the same perturbation, but in which the bidirectional mode was not switched on: the perturbation is well observable. This prove that the bidirectional mode of coupling ensure better immunity to noise and perturbation.

#### V. CONCLUSIONS

The successful demonstration of an alternative solution for complex SOC synchronization is presented. The advantage

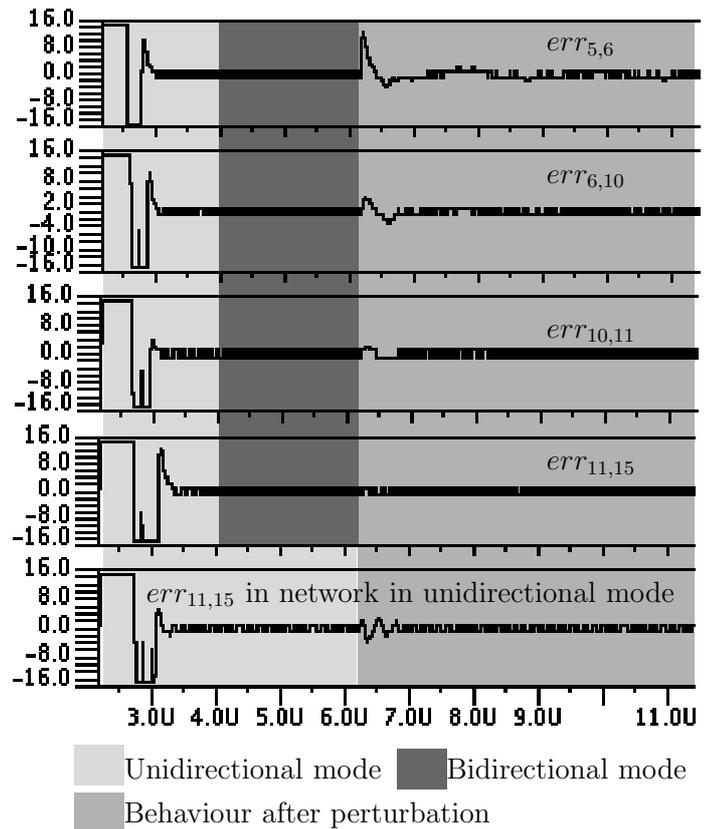


Fig. 7. Simulation results. The  $x$  axis represents the time in seconds.

of the proposed solution is its compatibility with the digital environment, and the possibility of complex and intelligent control over the clock generation by the main circuit. A silicon implementation of the proposed architecture is a subject of the ongoing work.

#### ACKNOWLEDGMENT

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