

## **LISTE CLASSEE DES PUBLICATIONS :**

(celles-ci ne doivent pas être jointes)

*Sauf erreur ou omission de ma part, environ 175 publications internationales (conférences et revues avec comités de lecture) dont 22 en revues.*

*Les revues sont signalées en caractères **gras et soulignés**.*

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*Bajot Yann, Mehrez Habib*

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**Microtechnologies for the New Millennium 2005: VLSI Circuits and Systems II, Sevilla, Spain, May 2005**

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pp. 275-278*

**[70]** “Data Path Optimization using Redundant Arithmetic and Pattern Matching “  
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*Parvez Husain, Marrakchi Zied, Farooq Umer, Mehrez Habib  
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**[76]** “Automatic Layout Generator of Domain Specific FPGA: “  
*Mrabet Hayder, Parvez Husain, Marrakchi Zied, Mehrez Habib  
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**[77]** “The Effect of LUT and Cluster Size on a Tree based FPGA Architecture “  
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**[83] “Comparison of Tree-Based and Mesh-Based Coarse-Grained FPGA Architectures”, Marrakchi Zied, Farooq Umer, Mrabet Hayder, Mehrez Habib, International Conference on Microelectronics (ICM'2009), Marrakech, Morocco, December 2009**

**[84] “FPGA Interconnect Topologies Exploration”, Marrakchi Zied, Mrabet Hayder, Farooq Umer, Mehrez Habib, International Journal on Reconfigurable Computing, Oct. 2009, vol. 2009, num. 2598, pp. 1-13, Hindawi Publishing Corporation**

**[85]"Placement and Routing Techniques to Improve Delay Balance of WDDL Netlist in MFPGA", Emna Amouri, Hayder Mrabet, Zied Marrakchi, Habib Mehrez, IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2009, Hammamet, Tunisia, December 2009.**

**[86]"Improving the Security of Dual Rail Logic in FPGA Using Controlled Placement and Routing", Emna Amouri, Hayder Mrabet, Zied Marrakchi, Habib Mehrez, 2009 International Conference on Reconfigurable Computing and FPGAs, Reconfig, Cancun, Quintana Roo, Mexico, pp.201-206**

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*Guitouni Zied, Chotin-Avot Roselyne, Machhout Mohsen, Mehrez Habib, Tourki Rached*

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*Amouri Emna, Marrakchi Zied, Mehrez Habib*

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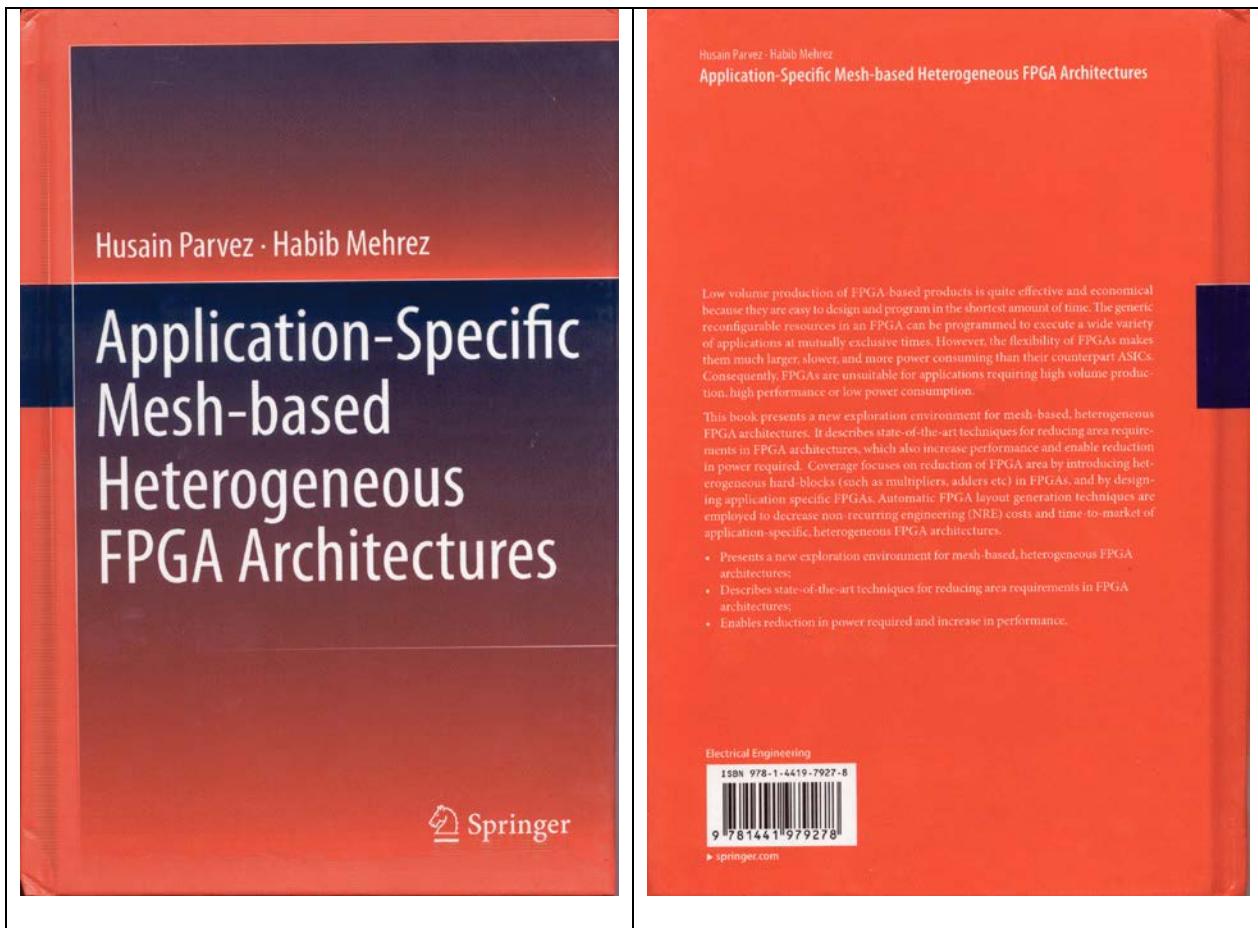
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- ***Ouvrages individuels et collectifs :***

**Ouvrage 1:**

*Application-Specific Mesh-based Heterogeneous FPGA Architectures  
Parvez Husain, Mehrez Habib  
Springer , December 2010, 1ère édition, 150 p*



Husain Parvez · Habib Mehrez  
**Application-Specific Mesh-based Heterogeneous FPGA Architectures**

Low volume production of FPGA-based products is quite effective and economical because they are easy to design and program in the shortest amount of time. The generic reconfigurable resources in an FPGA can be programmed to execute a wide variety of applications at mutually exclusive times. However, the flexibility of FPGAs makes them much larger, slower, and more power consuming than their counterpart ASICs. Consequently, FPGAs are unsuitable for applications requiring high volume production, high performance or low power consumption.

This book presents a new exploration environment for mesh-based, heterogeneous FPGA architectures. It describes state-of-the-art techniques for reducing area requirements in FPGA architectures, which also increase performance and enable reduction in power required. Coverage focuses on reduction of FPGA area by introducing heterogeneous hard-blocks (such as multipliers, adders etc) in FPGAs, and by designing application-specific FPGAs. Automatic FPGA layout generation techniques are employed to decrease non-recurring engineering (NRE) costs and time-to-market of application-specific, heterogeneous FPGA architectures.

- Presents a new exploration environment for mesh-based, heterogeneous FPGA architectures;
- Describes state-of-the-art techniques for reducing area requirements in FPGA architectures;
- Enables reduction in power required and increase in performance.

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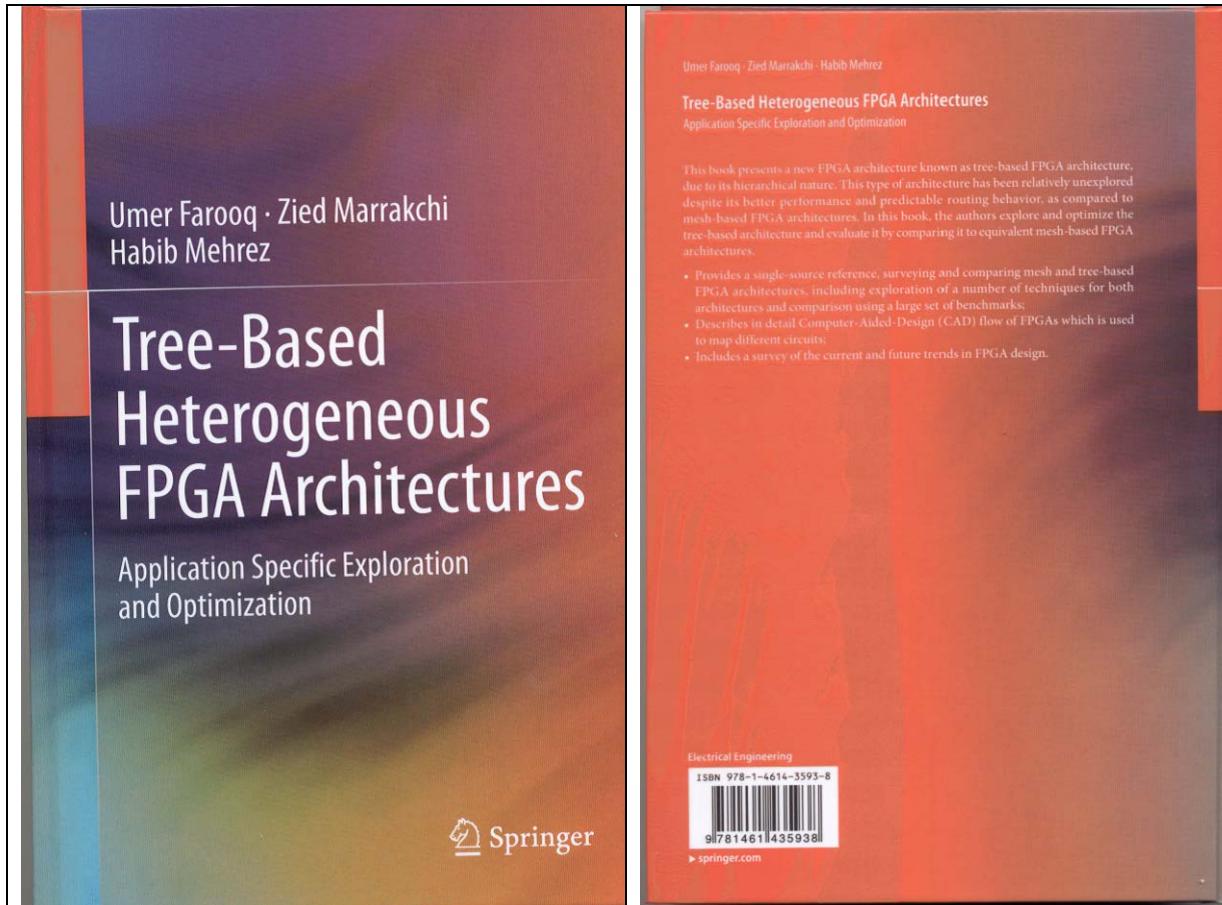


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**Ouvrage 2:**

Tree-based Heterogeneous FPGA Architectures  
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