T U N I S I A
P O L Y T E C H N I C
S C H O O L

Graduation Project Report

Option SISY

Band pass Sigma Delta modulators employing undersampling

Hosting laboratory : ASIM

Carried out by : KAMMOUN Abla
Supervised by : Mr ABOUSHADY Hassan
Mr BEILLEAU Nicolas

Academic year 2004/2005

Acknowledgements

I would like to express my sincere gratitude to my supervisors, Mr Hassan Aboushady and Mr Nicolas Beilleau, for their patience, valuable guidance throughout my graduation project internship.

Special thanks are also due to my colleagues at the laboratory for creating a pleasant working atmosphere, especially to Ramy Iskander and Ludovic Noury.

Résumé

Durant les dernières années, le développement de la téléphonie mobile a engendré un besoin pour des chaînes de réception radio-fréquences (RF) multi-standards et de très basse consommation. Pour atteindre ces objectifs, la conversion analogique numérique directe est plutôt utilisée. Elle consiste à amener la conversion analogique-numérique le plus près possible de l'antenne de réception. Par conséquent, on substituera la circuiterie analogique RF par une circuiterie numérique facilement programmable.

Cependant, la conversion directe présente l'inconvénient de nécessiter une fréquence d'échantillonnage assez élevée. Par exemple, pour les architectures classiques des convertisseurs $\Sigma\Delta$ passe bande, la fréquence d'échantillonnage est égale à quatre fois la fréquence centrale. Echantillonner à une telle fréquence complique davantage la partie numérique du récepteur RF. Pour palier à ces inconvénients, une architecture de modulateur $\Sigma\Delta$ temps continu basée sur le sous échantillonnage a été proposée.

Le but de ce projet est la conception au niveau système des modulateurs $\Sigma\Delta$ temps continu ayant des filtres LC et utilisant le sous échantillonnage.

Le premier chapitre présente une idée globale sur les modulateurs $\Sigma\Delta$. Ensuite, on expliquera dans le deuxième chapitre une méthode générale pour la conception des convertisseurs $\Sigma\Delta$ temps continu. Enfin, on se proposera dans le troisième chaptire d'appliquer cette méthode pour les convertisseurs $\Sigma\Delta$ sous échantillonnés.

Mots clés: Modulation $\Sigma\Delta$ passe bande , récepteurs RF , sous échantillonnage

Abstract

Recent years have shown an increasing interest to digitizing the input signal near to the front end of the antenna so as to push more signal processing functions into the digital domain. Direct digitization enables the production of flexible multi-standard RF receivers where channel selection and demodulation can become software programmable.

However, direct digitization is still difficult or almost impossible because of high sampling frequency requirement. For instance, for conventional bandpass $\Sigma\Delta$ converters, the sampling frequency is four times the center frequency. Sampling at such high frequencies requires expensive processes and increases the complexity and power consumption of the digital signal processing stage. Therefore, a new architecture of $\Sigma\Delta$ modulators based on undersampling techniques was proposed.

The objective of the project is to achieve the system level design of continuous time $\Sigma\Delta$ converters based on LC filters and employing undersampling.

The first chapter gives a brief overview of $\Sigma\Delta$ converters. After that, we present in the second chapter a general method for the system level design of $\Sigma\Delta$ modulators. And finally, we apply this method for LC filtered $\Sigma\Delta$ modulators using undersampling.

Key words: bandpass $\Sigma\Delta$ modulation, radio recievers, undersampling.

Contents

Introduction

1. RF receiver architectures

   Currently, the development trend of RF receivers is to increase their integration level and to minimze the number of discrete components. Several architectures have been proposed.

   (a) Superheterodyne receiver

   The superheterodyne receiver is the traditional receiver architecture and the one most often used. Figure 1 shows the main components of this kind of receiver.

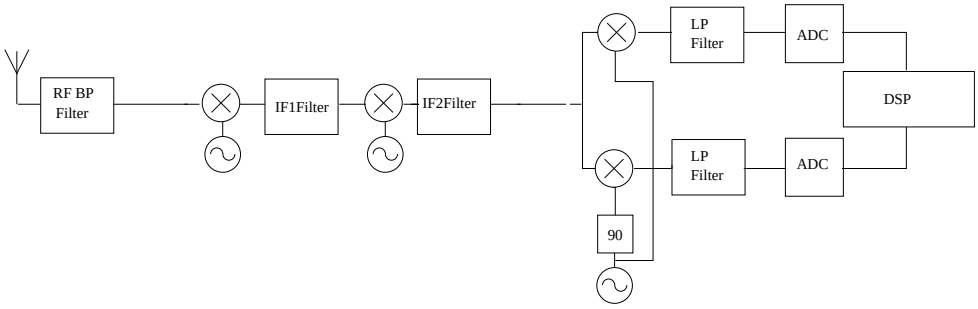

Figure 1: Superheterodyne receiver architecture

First, the RF band is selected, and the out of band signal are attenuated by the passive band selection filter, then the signal will be downconverted to two different intermediate frequencies.

The channel reception is finalized with an analog base band filter and an analog digital converter.

Including many blocks, this architecture has a high power consumption and a low integration level. Besides, as the analog quadrature demodulation is analog, the downconverted signal and its image do not have in general the same phase and amplitude, thus producing I/Q impairments.

(b) Direct conversion receiver

A direct conversion receiver is shown in Figure 2

Like the superhetrodyne receiver, analog components are needed in order to downconvert the input signal to an intermediate frequency.

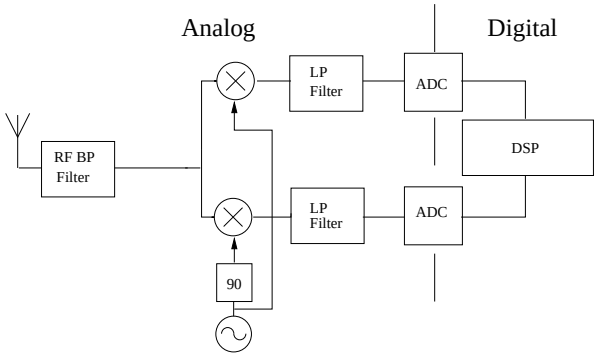

Figure 2: Direct conversion receiver architecture

Quadrature demodulation is also performed by analog circuits. The main advantage of this architecture over the previous one is the high level integration through the use of few number of elements. But the high DC offset induced by the RF mixer and the I/Q mismatch are the main inconvenients of this architecture.

2. RF bandpass $\Sigma\Delta$ architecture

   Another architecture is proposed in [1] (Fig 3). The RF band is first

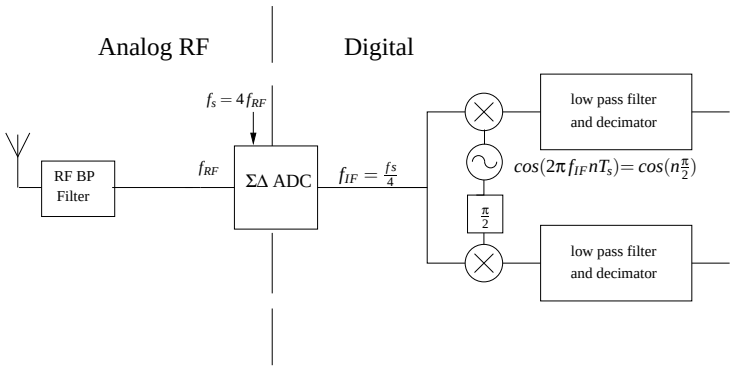

Figure 3: Proposed receiver architecture in [1]

selected and amplified by an analog RF band. After that the signal is directly digitized by a Σ Δ converter, which employs a sampling frequency of $4f_{RF}$.

As it is shown in Fig 3, quadrature demodulation could be easily performed digitally because the multiplying signal is a sequence of 0 and 1. Consequently, the mismatch of the I/Q paths is extremely attenuated.

Besides, this architecture contains few RF analog elements, thus having a better level of integration.

However, with 2.1 Ghz RF frequencies, the sampling rate at greater than

8 Ghz will likely cause critical design issues, severe jitter and loop delay problems. [2].

To overcome this problem, another architecture employing undersampling was proposed in [3] and [4].

The proposed architecture could be used for high frequencies because the rate of sampling is being made at a low level due to undersampling, allowing use of standard CMOS thechnology and reducing the complexity and power consumption of the digital part.

In this project, we focussed on the design of continuous time LC filtered $\Sigma\Delta$ modulators using undersampling. This report is divided as follows: we give in the first chapter a brief overview of $\Sigma\Delta$ modulators. After that we move on to present a general method for the system level design of continuous time $\Sigma\Delta$ modulators. And finally, we apply this method for LC filtered $\Sigma\Delta$ modulators using undersampling, and present the simulation results.

Chapter 1

$\Sigma\ \Delta$ modulators

Introduction

In order to transmit analog data, a discretization in time and in amplitude should be performed. According to Nyquist sampling theorem, time discretization does not entail any loss of information if the sampling frequency is more than the Nyquist rate (twice the bandwidth). However, the amplitude discretization implies some irreversible loss of information. Therefore, throughout the last decades, recent works have been conducted to produce ADCs with the least possible quantization noise. Nowadays, $\Sigma\Delta$ converters are the most qualified converters to meet this requirement. In this chapter, we explain with theoretical results the performance of $\Sigma\Delta$ converters compared to previous quantizers.

1.1 Conventional Analog to Digital Converters

1.1.1 Description of conventional converters

A conventional Analog to Digital Converter (ADC) is composed of a sampler and a quantizer, which is often modeled as an additive source of error.

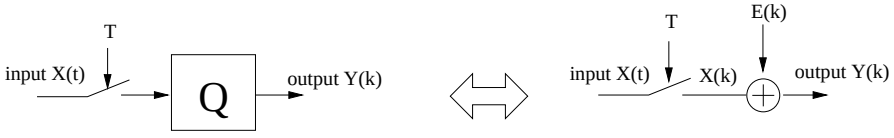

Figure 1.1: The diagram of a conventional Analog to Digital converter

According to Bennett, as it is shown in [5] the quantization noise can be assumed to be a a uniform white noise, under the following conditions:

1-the quantizer doesn't overload

2-the quantizer has a large number of levels

3-the distance between the levels is small

4-the probability distribution of pairs of input samples is given by a smooth probability density function.

The sampling rate of the conventional quantizer has to be more than $2f_m$, where f_m is the maximum frequency of the input signal.

The oversampling ratio is defined to be the ratio between the sampling frequency f_s and the minimum required sampling frequency $2f_m$

$$OSR = \frac{f_s}{2f_m}$$

Nyquist converters use an oversampling ratio that is approximately equal to 1.

1.1.2 Signal to Noise ratio

Assuming that the quantization noise is uniformly distributed and uncorrelated with the input signal (Fig 1.2), the variance of the noise is then equal to:

$$\sigma^2 = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} q^2 dq = \frac{\Delta^2}{12} \tag{1.1}$$

where Δ is the quantization step [6].

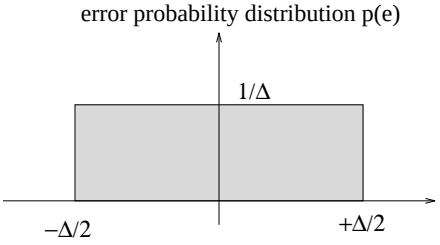

Figure 1.2: Noise distribution

The noise power spectrum density is then equal to:

$$E(f) = \frac{\sigma^2}{f_s} = \frac{\Delta^2}{12f_s} \tag{1.2}$$

where f_s is the sampling frequency. The power in the band of interest is then given by the next formula:

$$P_n = \int_{-f_m}^{f_m} E(f)df = \frac{\Delta^2}{12OSR} \tag{1.3}$$

where f_m denotes the maximum frequency of the signal and OSR the oversampling ratio.

$$OSR = \frac{f_s}{2f_m} \tag{1.4}$$

Therefore

$$P_n(db) = 10\log_{10}(\frac{\Delta^2}{12OSR})$$

Assuming that the input signal is sinusoidal with an amplitude equal to A, and that the quantizer has N bits, the expressions of Δ and the signal power are

$$\Delta = \frac{A}{2^{N-1}}$$

and

$$P_s = \frac{A^2}{2}$$

The signal to noise ratio is therefore equal to:

$$\begin{aligned} \text{SNR[db]} &= 10\log_{10}(12.2^{N-2}OSR) \\ \text{SNR[db]} &= 1.76 + 6.02N + 10\log_{10}(OSR) \end{aligned} \tag{1.5}$$

It results from 1.5, that the adding of one bit to the quantizer increases the SNR level by 6db, but increases the requirements for a more accurate quantizer circuits.

1.2 $\Sigma\Delta$ converters

1.2.1 Oversampling

Unlike Nyquist ADCs, $\Sigma\Delta$ modulators use a higher OSR, enabling the SNR improvement (equation(1.5)), while maintaining the same number of bits.

Furthermore, conventional converters are required to use an anti-aliasing filter with a sharp cutoff in order to eliminate all signal components with a frequency higher than the Nyquist rate.(Fig 1.3)

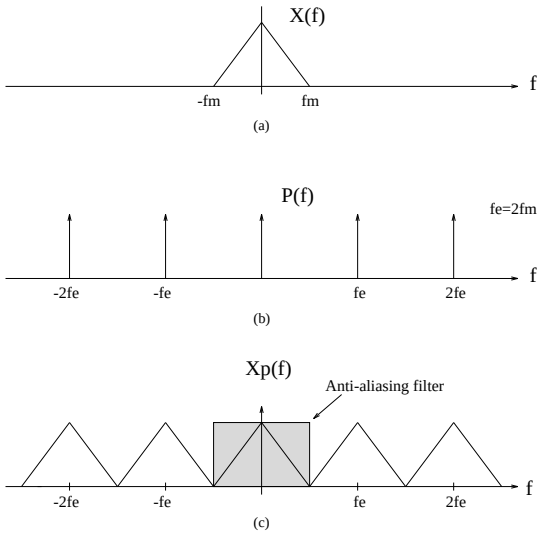

Figure 1.3: Sampling at the Nyquist frequency:(a)Signal input spectrum,(b)Spectrum of the sampling function (c)Spectrum of the sampled signal

On the other hand, in oversampled ADCs, the used anti-aliasing filter has in general a smooth slope, which reduces its design complexity a lot. (Fig 1.4)

However, after $\Sigma\Delta$ modulation, a decimation filter is needed in order to translate the spectrum of the output signal to the Nyquist frequency.

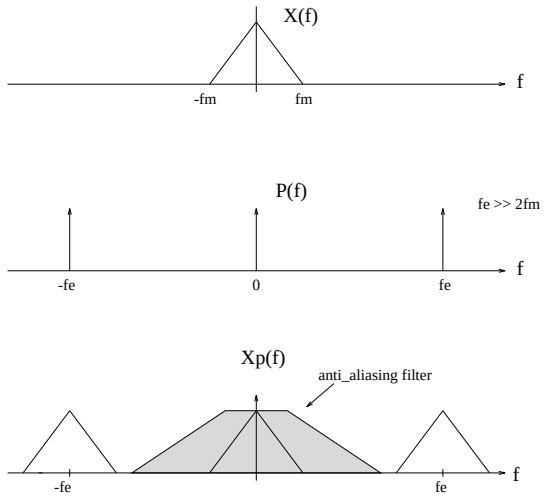

Figure 1.4: Oversampling: The anti-aliasing filter has a smooth slope

1.2.2 Discrete Time(DT) and continuous time $\Sigma\Delta$ modulators

Discrete time (DT) switched-capacitor technique has been preferred for the implementation of DT $\Sigma\Delta$ modulators. However, this technique suffers from a limiting sampling frequency, and therefore becomes no more suitable for high sampling frequency applications.

On the other hand, continuous modulators do not suffer from these limitations and have better performance than that of DT modulators.

1.2.2.1 Discrete time converters

Description Fig1.5 shows the general block diagram of a DT $\Sigma\Delta$ converter.

By using Schreier toolbox [7], the design in the system level of DT modulators is easier than CT modulators. Besides, discrete time converters have the advantage of being easier to simulate, but they are more sensitive to sampling errors.

Linear analysis This analysis consists in modeling the quantizer as an additive source of noise. Although the Bennet conditions are not always satisfied, this analysis still yields accurate results.

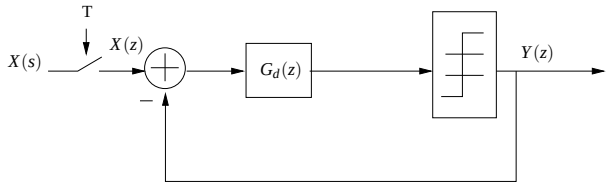

Figure 1.5: a Discrete time Σ Δ converter

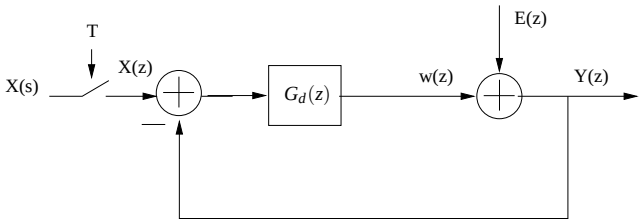

Figure 1.6: Linear model of discrete time ΣΔ converters

We have then,

$$Y(z) = X(z)\frac{G_d(z)}{1+G_d(z)} + \frac{E(z)}{1+G_d(z)} \tag{1.6}$$

The output of the modulator is expressed as the sum of two terms: one containing the input signal and the other containing the noise. We can see from equation(1.6) that the input signal is multiplied by $\frac{G_d}{1+G_d}$, whereas the noise signal is multiplied by $\frac{1}{1+G_d}$. These two terms are referred to be as the Signal Transfer Function (STF) and Noise Transfer Function (NTF) respectively.

We define also the loop gain of the discrete time ΣΔ converter as the opposite of the transfer function between the output of the modulator and the input of the quantizer, when the input is equal to zero (Fig1.5).

The loop gain is then given by $-\frac{Y(z)}{w(z)} = G_d(z)$, whereas the loop filter is equal to $G_d(z)$.

The order of the DT converter is given by the order of the denominator of its loop filter.

1.2.2.2 Continuous Time converters

Description Fig1.7 shows the general block diagram of a continuous time ΣΔ converter.

Continuous time converters are more suitable for higher sampling frequency and are less sensitive to sampling errors. However, they are more sensitive to the impairments of the feedback loop like clock jitter, mismatch in the DAC...

Linear Analysis As for discrete time modulators the loop gain is defined for continuous time (CT) ones by:

$$G_c(s) = H_c(s)H_{dac}(s)$$

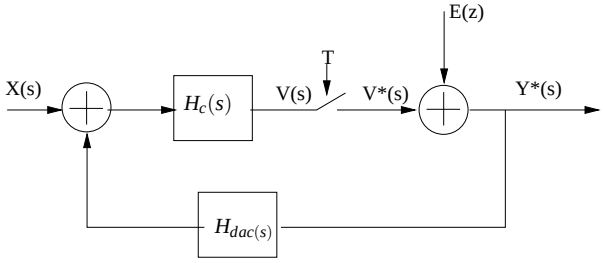

Figure 1.7: a Discrete time Σ Δ converter

. The loop filter is equal to $H_c(s)$.

The order of CT converter is also the order of the denominator of its loop filter.

The continuous time modulator output writes as follows:

$$Y(z) = \frac{Z[H_c X](z)}{1 + Z[H_c H_{dac}](z)} + \frac{E(z)}{1 + Z[H_c H_{dac}](z)}$$

where $Z[f]$ is the z-transform of f(s).

The NTF is given by:

$$NTF = \frac{1}{1 + (H_c Hdac)^*(s)}$$

As in general $Z[H_c X] \neq Z[H_c]Z[X]$, the STF cannot be represented in the Z domain. Another definition of the STF have been given in [8] using the Fourier representation:

$$STF(s) = \frac{H_c(s)}{1 + H_c(s)H_{dac}(s)}$$

1.2.3 Noise shaping

Called also the noise shaping encoders, ΣΔ modulators have the advantage of pushing the noise signal outside of the band of interest.(Fig1.8)

Due to the noise transfer function, the noise power of ΣΔ modulators is attenuated in the band of interest and amplified outside the signal band.

While the attenuation of the NTF in the band of interest is provided by its zeros, the out of band gain is controlled by its poles.

The design of ΣΔ modulators consists in choosing the poles and the zeros of the NTF so as to shape the noise power in a certain manner.

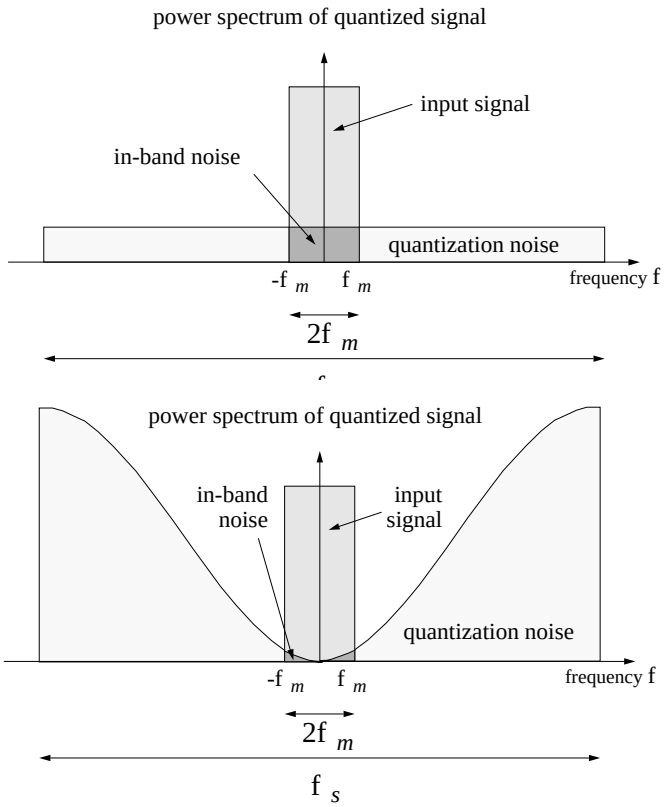

Figure 1.8: Power spectrum of the output of oversampled A/D conversion. (a)Conventional ADC (b) Σ Δ modulator

Conclusion

In this chapter, we have given a brief overview of ΣΔ modulators. We have particularly shown the basic principles of operation of discrete time and continuous time ΣΔ modulators and proved their performance over conventional converters.

Chapter 2

Method for the computation of continuous time $\Sigma\Delta$ modulators coefficients

Introduction

Recently, there has been a great trend for using continuous time (CT) Σ Δ modulators for their high speed and low power applications. However, as they are composed of discrete time continuous time circuits, their design is much more difficult than that of discrete time converters.

A general method based on the equivalence between a CT architecture and its DT counterparts has been presented in[9]. By using the Z modified transform, it has allowed the determination of CT coefficients for high order architectures, without passing by the time domain.

The architecture of the CT $\Sigma\Delta$ modulator does not always allow to find an equivalence with its DT counterpart, hence we have to introduce some compensation elements to achieve the equivalence. It is also in some cases impossible to perform computation and we need to introduce some changes in the structure of the DAC or the loop filter.

In this chapter, we will present a new method which determines, before doing computations, if it is possible to achieve the CT-DT transformation. When this is not possible our method allows to predict the changes that have to be introduced in the structure of the considered CT Σ Δ modulator.

2.1 Design of CT $\Sigma\Delta$ converters

The first step in the design of a CT $\Sigma\Delta$ modulator consists in determining the convenient coefficients for its architecture by making use of a Discrete Time Continuous Time (DT-CT) transformation. The objective of the DT-CT transformation is to find for a given topology of a continuous time modulator, the

convenient coefficients so that we have for the loop gain the same expression as its DT counterpart.

Previous work has usually determined the equivalence in the time domain by solving the following equation:

$$\mathbf{Z}^{-1}\{G_d(z)\} = \mathbf{L}^{-1}\{H(s)H_{dac}(s)\}$$

where

- $\mathbf{L}\{\cdot\}$ is the Laplace transform.
- $\mathbf{Z}\{\cdot\}$ is the Z transform. (cf appendixA)
- $G_d(z)$ is the DT loop gain.
- $H(s)H_{dac}(s)$ is the CT loop gain.

The complicated mathematics involved in the time domain convolutions make this method not adapted to design automation and has usually been for special cases. [10] [11], [12]

A more general transformation method using state space representation has been presented in [13]. But heavy use of matrix notations make the use of this transformation technique rather difficult. In [9], a systematic approach for DT-CT transformation that directly perform the equivalence in the Z domain by using the Z modified transform (see appendix A for the definition and proprieties of the Z modified transform) was proposed. This technique proposes to solve the next equation

$$\underbrace{G_c(z)}_{\text{CT loop gain}} = Z_m[H(s)H_{dac}(s)] \equiv \underbrace{G_d(z)}_{\text{DT loop gain}}$$

where $\mathbf{Z}_m\{\cdot\}$ denotes the Z modified transform. (see appendix A)

Having the same loop gain, the continuous time modulator will have the same NTF function as the discrete one, thus we predict that they have also the same behaviour in terms of SNR level and stability. (cf chpater 3)

However, for some cases, the DT-CT transformation is not always possible. Some compensation elements are sometimes needed to be added so as to perform the equivalence.

In this chapter, we present a method which helps predict, before doing any computations, if it is possible to perform the DT-CT transformation. This method is based on the decomposition into partial fractions of the DT and the CT loop gains. First the decomposition into partial fractions of the usual DT pass-band modulators is presented. After that, we will explain how to write the CT loop gain as a sum of partial fractions, and then we will deduce some necessary conditions for the DT-CT transformation.

We will also describe how to determine the value of compensation delays and their numbers without doing any calculations.

This method is validated with the CRFF modulators in this chapter and with the $\Sigma\Delta$ modulators based on LC resonators in the next one.

2.2 Loop gains expressions for usual DT passband converters

In this section, we give the loop gains for the usual DT passband converters. The decomposition into partial fractions of the DT loop gains over $\mathbb{R}$ and $\mathbb{C}$ is also presented.

Two types of passband modulators are considered:

1. DT ideal modulators
2. CRFF DT modulators

2.2.1 Low pass to band pass DT modulators or Ideal modulators

Low pass (LP) to band pass (BP) modulators are obtained by applying the transformation $z^{-1} \rightarrow z^{-2}$ to low pass converters. The resulting BP modulator maintains the same proprieties of the original LP, in terms of stability and signal to noise ratio level[14].

Here are two examples of DT ideal modulators:

2^{nd} order converter The diagram of a 2^{nd} order DT $\Sigma\Delta$ modulator is shown in Fig2.1.

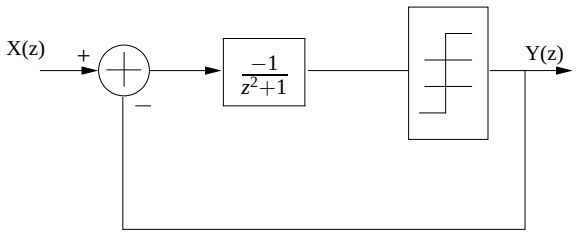

Figure 2.1: Diagram of the ideal 2^{nd} order bandpass DT $\Sigma\Delta$ modulator

The expression of the loop gain of this converter is :

$$H(z) = \frac{-1}{z^2+1}$$

The decomposition of the loop gain $H(z)$ into partial fractions over $\mathbb{C}$ is:

$$H(z) = \frac{I}{2(z-I)} - \frac{I}{2(z+I)}$$

4^{th} order converter The diagram of a 4^{th} order DT $\Sigma\Delta$ modulator is shown in Fig2.2. Its loop gain is

$$H(z) = \frac{-2z^2-1}{(z^2+1)^2}$$

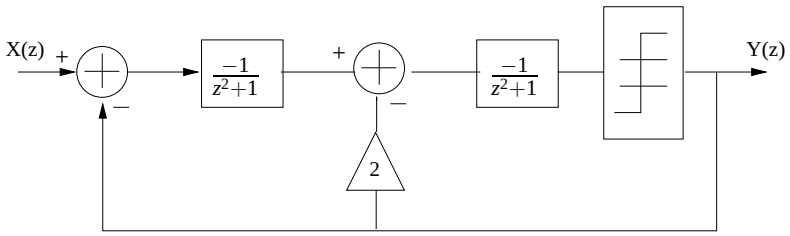

Figure 2.2: The diagram of the ideal 4^{th} order bandpass DT $\Sigma\Delta$ modulator

H(z) can be decomposed into partial fractions over $\mathbb{R}$

$$\begin{aligned} H(z) &= \frac{1-2(1+z^2)}{(z^2+1)^2} \\ &= \frac{1}{(z^2+1)^2} - \frac{2}{z^2+1} \end{aligned} \tag{2.1}$$

$$\tag{2.2}$$

The decomposition of the loop gain $H(z)$ into partial fractions over $\mathbb{C}$ is:

$$H(z) = \frac{3I}{4(z-I)} - \frac{1}{4(z+I)^2} - \frac{1}{4(z-I)^2} - \frac{3I}{4(z+I)}$$

2.2.2 DT CRFF architectures

Figure 2.3 shows the diagram of a 4^{th} order CRFF DT converter.

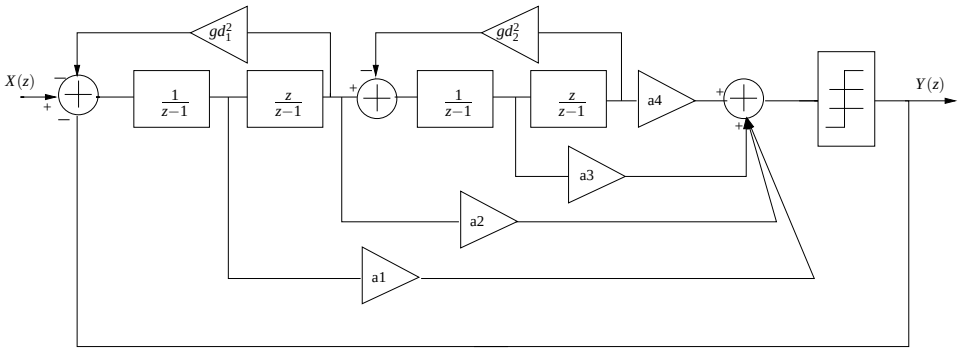

Figure 2.3: The diagram of a 4^{th} order CRFF converter

The expression of the loop gain for a n^{th} ordered CRFF architecture converter is: [8]

$$Gd(z) = \sum_{iodd}^{n} \frac{biz^{\frac{i-1}{2}}(z-1)}{\prod_{j=1}^{\frac{i+1}{2}} (z^2-(2-gdi^2)z+1)} + \sum_{ieven}^{n} \frac{biz^{\frac{i}{2}}}{\prod_{j=1}^{\frac{i}{2}} (z^2-(2-gdi^2)z+1)}$$

2.2.2.1 Partial fraction decomposition over $\mathbb{R}$

We note that Gd(z) can be written as the sum of partial fractions over $\mathbb{R}$:

$$Gd(z) = \sum_{i=1}^{i=\frac{n}{2}} \frac{\alpha_{2i} z + \alpha_{2i+1}}{z^2 - (2 - gdi^2)z + 1} \tag{2.3}$$

where n is the order of the DT $\Sigma\Delta$ modulator.

2.2.2.2 Partial fraction decomposition over $\mathbb{C}$

Gd(z) could also be put as the sum of partial fractions over $\mathbb{C}$. In fact let r_{2i} and r_{2i+1} denote the roots of the following equation: $z^2 - (2 - gdi^2)z + 1 = 0$

Assume that $\Delta = (2 - gdi^2)^2 - 4 < 0$ which is the case for the DT modulators proposed by Schreier, then

$$\begin{aligned} r_{2i} &= \frac{(2 - gdi^2) + I\sqrt{-\Delta}}{2} \\ r_{2i+1} &= \frac{(2 - gdi^2) - I\sqrt{-\Delta}}{2} \end{aligned} \tag{2.4}$$

We note that $|r_{2i}| = 1$ and $|r_{2i+1}| = 1$ and therefore there exists pr_{2i} and pr_{2i+1} opposites so that

$$\begin{aligned} r_{2i} &= e^{Ipr_{2i}} \\ r_{2i+1} &= e^{Ipr_{2i+1}} \end{aligned} \tag{2.5}$$

We have then,

$$\cos(pr_{2i}) = \tfrac{(2 - gd_i^2)}{2}$$

and

$$\cos(pr_{2i+1}) = \tfrac{(2 - gd_i^2)}{2}$$

and thus

$$pr_{2i} = \arccos(\frac{(2 - gd_i^2)}{2})$$

and

$$pr_{2i+1} = -\arccos(\frac{(2 - gd_i^2)}{2})$$

Gd(z) could be then decomposed into partial fractions as follows:

$$Gd(z) = \sum_{i=1}^{i=n} \frac{\beta_i}{z - e^{Ipr_i}} \tag{2.6}$$

where $\beta_i = \lim_{z \to e^{pr_i}} (z - e^{pr_i}) Gd(z)$.
We note also that $\beta_{2i} = \overline{\beta_{2i+1}}$

2.3 DT-CT transformation

As described in section2.1, the DT-CT transformation consists in finding the coefficient of a CT architecture from its discrete time counterpart so that they have the same loop gain. It has been shown in the previous section that the discrete time loop gain can write as a sum of partial fractions in $\mathbb{C}$. (Section 2.2.) The unicity of decomposition of a fraction into partial fractions over one field allows to identify CT loop gain partial fractions with that of the DT loop gain. The possibility of DT-CT transformation can then be verified. In this section the following issues will be addressed:

- describe a general model of a $\Sigma\Delta$ modulator inspired from the architectures which have been studied in this work.
- present a systematic method for the determination of a set of partial fractions containing those of the CT loop gain.
- find necessary conditions for the DT CT transformation.
- explain how to determine,without any computations, the compensation delays and their number.
- Validate the proposed method by the example of a CRFF architecture modulator.

2.3.1 A general model of a $\Sigma\Delta$ modulator

In order to make the proposed method valid for any kind of $\Sigma\Delta$ modulator we propose a general architecture that has been inspired from the ones that we have studied in this work.

In fact, in this report, we consider two kinds of CT $\Sigma\Delta$ modulators

- CRFF architecture
- LC based resonator architecture

The CT CRFF architecture provides the necessary required unknown coefficients in the feedforward path for the DT-CT transformation (Fig2.4), whereas the architecture of CT LC filtered modulators doesn't provide enough unknown parameters to achieve the DT-CT equivalence.

Previous work has been done for the design of LC filtered converters in [15], by adding two degrees of freedom at each input to the LC resonator. An example of a 2^{nd} and a 4^{th} order $\Sigma\Delta$ modulator have been also presented. (Fig2.5) But the DACs that have been used in this architecture are too sensitive to jitter noise.

A very recent work in [16] proposed a new architecture using Finite Impulse Response feedback DAC (FIR DAC) Fig2.6.

In order to make the proposed method valid for any type of $\Sigma\Delta$ modulator, we propose a general architecture that have been inspired from the previously described architectures.(CRFF and FIR DAC based $\Sigma\Delta$ modulators)

The general modulator that we consider is depicted in Fig2.7

H_{FIR1} and H_{FIR2} are two loop FIR filters. (Fig2.8)

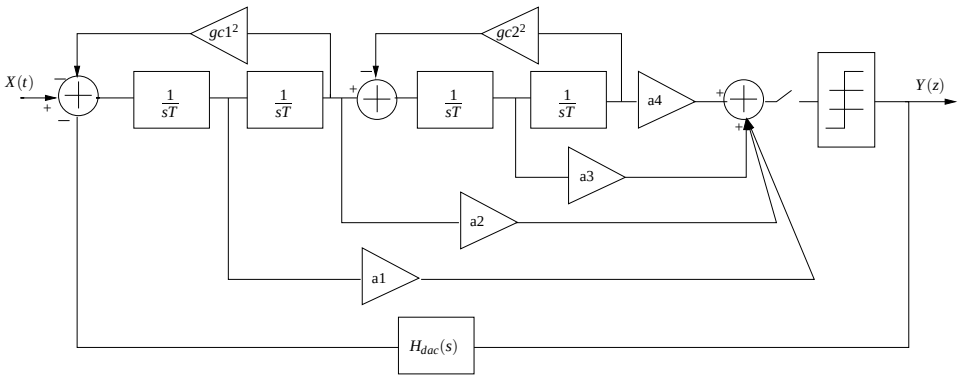

Figure 2.4: The diagram of a CT 4^{th} order CRFF converter

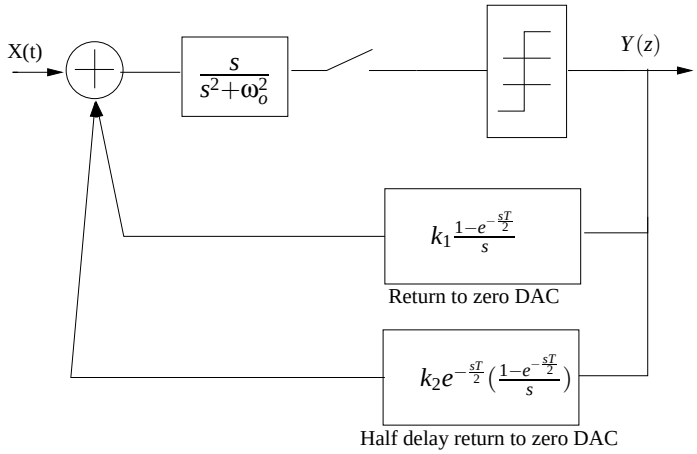

Figure 2.5: A second order multi-feedback $\Sigma\Delta$ modulator proposed in [15]

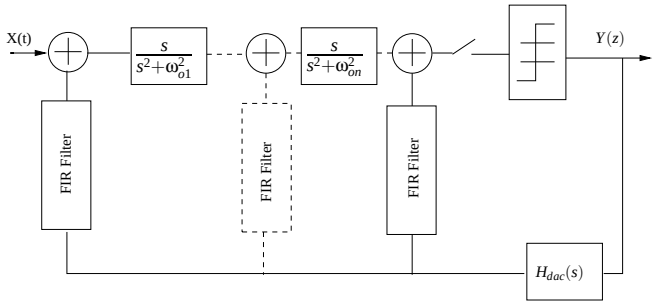

Figure 2.6: A $\Sigma\Delta$ modulator Based on LC filters and using a Finite Impulse Response Feedback DAC

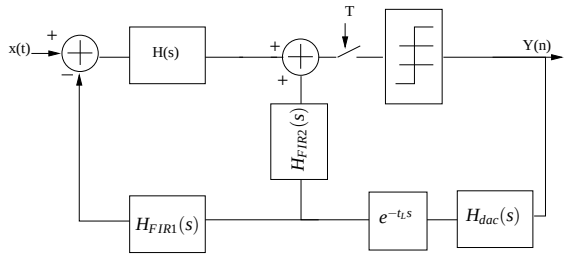

Figure 2.7: The general modulator diagram

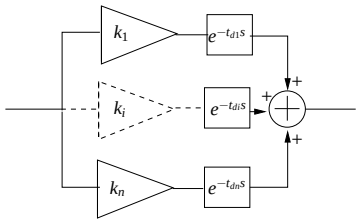

Figure 2.8: A FIR filter

The delays considered in the loop FIR filter can take any real values but for practical reasons these delays are chosen to be multiple integer of the sampling period.

2.3.2 Systematic method for the determination of a set of partial fractions containing those of the CT loop gain

2.3.2.1 Some definitions

Let us begin by defining the following terms:

feed back useful path we denote by *feedback useful path* any path that contains a delay in H_{FIR1}.

compensation path we denote also by *compensation path* any path that contains a delay in H_{FIR2}.

compensation coefficients the coefficients in H_{FIR2} are called *compensation coefficients*

useful coefficients the coefficients in H_{FIR1} or in H(s) are called *useful coefficients*

The unknown coefficients could be either in the feedforward path (the expression of H_{FIR1} is given in this case) or in the feedback paths. (H_{FIR1} is function of unknown coefficients)

2.3.2.2 Presentation of the method

In what follows, we assume that the delay loop t_L is null (see Fig 2.7) and that all the set of singularities of $H_{dac}(s)$ is included in $\{\frac{2\pi n}{T}\}$ $n \in \mathbb{Z}$. We assume also that the number of unknown coefficients is equal to the order of the DT modulator. The other case of a non null delay loop is considered in a next section and is also illustrated by an example in the next chapter. We propose now to:

- give the expression of the loop gain in terms of the loop FIR filters, the loop filter and the DAC.
- propose a systematic approach for the determination of a set of partial fractions containing those of the CT loop gain.

CT loop gain expression We recall that the CT loop gain expression is:

$$G_c(s) = H(s)H_{dac}(s)$$

$H_{dac}(s)$ can be derived as follows. For each output of the quantizer, which is an impulse function $y(t) = \pm\delta(t)$, the DAC steers a current equal to $y(t) \times g(t)$ during one sampling period.

We have then:

$$\begin{aligned} &h_{dac}(t) = g(t)(u(t) - u(t-T)) \text{ where } u(t)\text{is the Heaviside impulse} \\ &H_{dac}(s) = (1 - e^{sT})G(s) \end{aligned} \tag{2.7}$$

The Z modified transform of the loop gain is then equal to:

$$\begin{aligned} Z_m(H_{dac}H(s)) &= (1 - z^{-1})Z_m(G(s)H(s)H_{FIR1} - G(s)H_{FIR2}) \\ &= \underbrace{(1 - z^{-1})(Z_m(G(s)H(s)H_{FIR1})}_{\text{Useful transfer function}} - \underbrace{(1 - z^{-1})Z_m(G(s)H_{FIR2})}_{\text{compensation transfer function}} \end{aligned} \tag{2.8}$$

The loop gain expression is therefore a sum of two transfer functions, the first one is derived from the elements in the feedback useful path and is called useful transfer function whereas the other one is derived from the elements in the compensation path, and is called compensation transfer function.

Systematic approach for the determination of a set containing the partial fractions of the CT loop gain We recall that our target consists in determining the partial fractions of the CT loop gain, in order to identify them with that of the DT loop gain.

We recall also that in section 2.2, we have computed the partial fraction decomposition of the usual DT modulators. In the following we propose to give a systematic method for the determination of a set containing the partial fractions of the CT loop gain. This set is chosen as the union of the partial fractions of the useful transfer function and that of the compensation transfer function.

By comparing the elements of this set with the partial fractions of the DT modulator loop gain, we can deduce the possibility of DT-CT transformation. This is detailed in paragraph 2.3.2.3

Useful partial fractions Let maxdelay denote the maximum delay in the feedback useful path. Let M be

$$M = \left\lceil \frac{\text{maxdelay}}{T} \right\rceil \tag{2.9}$$

where $\lceil x \rceil$ is the smallest integer superior or equal to x.

Let p_i be the singularities of the loop filter. It is proved in Appendix B, that two cases should be taken:

1. There is at least one useful path where the signal is not delayed
   ($H_{FIR1} = a_1 + \sum a_i e^{-t_{di}s}$.)
   Then the partial fractions of the useful transfer function will be inside the set S_U:
   $$S_U = \left\{ \frac{1}{z^k}, \frac{1}{z - e^{Tp_i}}, ..., \frac{1}{(z - e^{Tp_i)^{mu_i}}} \; k \in [\![0, M]\!] \; i \in [\![1, n]\!] \right\}$$
   n is the order of the modulator which is also the number of singularities of the loop filter, and mu_i is the multiplicity of the pole p_i.
   If the poles of the loop filter are simple, then the expression of the useful transfer function is given by
   $$Z_U = \sum_{i=1}^{i=n} \frac{c_i}{z - e^{Tp_i}} + \sum_{i=0}^{i=M} \frac{d_i}{z^i}$$
2. All delays are different from zero
   ($H_{FIR1} = \sum a_i e^{-t_{di}s} \; t_{di} > 0$.)
   Then the partial fractions of the useful transfer function will be inside the set:
   $$S_U = \left\{ \frac{1}{z^k}, \frac{1}{z - e^{Tp_i}}, ..., \frac{1}{(z - e^{Tp_i)^{mu_i}}} \; k \in [\![1, M]\!] \; i \in [\![1, n]\!] \right\}$$
   If the poles of the loop filter are simple, then the expression of the useful transfer function is given by
   $$Z_U = \sum_{i=1}^{i=n} \frac{c_i}{z - e^{Tp_i}} + \sum_{i=1}^{i=M} \frac{d_i}{z^i}$$

We note that the partial fractions of the set S_U are of two kinds:

- Partial fraction derived from the singularities of the loop filter, and are given by $\frac{1}{(z - e^{Tp_i})^k}$
- extra partial fractions that are derived from the delays in the feedback loop and are given by $\frac{1}{z^k}$.

Compensation partial fractions Let t_{di} be the delays of H_{FIR2}. Let m_i be the integer satisfying $t_{di} \in](m_i - 1)T, m_i T]$ if t_{di} is non null and $m_i = 0$, otherwise.

It is proved in Appendix B that if all the compensation delays are non null, the partial fractions of the compensation transfer fraction are inside the set:

$$S_C = \{\frac{1}{z^{m_i}}\}$$

The compensation transfer function is given by:

$$Z_C = \sum_{i=1}^{i=nc} \frac{1}{z^{m_i}}$$

where n_c is the number of compensation elements. The following diagram illustrates how to determine the partial fraction decomposition of the useful transfer function and that of the compensation transfer function Fig 2.9.

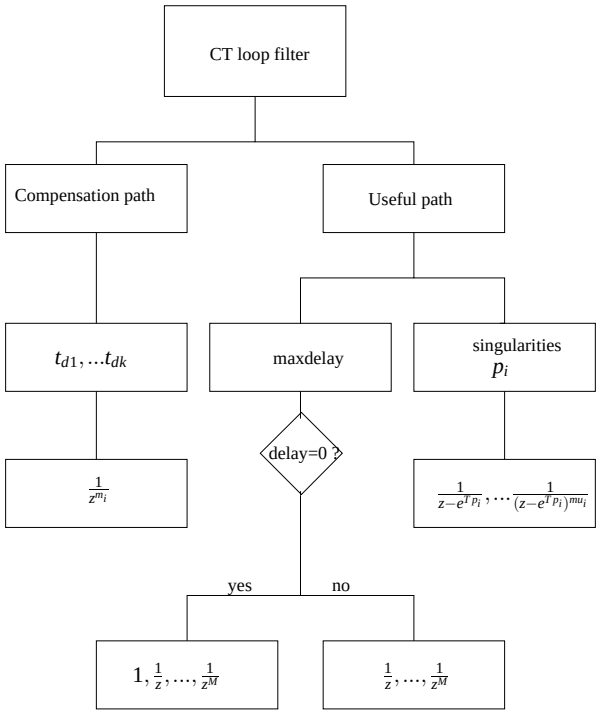

Figure 2.9: Systematic method for determination of CT loop filter partial fractions

2.3.2.3 Necessary Conditions for the DT-CT transformation

Let us summarize all what we have covered so far:

1. We have first determined the partial fractions of the DT loop gain. These partial fractions are given for the CRFF architecture by $\frac{1}{z-e^{Tpr_i}}$,

That means that:

$$Z_{DT} = \sum_{i=1}^{i=n} \frac{\beta_i}{z - e^{Ipr_i}}$$

2. Then we have determined the partial fractions of the CT loop gain, and particularly the set S_U, containing the partial fractions of the Useful transfer function and the set S_C, containing the partial fractions of the compensation transfer function. If the poles of the loop filter are simple then

$$Z_U = \sum_{i=1}^{i=n} \frac{c_i}{z - e^{ITp_i}} + \sum_{i=0}^{i=M} \frac{d_i}{z^i}$$

$c_0 = 0$ when all delays in the feedback path are different from zero. The compensation transfer function is given by:

$$Z_C = \sum_{i=1}^{i=n_c} \frac{g_i}{z^{m_i}}$$

Our target in this section is to present some necessary conditions that can be easily verified so as to conclude about the possibility of DT-CT transformation. Two cases are considered:

1. DT loop gain with simple poles: example CRFF DT architecture. From the previously given expressions of the CT and the DT loop gains, we can conclude that to achieve the equivalence between a CT loop gain with the DT loop gain having simple pole, we must verify the following statement: For every q_i pole of the DT loop gain, we have p_i simple pole of the CT loop gain verifying:

$$q_i = e^{Tp_i}$$

Example: With the CRFF architecture, for every pr_i, we have p_i simple pole of the CT loop gain verifying:

$$e^{Ipr_i} = e^{Tp_i}$$

2. DT loop gain with multiple poles: example ideal DT modulators.

To achieve the equivalence between a CT loop gain with a DT loop gain having multiple poles, we should verify the following statement: for each q_i pole with a multiplicity mu_i of the DT loop gain we should have p_i a multiple pole with a multiplicity of mu_i of the CT loop gain verifying:

$$e^{Tp_i} = q_i$$

These two conditions are necessary for the achievement of the DT-CT transformation. In the next chapter, we will explain by referring to these two conditions why it is impossible to achieve the DT-CT transformation in the case of real LC filtered $\Sigma\Delta$ modulator.

2.3.3 Adding compensation elements

2.3.3.1 Choice of the delay of the compensation path.

As seen previously, the DT-CT transformation consists in identifying the discrete time transfer function Z_{DT} with the continuous time one given by $Z_U - Z_C$. Seeing that Z_{DT} does not contain any element in the form $\frac{\alpha_i}{z^i}$ we need to choose the compensation delays so that to anneal the $\frac{d_i}{z^i}$ terms in the useful transfer function.

If the maximum of delay in the feedback path is in the interval $[kT, (k+1)T[$, and all delays in H_{FIR1} are different from zero, then we have to add k+1 compensation elements, so that the ith compensation coefficient is connected to a delay in the interval $](i-1)T, iT]$. $i \in \{1, ..., k+1\}$

For example if the maximum of delay is equal to $\frac{3}{2}$, we will have then extra partial fractions in the feedback path equal to $\frac{1}{z}$ $\frac{1}{z^2}$. To eliminate these partial fractions, we have to add in the compensation path two delays between $]0, T]$ and $]T, 2T]$.

This result will be illustrated by several examples in the next chapter.

2.3.3.2 Inefficient compensation elements

In some cases, compensation elements that are connected to some delays are without any interest. This is because the Z transform that corresponds to these delays with particular expressions for H_{FIR2} are equal to zero. We recall that the transfer function that corresponds to the compensation path is:

$$Z_C = (1 - z^{-1})\mathbf{Z}_m\{G(s)H_{FIR2}(s)\} \tag{2.10}$$

if $H_{FIR2} = \sum_{i=1}^{i=n_c} x_i e^{-t_{di}s}$, where x_i is a compensation coefficient that is connected to the delay t_{di}, then

$$Z_C = (1 - z^{-1}) \sum_{i=1}^{i=n_c} \mathbf{Z}_m\{G(s)x_i e^{-t_{di}s}\} \tag{2.11}$$

it is clear that if

$$(1 - z^{-1})\mathbf{Z}_m\{G(s)x_i e^{-t_{di}s}\} = 0$$

then the compensation coefficient is without any interest. This could entail some problems because in practice, at high frequencies the delays should be an integer multiple of the half of the sampling period. In the next chapter, we will give an example of a $\Sigma\Delta$ converter, where the DT-CT transformation is impossible by using such delays, and we will evaluate the loss in terms of SNR decrease if we change the delays for these practical reasons.

2.3.3.3 Maximum delay loop

Until now, we have taken the case of a null delay loop. However practical circuitry introduces unwanted delays in the feedback loop of the modulator [14]. These delays have to be taken into account in the determination of CT coefficients. [17] However in some cases these delays make DT CT transformation

impossible. In this paragraph we derive a necessary condition on the possibility of DT CT transformation, when a non null delay loop is considered.

Taking into consideration a non null delay loop t_L the delays of the compensation path becomes

$$t'_{di} = t_{di} + t_L$$

and the maxdelay of the useful feedback path becomes

$$\text{maxdelay}' = \text{maxdelay} + t_L$$

which corresponds to $M' = \frac{\text{maxdelay}'}{T}$

and the m_i becomes $m'_i = \left\lceil \frac{t_{di}+t_L}{T} \right\rceil$ The expression of Z_C is then

$$Z_C = \sum_{i=1}^{i=n_c} \frac{1}{z^{m'_i}} \tag{2.12}$$

For a CRFF architecture Z_U becomes

$$Z_U = \sum_{i=1}^{i=n} \frac{c_i}{z - e^{Tp_i}} + \sum_{i=0}^{i=M'} \frac{d_i}{z^i} \tag{2.13}$$

It is obvious that if $m'_1 > \min\{i \geq 0 | d_i \neq 0\}$ then the DT-CT transformation is impossible to perform.

Figure 2.10, illustrates the evolution of coefficients d_1, d_2 and d_3 (corresponding to the partial fractions $\frac{1}{z}$, $\frac{1}{z^2}$ and $\frac{1}{z^3}$) with the delay loop for a 4^{th} order CRFF architecture modulator.

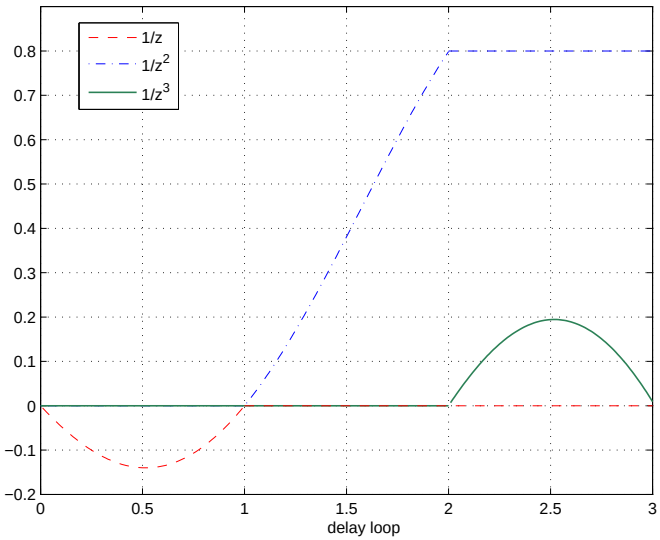

Figure 2.10: Variation of partial fractions with delays

We note that, in this case we can achieve a delay $\in [T, 2T]$ as the partial fraction on $\frac{1}{z}$ is not produced for such delays. But for a delay loop superior between $]2T, 3T]$ DT-CT transformation is impossible to achieve.

2.3.4 Validation of the method for CRFF architecture modulators

In the following part, we will apply the techniques that have been covered above on the CRFF architecture modulators (Fig2.11).

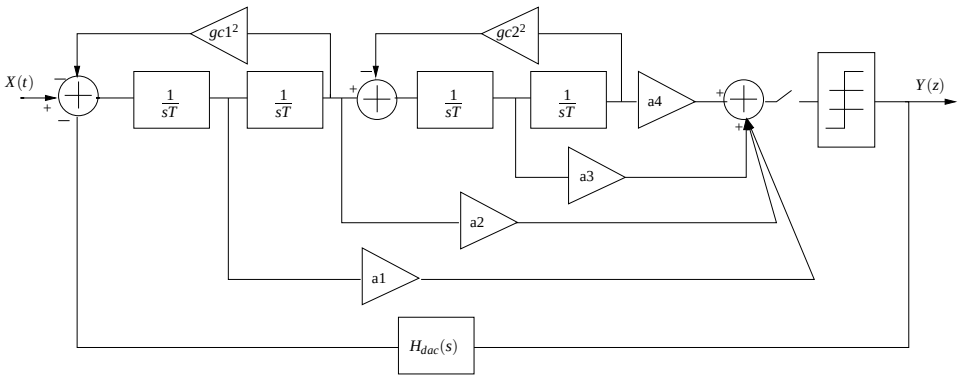

Figure 2.11: CT 4^{th}CRFF architecture converter

In this case, the expression of the loop filter is:

$$H(s) = \sum_{iodd}^{n} \frac{a_i Ts}{\prod_{j=1}^{\frac{i+1}{2}}((Ts)^2 + gci^2)} + \sum_{ieven}^{n} \frac{a_i}{\prod_{j=1}^{\frac{i}{2}}(Ts)^2 + gci^2)}$$

The Conventional DAC with a delay t_d between $]0, T]$ is considered [9]

$$H_{dac} = \frac{e^{-t_d s} - e^{-(t_d+T)s}}{s}$$

1. Necessary conditions for the DT-CT transformation

   The poles of H(s) are $\pm Ig_{ci}$. To make the equivalence between the CT CRFF and the DT CRFF architectures, we need:

   $$\{e^{Ipr_i}\} \subseteq \{e^{\pm Igc_i}\}$$

   By choosing

   $$\begin{aligned} gc_i &= \pm pr_i + 2\pi k \\ gc_i &= \pm \arccos(\frac{1 - gd_i^2}{2}) + 2\pi k \end{aligned} \tag{2.14}$$

   where k is an integer, we can satisfy the necessary condition.

2. Compensation coefficients

   As we have a delay in the feedback path between $]0, T]$, we predict that a compensation element may be needed.

2.4 Conclusion

In the chapter above, we have explained a systematic method for the DT-CT transformation. Based on the partial fraction decomposition of the DT and the CT loop gains, the proposed method derives necessary conditions for the DT-CT transformation. It also predict the required delays and their number as well. As we will see in the next chapter, this fact helps the automation of the design of $\Sigma\Delta$ modulators.

Chapter 3

Bandpass Σ Δ modulators with undersampling

Introduction

In this part of the report, we will see that the same method explained in the previous chapter can be applied to CT $\Sigma\Delta$ modulators employing undersampling.

First, we start from the example of a 2^{nd} order converter given in [4]. After that, we validate the previous method for CRFF architecture modulators using undersampling. Then, three kinds of approaches for the design of LC filtered $\Sigma\Delta$ modulators are detailed. And finally we present a Matlab graphic interface for the automatic determination of feedback coefficients.

3.1 Example of a LC Σ Δ modulator employing undersampling

3.1.1 Design of LC filtered modulator employing undersampling

In [4], a 2^{nd} order LC BP $\Sigma\Delta$ modulator for the digitization of a signal at the intermediate frequency of 195 MHz with a 300 KHz bandwidth have been presented. Referring to [4], the general block of a Σ Δ converter using undersampling is depicted in fig 3.1.

As it is explained in [4], in this design there is: (Fig3.1)

- oversampling with respect to signal bandwidth to provide the needed SNR.
- undersampling with respect to the f_{IF} signal which enables sampling at a frequency much lower than the f_{IF} signal.

The input signal at f_{IF} is undersampled at a frequency of f_s. Hence, many replicas of the input signal spectrum are created in the spectrum of the output signal of the modulator: at $(\pm f_{IF} \pm k f_s)$, where $k \in \mathbb{N}$. The only replica that is useful for the feedback is the one at f_{IF} frequency. These replicas will be

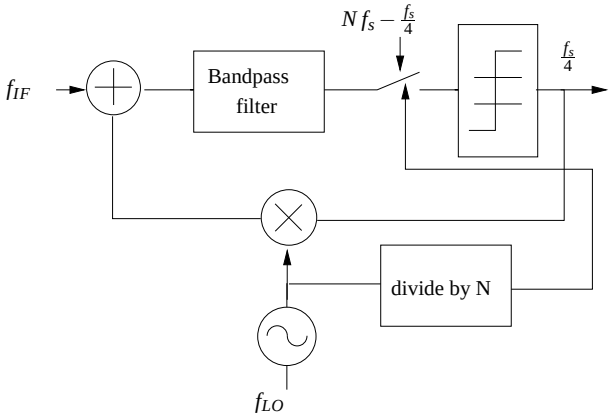

Figure 3.1: Block diagram of the BP $\Sigma\Delta$ modulator employing undersampling considered in [4]

severely attenuated by the conventional DAC which behaves as a low pass filter Fig3.2.

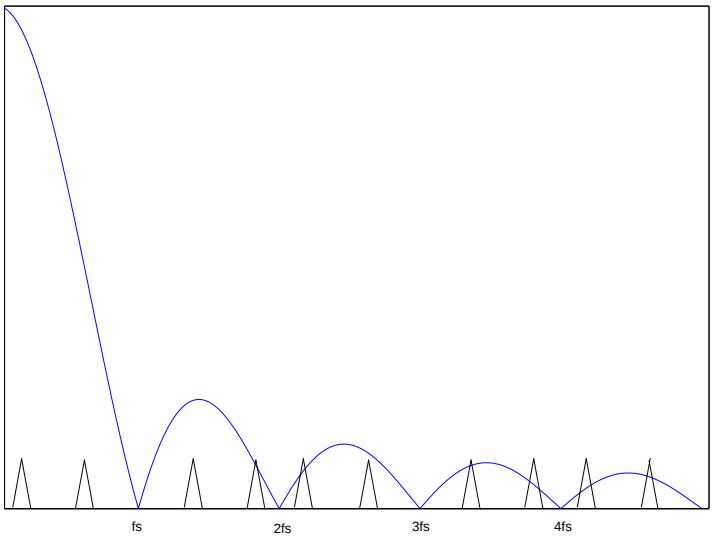

Figure 3.2: Attenuation of high frequency replicas by the NRZ DAC

The solution given in [4] consists in translating the output replicas which are located at $[-\frac{f_s}{2}, \frac{f_s}{2}]$ to the f_{IF} frequency by using a mixer.

In the proposed design (Fig3.1), the relation between f_{IF} and f_s is set up so that the f_{IF} is converted down to $\frac{f_s}{4}$. That is:

$$f_s = \frac{f_{IF}}{N - 0.25}$$

where N is the undersampling ratio. Therefore the modulating frequency of the mixer should be equal to

$$f_{LO} = Nf_s$$

so that the signal frequency out of the mixer is exactly equal to f_{IF}.

3.1.2 Design of a 2^{nd} order CT $\Sigma\Delta$ modulator

Figure 3.3 shows the example of a 2^{nd} order $\Sigma\Delta$ modulator which is given in [4], where A is a parameter that has to be determined so as to have the equivalence with the loop gain of the discrete time 2^{nd} order $\Sigma\Delta$ modulator, and $w2 = w_o^2$.(w_o is the resonance pulsation of the LC filter.)

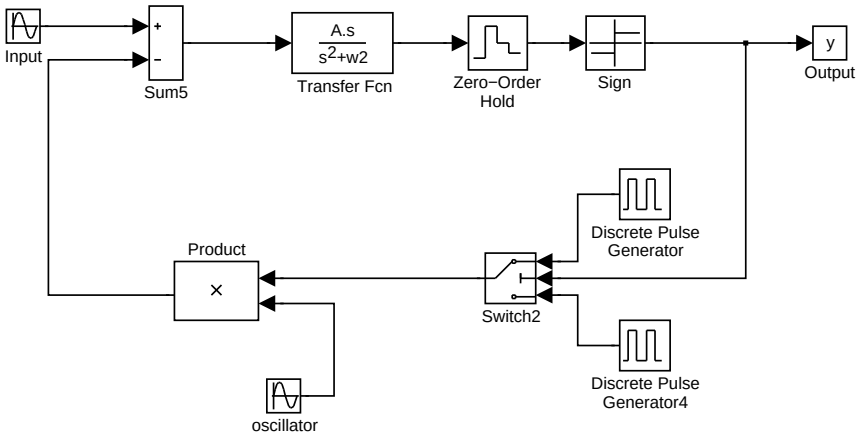

Figure 3.3: A 2^{nd} order BP $\Sigma\Delta$ modulator based on a LC resonator

However, it is proved in [4] that this equivalence can be performed approximately only if the local oscillator signal is equal to $sin(2\pi f_{LO}t + \frac{\pi}{4})$. In fact, if the local oscillator signal is equal to $sin(2\pi f_{LO}t + \theta)$, the Z transform of CT loop gain transfer function is:

$$Z_{CT} = g_t \frac{k_1 z^{-1} - k_2 z^{-2}}{1 + z^{-2}}$$

where

$$g_t = \frac{A f_{LO}}{2\pi(f_{LO}^2 - f_o^2)},$$

$k_1 = -\cos(\theta) + c\sin(\theta)$ $k_2 = \cos(\theta) + c\sin(\theta)$ and $c = \frac{f_o}{f_{LO}}$

If $\theta = \frac{\pi}{4}$ then, k_1 is small with respect to k_2, and therefore we can determine the parameter A that achieves the equivalence with the discrete time loop gain

$$Z_{DT} = \frac{-1}{1 + z^2}$$

For an input frequency equal to 195 MHz and an undersampling ratio of 10, it is proved that A should be equal to 1.5.

The CT loop gain has been computed by returning to the time domain, a method that doesn't allow the prediction of a possible equivalence between DT and CT loop nor the automation of the design of $\Sigma\Delta$ modulators.

3.2 Proposed model for $\Sigma\Delta$ modulators employing undersampling

The same model given in [4] has been adopted but with a slight difference that the mixer has been substituted by a FIR sine shaped DAC, which behaves as passband filter at f_{IF} (Fig3.4). In fact, it is shown in [18] that such a DAC is less sensitive to jitter noise and allow the power and noise budget savings by eliminating the need for mixers.

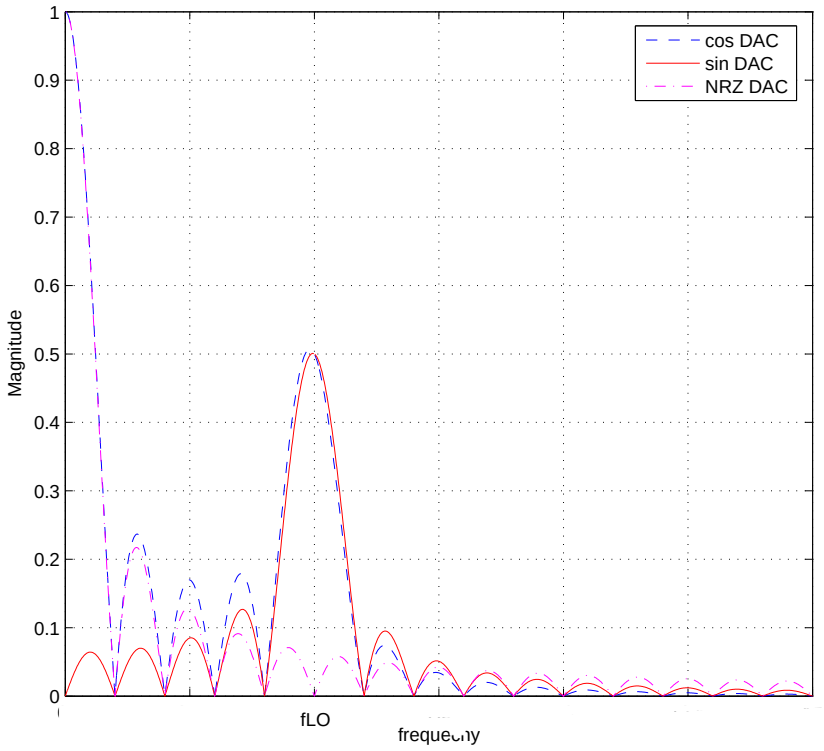

Figure 3.4: A 2^{nd} order BP $\Sigma\Delta$ modulator based on a LC resonator

In the following, two kinds of FIR sine shaped DAC's are considered:

1. A sinusoidal DAC

   The impulse response of a sinusoidal DAC is:

   $$h(t) = sin(w_{LO}t)(u(t) - u(t-T))$$

   Thus,

   $$H_{dac} = \frac{w_{lo}}{s^2 + w_{lo}^2} \tag{3.1}$$

2. A cosinusoidal DAC

   The impulse response of a cosinusoidal DAC is:[19]

$$h(t) = \cos(w_{LO}t)(u(t) - u(t-T))$$

   Thus,

$$H_{dac} = \frac{w_{lo}^2}{s(s^2 + w_{lo}^2)} \tag{3.2}$$

where $w_{LO} = 2\pi f_{LO} = \frac{2\pi N}{T}$ and N is the undersampling ratio. Figure 3.4 shows the impulse response magnitude for these two DAC's and the NRZ DAC.

Both the sinusoidal DAC and the cosinusoidal DAC impulses have a high gain at f_{IF} compared to the NRZ DAC impulse.

The cosinusoidal DAC has also a high gain at DC frequencies but these components will be removed by the loop filter.

Moreover, we note that unlike the cosinusoidal DAC, the sinusoidal one is inadequate for low pass ADC as it cuts off low frequencies.

And finally, the cosinusoidal DAC is less sensitive to jitter because its time domain response has a zero slope at sampling instants, whereas it is equal to $2\pi f_{LO}$ for the sinusoidal DAC [20].

3.3 Design of CRFF BP $\Sigma\Delta$ modulators employing undersampling

3.3.1 Determination of the resonators coefficients(g_{ci}^2)

For the design of CRFF architectures, we have applied the same method that we have explained in the previous chapter, by referring to DT CRFF $\Sigma\Delta$ modulators calculated with Schreier Toolbox. [7]

The loop gain of a CRFF architecture with a sine shaped DAC is

$$G_c(s) = H_{dac}H_s$$

We recall that the singularities of H_s are: $\{\pm Igc_i\}$.

From Equations (3.1) and (3.2), we deduce that the singularities of the two DAC's are inside the set $\{0, \frac{2\pi N}{T}, \frac{-2\pi N}{T}\}$. The suppositions that we have mentioned in the previous chapter are then verified. Having the following relation on g_{ci}

$$g_{ci} = \delta \arccos(\frac{1 - gd_i^2}{2}) + 2\pi k \tag{3.3}$$

the DT CT transformation is possible. where $\delta = \pm 1$ and k is an integer. Many values for k allow the DT CT equivalence, however it must be chosen so that the loop filter has the maximum amplification at the input frequency.

We recall that for passband CRFF architecture, the loop filter has the following expression:

$$H(s) = \sum_{i\text{odd}}^{n} \frac{a_i Ts}{\prod_{j=1}^{\frac{i+1}{2}}((Ts)^2 + gci^2)} + \sum_{i\text{even}}^{n} \frac{a_i}{\prod_{j=1}^{\frac{i}{2}}(Ts)^2 + gci^2)}$$

where T is the sampling period. Therefore, the decomposition into partial fractions of H(s) gives:

$$H(s) = \sum_{i\text{odd}}^{n} \frac{\alpha_i a_i Ts}{(Ts)^2 + gci^2} + \sum_{i\text{even}}^{n} \frac{\alpha_i a_i}{(Ts)^2 + gci^2} \tag{3.4}$$

where α_i are real numbers.

We note from equation (3.4), that H(s) is a sum of passband filters whose resonance frequency is at $\frac{g_{ci}}{2\pi T}$. If we substitute k with 0 in Equation (3.3), and δ with 1 we will get,

$$g_{ci} = \arccos(\frac{1 - gd_i^2}{2}) \simeq \frac{\pi}{2}$$

The resonance frequency is then equal to $\frac{1}{4T}$ thus the input frequency $f_{IF} = \frac{N}{T} - \frac{1}{4T}$ is attenuated by the loop filter.

However, when choosing

$$g_{ci} = -\arccos(\frac{1 - gd_i^2}{2}) + 2\pi N \simeq -\frac{\pi}{2} + 2\pi N$$

the resonance frequency is then equal to $\frac{N}{T} - \frac{1}{4T}$, which corresponds exactly to the input frequency.

For high rate of undersampling, the coefficient g_{ci}^2 is so high that it is not easily feasible. For example, for an undersampling rate of 10, the value of this coefficient is approximately equal to: $(-\frac{\pi}{2} + 2\pi 10)^2 = 3752.9$.

To overcome this problem, we have chosen to make a slight change to the structure of the loop filter, by multiplying all integrators by the same coefficient x.

The expression of H(s) become:

$$H(s) = \sum_{i\text{odd}}^{n} \frac{a_i Ts}{\prod_{j=1}^{\frac{i+1}{2}}((xTs)^2 + gci^2)} + \sum_{ieven}^{n} \frac{a_i}{\prod_{j=1}^{\frac{i}{2}}(xTs)^2 + gci^2)}$$

Therefore, H(s) is a sum of passband filters whose resonance frequency is at $\frac{g_{ci}}{2\pi xT}$.

For $x = \frac{1}{4N-1}$ $g_{ci} = -\arccos(\frac{1-gd_i^2}{2})$, the resonance frequency is of $\frac{N-0.25}{T}$, which corresponds exactly to the input frequency.

For N=10, the value of x is $\frac{1}{39}$, whereas that of gc_i^2 is approximately equal to 2.46 (which is a reasonable value). The gain of g_{ci}^2 is the same for any sampling ratio, while the gain x decreases as N goes up. Therefore, it may be hard for high ratio of undersampling to design the gain x. Therefore, CRFF architectures are inadequate for high sampling ratios.

3.3.2 Determination of the feedforward coefficients

As described in the previous chapter, the Z transform of the CT loop gain is decomposed into partial fractions which are identified with the partial fractions of the DT loop gain.

For example, for the 4^{th} order CRFF architecture modulator with a sine shaped DAC and an undersampling rate of 10, we have found the following feedforward coefficients :

- Cosinusoidal DAC

a1	a2	a3	a4
-.0242	-.0366	-.000364	.000487

- Sinusoidal DAC

a1	a2	a3	a4
.0238	-.0390	-.0003185	-.00058765

3.3.3 Results and simulation

Although the equivalence between the CT and the DT loop gains is achieved for the feedforward coefficients, the PSD curves shows several peaks close to the input frequency, degrading the performance of the CT modulator Fig 3.5

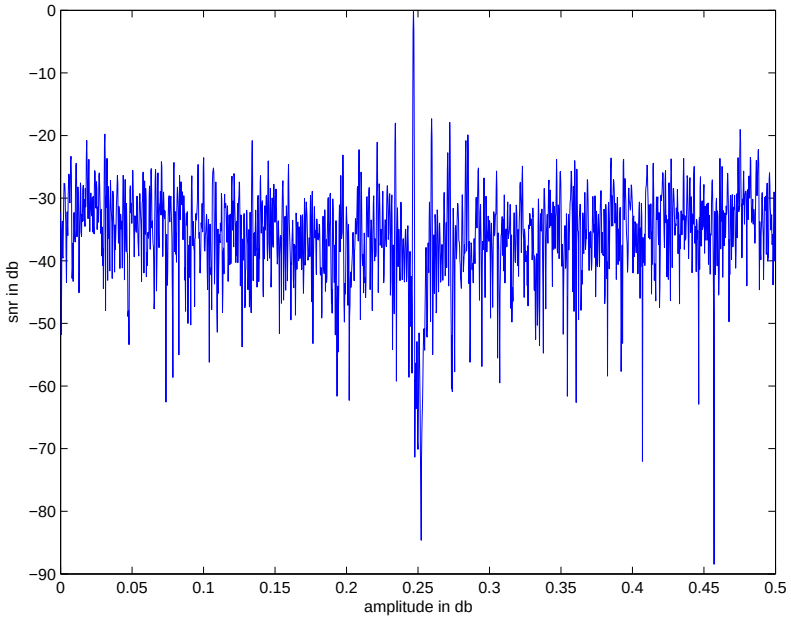

Figure 3.5: PSD curve of a 4^{th} order CRFF architecture before STF adjustment

3.3.3.1 Identification and analysis of the problem

In fact, having the same loop gain for the DT and the CT modulator is not sufficient to ensure the equivalence. An other condition is also necessary: the STF must be approximately equal to 1 at the input frequency.

We recall that the expression of the STF for a CT modulator is:

$$STF(s) = \frac{H(s)}{1 + H_{dac}(s)H(s)}$$

As H is a high gain filter at f_{IF},

$$STF(s)_{s=2\pi I f_{IF}} \approx \frac{1}{H_{dac}(f_{IF})} \tag{3.5}$$

3.3.3.2 Proposed solution

It is obvious that the adjustment of the value of the STF at the input frequency must maintain the equivalence between the CT and the DT loop gains. We note that if we multiply the returning signal by an adjustment coefficient K Fig3.6 and by its inverse in the feedforward path then the expression of the CT loop gains will remain unaltered. However, this will affect the expression of the STF.

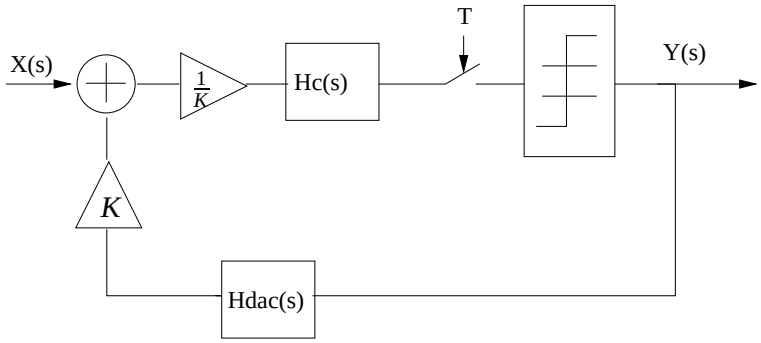

Figure 3.6: STF adjustment

In fact in this case the expression of the STF is:

$$STF(s) = \frac{H(s)}{(1 + H_{dac}(s)H(s))K}$$

Therefore

$$STF(f_{IF}) \simeq \frac{1}{KH_{dac}(f_{IF})} \tag{3.6}$$

If we choose K=$\frac{1}{H_{dac}(f_{IF})}$ then we will meet the STF requirement while maintaining the equivalence between the DT and the CT loop gains.

To illustrate (3.6), we have determined by simulation the amplitude of the STF at the input frequency for different adjustment coefficients.

Figure 3.7 shows two regions:

- The first region ranges below a value of 1 of the adjustment feedback coefficient K. The evolution of the amplitude of the STF at f_{IF} in this region doesn't match Equation (3.6)
- The second region corresponds to a value of adjustment feedback coefficient superior to 1. We note that the variation of the STF amplitude at f_{IF} fits perfectly well with equation (3.6)

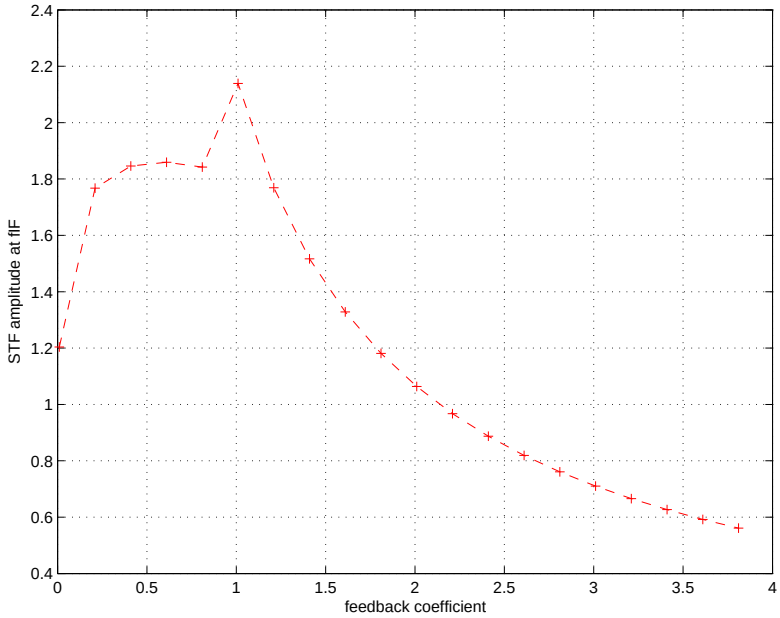

Figure 3.7: STF evolution with the feedback coefficient for a 4^{th} order CRFF architecture converter

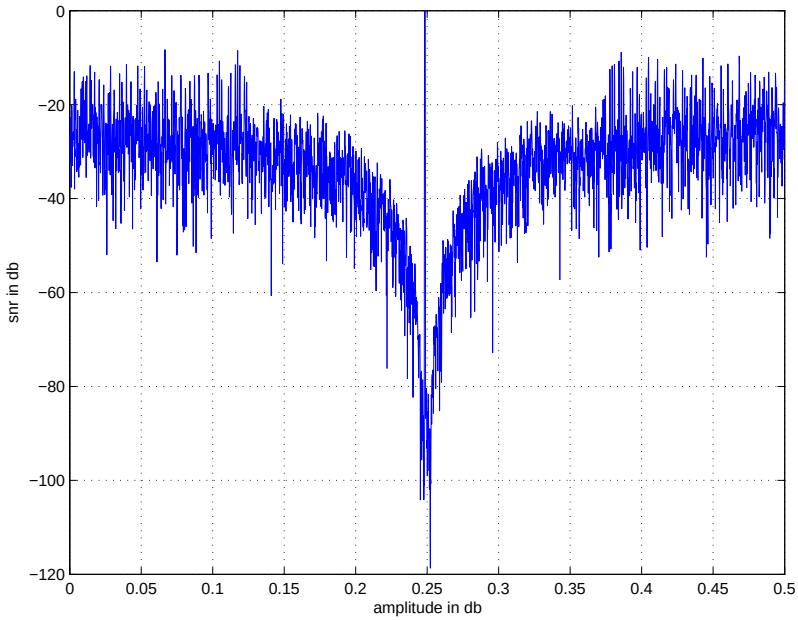

Figure 3.8: PSD curve of a 4^{th} order CRFF architecture modulator using a cosinusoidal DAC after STF adjustment

For the two proposed architectures, we have found that the adjustment coefficient is equal to 2.19. Figure 3.8 illustrates the PSD curve after the STF adjustment of the 4^{th} order CRFF architecture having a cosinusoidal DAC.

This method will be also used for LC filtered converters.

3.4 Design of feedback LC filtered ΣΔ converters

In what follows, we give a general model of LC filtered modulator and particularly consider three different approaches for the design of LC filtered ΣΔ modulators using undersampling.

In each approach we propose to find the equivalence between a CT ΣΔconverter composed of m LC filters with a $n = 2m$ ordered DT converter.

The characteristics of each structure are explained as well.

3.4.1 General model of LC filtered converter

Figure 3.9 shows the general model adopted for the design of LC filtered converters

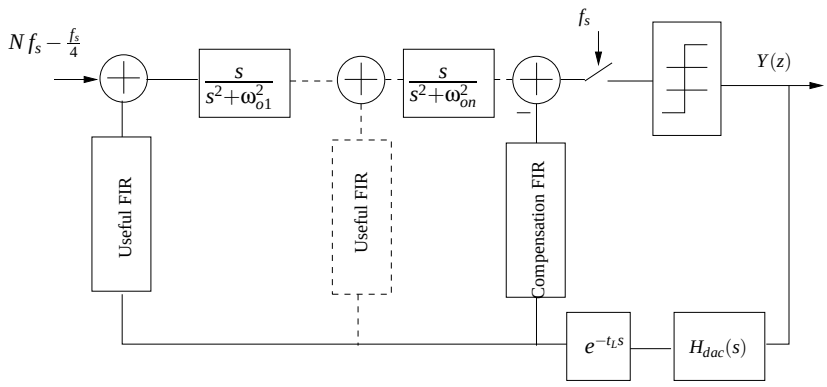

Figure 3.9: General model of the design of LC filtered converter

As it is shown in Fig3.9, we denote by useful FIR, the feedback FIR filter that is connected to the LC filter and by the compensation FIR filter, the FIR filter that is looped to the quantizer.

3.4.2 Compensation coefficients

Delays in the feedback path may create partial fractions given by $\frac{1}{z^i}$. To eliminate them, we need to add compensation elements in the compensation path.

But we have seen in the previous chapter that for some delays, compensation coefficient may be inefficient if the corresponding Z transform is null.

Let us determine the expression of the Z transform of the sinusoidal and cosinusoidal DACs.

3.4.2.1 Sinusoidal DAC

The Z modified transform of a compensation path delayed by $t_d \in]kT, (k+1)T]$ is

$$\begin{aligned} \mathbf{Z}_m\{C_{path}\} &= \frac{z-1}{z^k} \sum_{p_i \text{ singularity of } H_{dac}(s)} \text{Res}\left(\frac{\omega_{\text{lo}} \text{e}^{\text{mTs}}}{(\text{s}^2+\omega_{\text{lo}}^2)(\text{z}-\text{e}^{\text{sT}})}\right) \\ &= \frac{z-1}{z^k}\left(\frac{\omega_{lo} e^{mIT\omega_{lo}}}{2I\omega_{lo}(z-e^{I\omega_{lo}T})} + \frac{-\omega_{lo} e^{-mIT\omega_{lo}}}{2I\omega_{lo}(z-e^{-I\omega_{lo}T}))}\right. \end{aligned} \tag{3.7}$$

where $m = k + 1 - \frac{t_d}{T}$, and $\omega_{lo} = \frac{2\pi N}{T}$

Substituting ω_{lo} by $\frac{2\pi N}{T}$, we will get

$$\mathbf{Z}_m\{C_{path}\} = \frac{sin(2\pi N m)}{z^k} \tag{3.8}$$

Consequently, if $m = \frac{q}{2N}, q \in \mathbb{N}$, $\mathbf{Z}_m\{C_{path}\}$ is null and the compensation coefficient is inefficient.

Therefore, delays that are multiple of the half of the sampling period don't allow the DT-CT transformation. However in practice only these delays are feasible. Fig3.10 illustrates the loss of SNR resulting from using these delays instead of the theoretical compensation delays given by $kT + \frac{5T}{8}$.

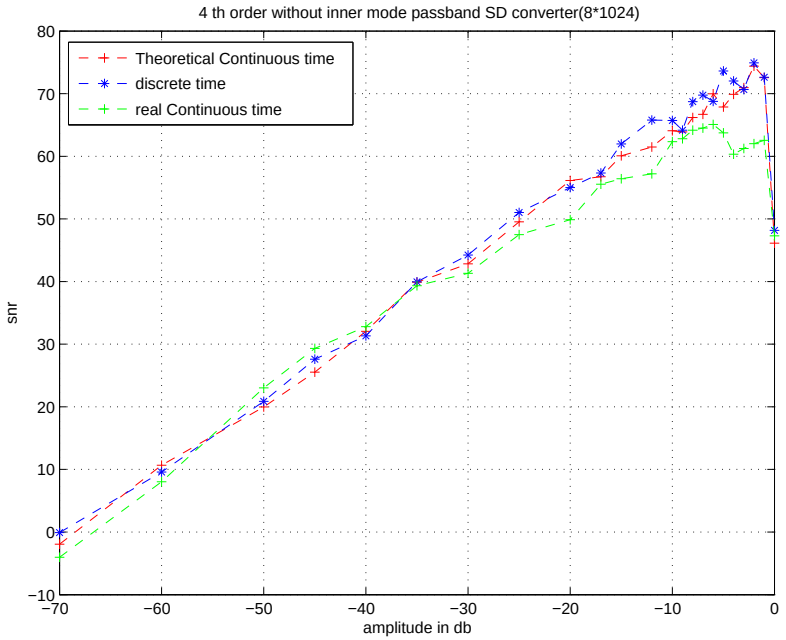

Figure 3.10: SNR loss caused by inefficient compensation coefficient

We note that the SNR loss is more significant for high amplitudes.

3.4.2.2 Cosinusoidal DAC

The Z modified transform of a compensation path delayed by $t_d \in]kT,(k+1)T]$ is: (See Appendix A)

$$\begin{aligned}\mathbf{Z}_m\{C_{path}\} &= \frac{z-1}{z^k}\sum_{p_i \text{ singularity of } H_{dac}(s)} \frac{\omega_{lo}^2 e^{mTs}}{s(s^2+\omega_{lo}^2)(z-e^{sT})} \\ &= \frac{z-1}{z^k}\left(\frac{\omega_{lo}^2 e^{mIT\omega_{lo}}}{-2\omega_{lo}^2(z-e^{I\omega_{lo}T})} + \frac{\omega_{lo}^2 e^{-mIT\omega_{lo}}}{2\omega_{lo}^2(z-e^{-I\omega_{lo}T}))} + \frac{1}{z-1}\right.\end{aligned} \tag{3.9}$$

where $m = k+1-\frac{t_d}{T}$, and $\omega_{lo} = \frac{2\pi N}{T}$

Substituting ω_{lo} by $\frac{2\pi N}{T}$, we get:

$$\mathbf{Z}_m\{C_{path}\} = \frac{-\cos(2\pi N m)+1}{z^k} \tag{3.10}$$

We note that $\mathbf{Z}_m\{C_{path}\}$ is null when mN is integer. To meet to practical requirements we need $t_d = \{\frac{q}{2T}\ q \in 2\mathbb{N}+1\}$ and N odd.

In the following, we propose to apply the method given in chapter 2 for the LC filters based modulators.

Three approaches will be considered. In the two first approaches the delay loop is null thus the set of compensation delays S_C is given by

$$S_C = \{0, t_C + kT, k \in [\![0, n_c-1]\!]\}$$

where n_c is the number of compensation elements connected to non null delays. The compensation transfer function is given by:

$$H_C = \sum_{i=0}^{n_c-1} x_i e^{-(t_C+iT)s} H_{dac}(s) + y_0 H_{dac}(s)$$

where x_i are the compensation coefficients connected to non null delays and y_0 is the compensation coefficient connected to a null delay.

In the third approach the delay loop is non null and is given by $\frac{q}{2T}\ q \in \mathbb{N}$. Hence, the useful compensation filter writes as:

$$H_C = \sum_{i=0}^{i=n_c-1} x_i e^{-(t_C+iT+t_L)s} H_{dac}(s)$$

3.4.3 1^{st} approach: two coefficients in each useful loop filter

This approach consists in considering only two coefficients in each useful loop filter. The number of coefficients in the compensation filter H_C is determined in the next paragraph.

The expression of the i^{th} useful filter is: ($i \in [\![1, \frac{n}{2}]\!]$ where n is the modulator order)

$$H_{Ui} = k_{2i} e^{-t_{d2i}s} + k_{2i+1} e^{-t_{d(2i+1)}s}$$

A null delay loop is also considered.

3.4.3.1 CT loop gain

The Z modified transform of the CT loop gain of a $\Sigma\Delta$ modulator having such architecture is:

$$\mathbf{Z}_m\{CT\} = \sum_{i=1}^{i=\frac{n}{2}} \underbrace{Z_m[\frac{H_{Ui}H_{dac}}{z-e^{sT}} \prod_{j=i}^{j=\frac{n}{2}} \frac{s}{(s^2+\omega_j^2)}]}_{i^{th}\text{useful transfer function}} - \underbrace{Z_m[H_C H_{dac}(s)]}_{\text{compensation transfer function}}$$

3.4.3.2 Determination of the LC filters pulsations and the number of compensation coefficients

Determination of the LC filters pulsations The assumptions of the method that we have developed in the previous chapter are verified. That is:

- The number of coefficients is equal to the order of the modulator.
- The singularities of the sine shaped DAC's are inside the set $\{\frac{2\pi n}{T} n \in \mathbb{Z}\}$.

Having $\omega_i = -\arccos(1-\frac{gd_i^2}{2}) + 2\pi N$ allows to perform the DT CT transformation between the DT Schreier toolbox modulators and the considered CT ones (LC filtered of the first approach)

Number of compensation delays Let's maxdelay be the maximum of delay in the feedback path and M defined in Equation (B.2)

The number of needed compensation coefficients is given by:

- $M+1$ if there is a null delay in the feedback path.
- M otherwise.

If all delays are non null, then the delays in the compensation path must belong to $]iT,(i+1)T]$ where $i \in [\![0, M-1]\!]$., otherwise a null delay in the compensation path may be required.

For example if all feedback delays are non null and we have a maximum of delay of $\frac{5T}{2}$, we should add 3 compensation elements connected to the delays: $\frac{T}{2}$, $\frac{3T}{2}$ and $\frac{5T}{2}$

3.4.3.3 Determination of the feedback coefficients

The determination of feedback coefficients have been performed by using Maple.

For an LC filtered 4^{th} order $\Sigma\Delta$ modulator with a cosinusoidal DAC we have found the following coefficients:

	1^{st}Useful filter		2^{nd}Useful filter		Compensation filter
coefficient	k_1	k_2	k_3	k_4	x
delay	1	$\frac{1}{2}$	1	$\frac{1}{2}$	$\frac{1}{2}$
value	0.658	0.509	2.172	1.438	0.1744

We need an adjustment coefficient of 4.6198, when the undersampling rate is of 11, which implies that $\omega_1 = 67.5583$ and $\omega_2 = 67.53$

Figure 3.11 shows a good fit between the SNR versus amplitude curve of CT and DT modulators.

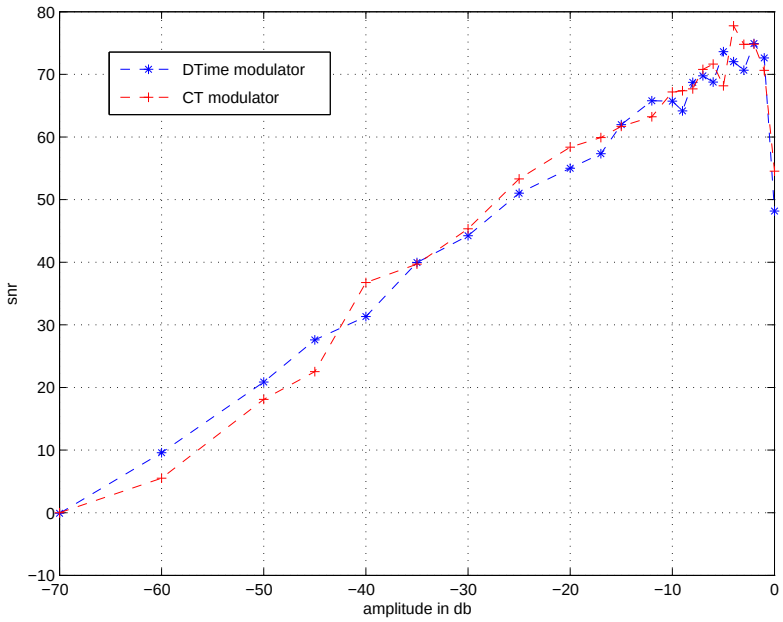

Figure 3.11: 4^{th} order LC filtered converter

3.4.3.4 Some characteristics of the 1^{rst} proposed architecture

For practical reasons, after each feedback loop, a transconductor is needed in order to convert voltage into current. Thus, having more than one feedback loop, this architecture have the disadvantage of needing more components.

3.4.4 2^{nd} approach: Only one Useful filter is used

This approach consists in considering only one useful loop filter composed of n coefficients. All delays that are connected to those coefficients are different. The number of compensation coefficients and compensation delays are determined by the same method as the first approach. We assume also in this case that the delay loop is equal to zero.

The useful loop filter has the following expression:

$$H_U = \sum_{i=1}^{i=n} k_i e^{-t_{di}s}$$

3.4.4.1 CT loop gain

The CT loop gain of a $\Sigma\ \Delta$ converter with the considered architecture is:

$$\mathbf{Z}_m\{CT\} = Z_m[\frac{H_U H_{dac}}{z - e^{sT}} \prod_{j=1}^{j=\frac{n}{2}} \frac{s}{(s^2 + \omega_j^2)}] - Z_m[H_{dac} H_C]$$

3.4.4.2 Determination of ω_i and compensation delays

It is preferred for this architecture to refer to ideal converters while doing the DT-CT transformation. In fact, in this case, the value of ω_i must be equal to :

$$\omega_i = Nf_s - \frac{f_s}{4}$$

Which implies that the LC filters are identical and as there is no internal feedback loop, it is possible to assemble them into one block.

The number of compensation delays and their values is determined by using the same method explained in the first approach.

3.4.4.3 Determination of feedback coefficients

The determination of feedback coefficients has also been performed with Maple. For an LC filtered 4^{th} order $\Sigma\Delta$ modulator with a cosinusoidal DAC, we have found the following coefficients.

	Useful filter				Compensation filter	
coefficient	k_1	k_2	k_3	k_4	extra_1	extra_2
delay	0	$\frac{1}{2}$	$\frac{3}{2}$	2	0.5	$\frac{3}{2}$
value	-9	-8.3	6.16	2.74	0.1592	0.002197

The undersampling ratio is equal to 11 and thus the resonance frequency of the two filters is equal to 67.5442 The adjustment coefficient is found to be equal to 1.

3.4.4.4 Some characteristics of the 2^{nd} approach

The 2^{nd} approach has the advantage of containing only one useful feedback loop. However, a compensation loop filter is still needed.

3.4.5 Third approach: One loop feedback filter and a non null delay loop

This approach consists in considering a unique loop filter composed at least of n coefficients, where n is the order of the DT modulator with which the equivalence is performed. A non delay loop is also allowed.

The useful filter has the following expression:

$$H_U = \sum_{i=1}^{i=L} k_i e^{-t_{di}s}$$

where L is the number of useful coefficients.

3.4.5.1 CT loop gain

The CT loop gain has the following expression:

$$\mathbf{Z}_m\{CT\} = \underbrace{(1-z^{-1})Z_m[\frac{H_U H_{dac} e^{-t_L s}}{z-e^{sT}} \prod_{j=1}^{j=\frac{n}{2}} \frac{s}{(s^2+\omega_j^2)}]}_{\text{Useful transfer function}} - \underbrace{(1-z^{-1})Z_m[\frac{H_{dac}H_C}{z-e^{sT}}]}_{\text{Compensation transfer function}} \tag{3.11}$$

3.4.5.2 Determination of the number of useful and compensation coefficients

We recall that for one loop feedback architectures, we refer to ideal converters. In this approach a non delay loop is considered. The compensation loop filter have the following expression

$$H_C = \sum_{k=0}^{k=n_c-1} x_k e^{-(t_C+t_L+k)s} H_{dac}(s)$$

where n_c is the number of compensation elements.

Let maxdelay be the maximum delay in the useful feedback path taking into account the delay loop t_L.

Let M be the integer defined as maxdelay $\in](M-1)T, MT]$ and j be the integer that satisfies: $t_C + t_L \in]jT, (j+1)T]$.

The expression of the useful transfer function writes as:

$$Z_U = \sum_{i=1}^{i=\frac{n}{2}} (\frac{c_i}{(z-e^{I\omega_0 T})^i} + \frac{\overline{c_i}}{(z-e^{-I\omega_0 T})^i} + \sum_{i=1}^{i=M} \frac{d_i}{z^i}$$

, and the expression of the compensation transfer function is given by:

$$Z_C = \sum_{i=1}^{n_c} \frac{g_j}{z^{j+i-1}}$$

The expression of the DT loop filter with which the equivalence should be performed is:

$$Z_{DT} = \sum_{i=1}^{i=\frac{n}{2}} \frac{\beta_i}{(z-e^{I\omega_0 T})^i} + \frac{\overline{\beta_i}}{(z-e^{-I\omega_0 T})^i}$$

The number of compensation elements that we have chosen is equal to $n_c = M + n - L \leq M$.

Identifying the partial fractions of Z_{DT} with that of $Z_U - Z_C$, we get:

$$\begin{aligned}
\Re c_i(k_1,...,k_L) &= \Re\beta_i, i \in [\![1, \frac{n}{2}]\!] \\
\Im c_i(k_1,...,k_L) &= \Im\beta_i, i \in [\![1, \frac{n}{2}]\!] \\
d_i(k_1,...,k_L) &= 0, i \in [\![1, j-1]\!] \\
d_i(k_1,...,k_L) - g_i(x_1,...,x_{n_c}) &= 0, i \in [\![j, n_c]\!] \\
d_i(k_1,...,k_L) &= 0, i \in [\![n_c+1, M]\!].
\end{aligned}$$

We have therefore to solve a linear system having $n+M$ equations and n_c+L unknown coefficients which can be written in the following matrix representation

$$AX = b$$

where $A \in \mathbb{R}^{(n+M)\times(n_c+L)}$ and $b \in \mathbb{R}^{(n_c+L)}$. We could verify easily that for the chosen value of n_c, we have as many equations as unkowns. A is therfore a square matrix.

As A is not in general invertible, we cannot write X under the form $X = A^{-1}b$.

The solution of this system can be the empty set ($S = \emptyset$), a single element($S = x_0$) or an affine space given by

$$S = \{x_0 + \sum_{i=1}^{i=dim} \lambda_i v_i, \lambda \in \mathbb{R}\} \tag{3.12}$$

where dim is the dimension of the space of solutions.

3.4.5.3 Some characteristics of the 3^{rd} approach

It is obvious that this approach is the most interesting. In fact it not only considers a unique feedback loop, but also allows removing of compensation loop filter, if $L = M + n$ ($n_c = 0$). When doing computations with maple, we have found that this is only possible for a 2^{nd} order LC filtered modulator using a sinusoidal DAC. Mathematical proofs of this propriety may require a lot of calculations, and is not detailed in this report. Besides, It is also noted that, all solutions in the set S allow the DT-CT equivalence, and therefore, we can determine the value of λ_i that minimizes certain practical constraints.

3.4.5.4 Determination of feedback coefficients

A unique loop $\Sigma\Delta$ converter without a compensation path As we have precised in the previous section, a2^{nd} Σ Δ modulator has been designed without the use of a compensation coefficients. The following table shows the coefficients that have been used for this modulator employing a rate of undersampling of 10. The adjustment coefficient is equal to 1.5028.

	Useful filter				
coefficient	k_1	k_2	k_3	k_4	k_5
delay	$\frac{1}{2}$	1	$\frac{3}{2}$	3	$\frac{5}{2}$
value	0	2.648	-1.979	-.1514	.517

To validate these coefficients, simulations have been performed and have shown the equivalence between the CT and DT converters. (Fig3.12)

An infinite set of solutions We have proved in the previous section that if the number of unknowns is greater than the number of independent equations we can have an infinite set of solutions.

For example, for a 2^{nd} order LC filtered converter, using a cosinusoidal DAC, and having an undersampling ratio of 11, the set of solutions is:

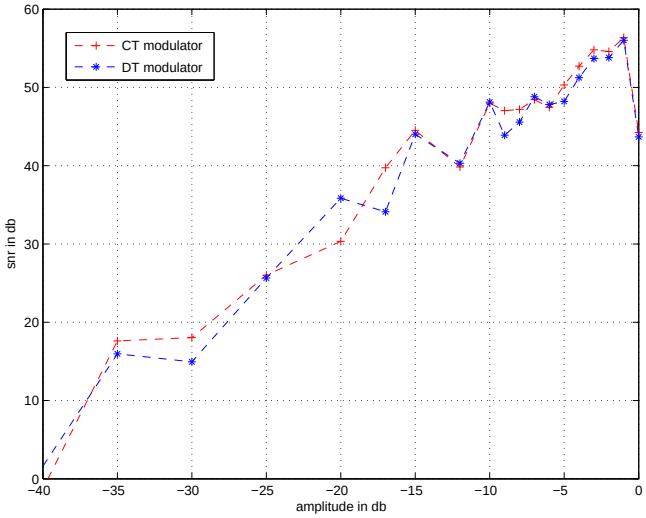

Figure 3.12: 2^{nd} order $\Sigma\Delta$ converter without compensation loop filter

	Useful filter		Compensation filter	
coefficient	k_1	k_2	x_1	x_2
delay	2	0	0	2
value	λ_1	λ_1-1.43	0.1164λ_1+0.166	-0.1164λ_1

Figure 3.13 shows that with$\lambda_1 = 0$, $\lambda_1 = 1$ and $\lambda_1 = 2$, $\Sigma\Delta$ converter is equivalent to the DT one.

3.5 Non ideal LC filtered converters

Until now, we have considered that the LC filter has the next expression:

$$H_{LC} = \frac{s}{s^2 + \omega_0^2} \tag{3.13}$$

However, equation 3.13 implies that the used self has a resistance equal to zero, something that is hard to achieve in practice and that requires special quality factor enhancement circuits. The non-ideal LC filter has the following expression:

$$H_{LC} = \frac{s}{s^2 + \frac{\omega_0 s}{Q} + \omega_0^2} \tag{3.14}$$

where Q is the quality factor of the filter and ω_0 is the resonance pulsation. The determination of the coefficients has always been performed by considering the ideal expression of the LC filter because with the non-ideal one the DT-CT equivalence is impossible and not because the calculations are very hard as stated in [14].

This fact can be proved by only considering the necessary conditions explained in the previous chapter.

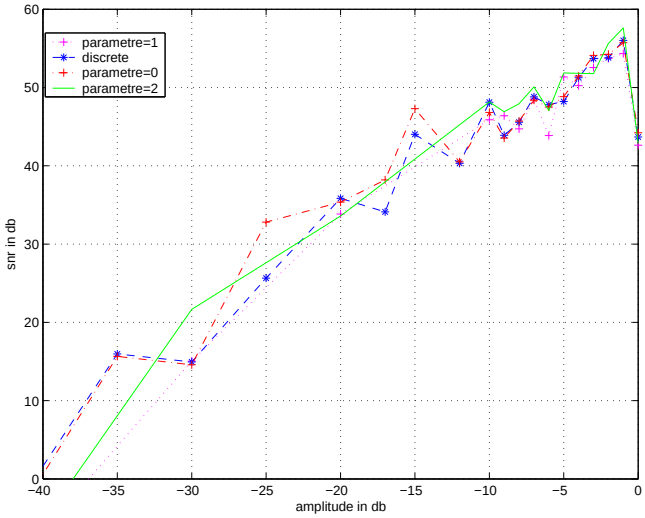

Figure 3.13: DT-CT equivalence for different parameters

It is clear that the singularities of the loop filter are:

$$\{-\frac{\omega_i}{Q} \pm I\sqrt{-\frac{\omega_i^2}{Q^2} + 4\omega_i^2}\}$$

In fact, for CRFF and ideal architectures the loop gain poles q_i are on the unit circle. While the singularities of a non-ideal LC modulator are given by $p_i = e^{r_i \pm I x_i}$ where

$$r_i = -\frac{\omega_i}{Q} \text{ and } x_i = \sqrt{-\frac{\omega_i^2}{Q^2} + 4\omega_i^2}$$

As shown in the previous chapter, the DT-CT transformation requires to identify the poles q_i with the $e^{p_i T}$. This transformation is then impossible when $Q \neq \infty$ which corresponds to non-ideal modulators.

As it is in practice impossible to design LC filters with an infinite quality factor we have performed simulations in order to assess the range of values of quality factors over which the performance of the CT $\Sigma\Delta$ modulator is not being degraded a lot.

Figure 3.14 illustrates the degredation of the performance of a 2^{nd} order LC filtered $\Sigma\Delta$ converter having an undersampling ratio of 1, when the quality factor decreses.

3.6 Design automation of $\Sigma\Delta$ modulators

In order to automate the design of LC filtered $\Sigma\Delta$ converters using undersampling, a Matlab graphic user interface that computes the feedback and compensation coefficients according to the third approach have been developed.

This interface consists of three parts: (Fig 3.15)

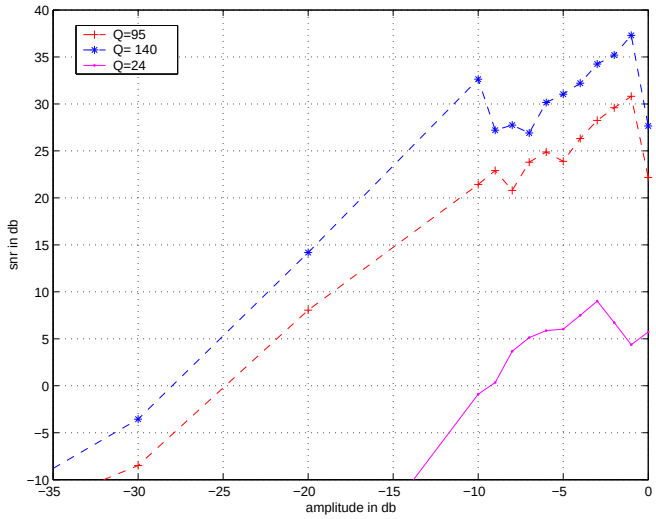

Figure 3.14: Influence of the quality factor on the performance of the 2^{nd} order LC filtered $\Sigma\Delta$ modulator having an undersampling ratio of 1

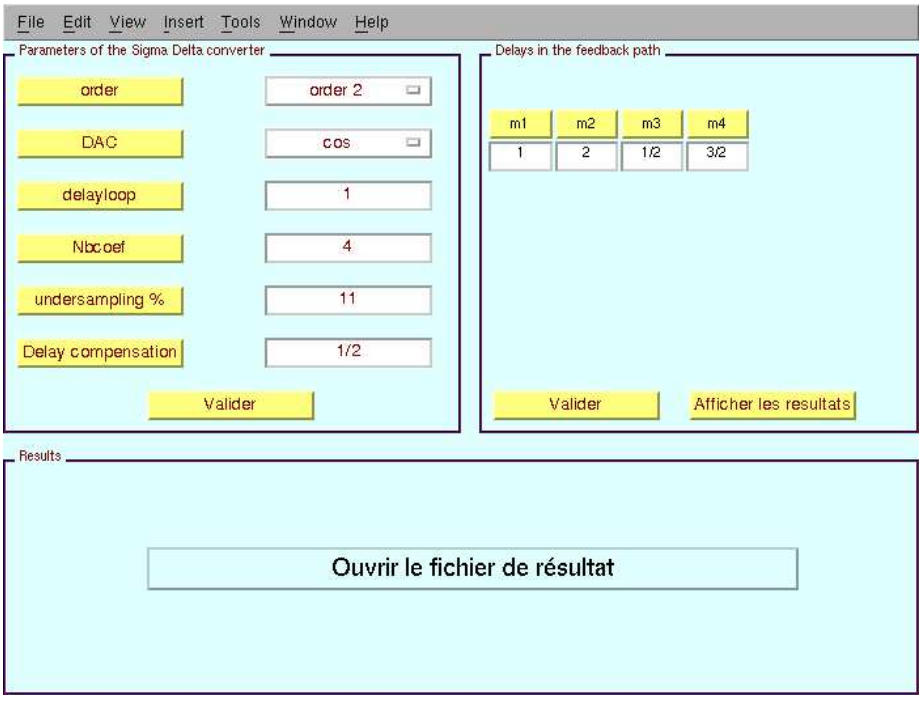

Figure 3.15: A graphic interface for the automation of the design of LC filtered Σ Δ converters

- 1^{st} part: The user sets the order of the LC converter, the number of feedback coefficients, the kind of DAC, the delay loop, the undersampling ratio and the compensation delay. The delay loop must be a multiple of the sampling period, the undersampling ratio must be integer and the number of feedback coefficients must be greater than the order of the converter.
- 2^{nd} part: Once the number of coefficients is specified in the first part, the user gives the delays that he wishes to have in the feedback path. To display the results, he should validate and click on the button "afficher les résultats".
- 3^{rd} part: To display the results, the user should click on the button"ouvrir les fichiers de résultats".

  The results are then displayed as it is shown in Fig3.16

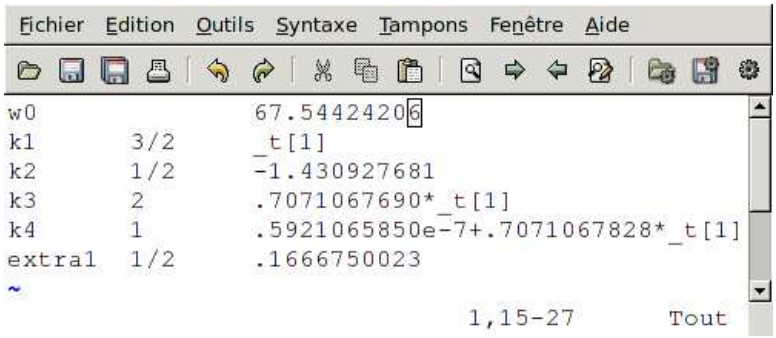

Figure 3.16: Results displaying by the interface

3.7 Conclusion

In this chapter, we have explained three different approaches for the design of LC filtered $\Sigma\Delta$ converters. We have also proved their validity by comparing the SNR level of the proposed architectures with that of the DT converters. A comparison between these three approaches have also been made. In order to allow the automation of the design of $\Sigma\Delta$ converters, a Matlab graphic user interface has been developed.

Conclusion

Conclusion

In this report, a method for the achievement of DT-CT transformation was presented. The proposed method has been verified for the CRFF architectures which have already been studied in previous works. Necessary conditions for the possibility of DT-CT transformation were derived. The value of compensation delays and their numbers were also discussed.

Then, this method has been applied on a new architecture based on LC filters, employing undersampling and a high pass DAC in the feedback.

Three different approaches based on different configurations of the feedback useful loop filter have been analysed and compared.

A Matlab graphic user interface, that automates the determination of the CT coefficients for the third approach, has been finally presented

Future work

Several points are worth considering:

Influence of some non idealities on the proposed architectures

Non idealities in the feedback loop cause a significant degradation on the performance of the $\Sigma\Delta$ modulator. The use of a cosinusoidal DAC rather than a sinusoidal one can make the $\Sigma\Delta$ modulator less sensitive to these non idealities.

A comparision between the performance of these two DAC's should be then analysed in details.

Practical constraints

When the added coefficients of the feedback useful loop are more than required, the feedback coefficients depend on a parameter which can be set to any real value, without causing any degradation on the performance of the $\Sigma\Delta$ modulator.

This parameter could be set so as to minimize the power consumption of the DAC or also to facilitate the implementation of the $\Sigma\Delta$ modulator.

Appendix A

Mathematical Preliminaries

A.1 Fractions

Definition 1 Proper fractions *Let f be a fraction. There exists N and D polynomials so that*

$$f = \frac{N}{D}$$

f is improper fraction if the degree (highest power) of N is greater or equal to the degree of D, otherwise it is called a proper fraction.

Theorem 1 *Over the field $\mathbb{R}$ of real numbers, the unique partial fractions are:*

$$\frac{\alpha}{(x-a)^n} \text{and} \frac{\beta x + \gamma}{(x^2 + bx + c)^n}$$

where $a, \alpha, \beta, \gamma, b$ and c are real numbers and $b^2 - 4c < 0$, and n is an integer.

Over the field $\mathbb{C}$ of complex numbers, the unique partial fractions are

$$\frac{\alpha}{(x-a)^n}$$

where α and a are complex numbers.

Theorem 2 *Every proper fraction could be decomposed in a unique manner into partial fractions over a specific field.*

This theorem will be the fundamental tool that we will use along this report.

A.2 Expression of the residue for fractions

Let R denote a fraction. R could be written as the quotient of two plynomials P and Q.

$$R(\nu) = \frac{P(\nu)}{Q(\nu)}$$

The singularities of R are the roots of Q which are denoted by p_i. If p_i is a simple pole then the residue of R at p_i is

$$\text{Res}\left(\text{R}(\nu), \text{p}_\text{i}\right) = \frac{P(p_i)}{\frac{dQ(\nu)}{d\nu}_{|\nu=p_i}}$$

if p_i is a multiple pole with multiplicity equal to n then

$$\mathrm{Res}\,(\mathrm{R}(\nu), \mathrm{p_i}) = \frac{1}{(n-1)!}[\frac{d^{n-1}}{d\nu^{n-1}}(\nu - p_i)^n \frac{P(\nu)}{Q(\nu)}]$$

if p_i isn't a pole of R then

$$\mathrm{Res}\,(\mathrm{R}(\nu), \mathrm{p_i}) = 0$$

A.3 Z transform and Z modified transform

A.3.1 Z transform

Using residues, the expression of the Z transform of a fraction f is

$$\mathbf{Z}\{f(s)\} = \sum_{p_i \text{ singularity of } f} \mathrm{Res}\left(\frac{\mathrm{f(s)}}{(1 - \mathrm{e^{Ts}z^{-1}})}\right) \tag{A.1}$$

A.3.2 The Z modified transform

A.3.2.1 Definition

The Z modified transform of x(t) Z_m is the Z transform of $x(t - \lambda T)$ where λ =1-m. That's mean that

$$Z_m x = \sum_{n=0}^{n=+\infty} x((n-1+m)T)z^{-n}$$

By using residues, we could prove that for $\lambda \in]0, T]$

$$Z_m f(s) = \sum_{p_i \text{singularity of f}} \text{residues of } \frac{f(s)e^{mTs}}{z - e^{Ts}} \tag{A.2}$$

More generally for $\lambda \in]kT, (k+1)T]$, the Z modified transform is equal to

$$Z_m(f(s)) = \sum_{p_i \text{ singularity of f}} \text{residues of} \frac{f(s)e^{mTs}}{(z - e^{Ts}).z^{k-1}} \tag{A.3}$$

where $m = 1 - \frac{\lambda}{kT}$

A.3.2.2 Use of the Z modified transform

The Z modified transform is generally used to compute the Z transform for signals that are delayed. It is used only for practical reasons and the result that we obtain is the same as the conventional Z transform, if the signal is delayed by $1 - m$ where m is the parameter of the Z modified transform.

A.3.2.3 Z modified Transform of the response of a linear filter

In this section, we propose to compute the Z modified transform for a linear filter.

Let f be a linear filter with the following representation:

$$F = \frac{f(s)}{D(s)}$$

where f is a function in s and D is a polynomial in s. Let p_i the roots of D(s) in $\mathbb{C}$ and assume that p_i are simple poles

As f is not in general a polynomial, two cases have to be considered:

- if f is a polynomial in s then from A.2 we have

$$\begin{aligned} \mathbf{Z}_m\{F(s)\} &= \sum_{p_i \text{roots of D}} \frac{f(pi)}{\frac{d}{ds}_{|s=p_i} D(s)(z - e^{sT})} \\ &= \sum_{p_i \text{roots of D}} \frac{f(p_i)}{\frac{dD}{ds}_{|s=p_i}(z - e^{p_i T}))} \end{aligned} \tag{A.4}$$

$$\frac{d}{ds}_{|s=p_i} D(s)(z - e^{sT}) = \frac{D}{ds}_{s=p_i}(p_i)(z - e^{p_i T}) + \underbrace{D(p_i)(-T)(z - e^{p_i T})}_{=0}$$

As p_i is a zero of D,

$$\frac{d}{ds}_{s=p_i} D(s)(z - e^{sT}) = \frac{D}{ds}_{s=p_i}(z - e^{p_i T})$$

- f is the laplace transform of a linear filter having a delay $t_d \in]kT, (k+1)T]$ $k \in \mathbb{N}$, and T is the sampling period.

$$f(s) = N(s)e^{-t_d s}$$

Equation (A.2) gives

$$Z_m(F(s)) = \sum_{i=1}^{i=n} \frac{N(p_i)e^{mTp_i}}{z^k . \frac{D}{ds}_{s=p_i}(z - e^{p_i T})} \tag{A.5}$$

where $m = k + 1 - \frac{td}{T}$

$\mathbf{Z}_m\{f(s)\}$ could be written as the sum of partial fractions over the field $\mathbb{C}$ of complex numbers. In fact, by decomposing $Z_m(F(s))$ in partial fractions, we will get, from A.5

$$Z_m(F(s)) = \sum_{i=1}^{i=k} \frac{\alpha_i}{z^i} + \sum_{i=1}^{i=n} \frac{\beta_i}{z - e^{piT}} \tag{A.6}$$

Appendix B

Partial fractions of the CT loop gain

B.1 Useful transfer function

In what follows, we propose to determine a set containing the partial fractions of the Useful partial fraction. We assume that the singularities of the DAC are inside the set $\{\frac{2\pi n}{T}\}$. Two cases should be taken:

- A zero delay in the feedback path

  If there is a useful path where the signal is no delayed, ($H_{FIR1} = a_1 + \sum a_i e^{-t_{di}s}$.)

$$\begin{aligned} Z_m(H_{dac}H(s)) &= (1-z^{-1})Z(G(s)H(s)H_{FIR1}) \\ &= \underbrace{(1-z^{-1})Z[G(s)H(s)a_1]}_{1^{st}\text{term}=A_1} + \\ &\quad \underbrace{+(1-z^{-1})Z_m(G(s)H(s)\sum_{i=1}^{i=n_u} a_i e^{-t_{di}s})}_{2^{nd}\text{term}=A_2} \end{aligned} \tag{B.1}$$

  Where n_u is the number of useful feedback paths. According to the expression of the Z and the Z_m transform (See Appendix A), and if all the singularities of the loop filter are simple, we have

$$A_1 = (z-1)(\sum_{i=1}^{i=n} \frac{\alpha_i}{z-e^{p_i T}} + \frac{\alpha_0}{z-1})$$

  If all t_{di} are different from zero, we have

$$A_2 = (z-1)\sum_{j=1}^{j=n_u} \frac{1}{z^{l_j}} \sum_{i=1}^{i=n} (\frac{\gamma_i}{(z-e^{p_i T})} + \frac{\gamma_0}{z-1})$$

where l_j is the integer satisfying $t_{dj} \in](l_j - 1)T, l_j T]$.

The first term A_1 in this sum is an improper fraction whose numerator and denominator have the same degree, and in the general case (p_i could be multiple poles) the decomposition into partial fractions of the Useful transfer function will be a linear composition of the following partial fractions:

$$S_U = \{\frac{1}{z^k}, \frac{1}{z - e^{Tp_i}}, ..., \frac{1}{(z - e^{Tp_i)^m u_i}} k \in [\![0, M]\!]\}$$

where p_i are the singularties of $H(s)$ different from $\frac{2\pi n}{T}, n \in \mathbb{N}$, because such singularity will provide a partial fraction $\frac{1}{z-1}$, which will be simplified by (z-1), mu_i is the multiplicity of the pole p_i, and

$$M = \left\lceil \frac{\text{maxdelay}}{T} \right\rceil \tag{B.2}$$

where $\lceil x \rceil$ is the smallest integer superior or equal to x.

That's means that, if all poles are simple, (case of CRFF architecture)

$$Z_m(H_{dac}H(s)) = \sum_{i=1}^{i=n} \frac{c_i}{z - e^{Tp_i}} + \sum_{i=0}^{i=M} \frac{d_i}{z^i}$$

- All delays are different from zero

  The decomposition into partial fractions of the Useful transfer function will be a linear composition of the following partial fractions:

$$S_U = \{\frac{1}{z^k}, \frac{1}{z - e^{Tp_i}}, ..., \frac{1}{(z - e^{Tp_i)^m u_i}} k \in [\![1, M]\!]\}$$

  That's means that, if all the poles are simple,

$$Z_m(H_{dac}H(s)) = \sum_{i=1}^{i=n} \frac{c_i}{z - e^{Tp_i}} + \sum_{i=1}^{i=M} \frac{d_i}{z^i}$$

B.2 Compensation transfer function

We recall that the compensation transfer function is equal to

$$Z_m(H_{dac}H_{FIR2}) = (1 - z^{-1})Z_m(G(s)H_{FIR2})$$

Let's t_{di} be the delays of H_{FIR2}.

As the singularities of G(s) are inside the set $\{\frac{2\pi n}{T}\}$, the decomposition into partial fractions of this term will be a linear composition of the following partial fractions:

$$S_C = \{\frac{1}{z^{m_i}}, i \in \{1..n_c\}\}$$

where n_c is the number of compensation elements, and m_i is the integer satisfying $t_{di} \in](m_i - 1)T, m_i T]$, if t_{di} is different from zero, and $m_i = 0$ otherwise.

That's means that:

$$(1 - z^{-1}) Z_m(G(s) H_{FIR2}) = \sum_{i=1}^{i=n_c} \frac{g_i}{z^{m_i}}$$

Bibliography

[1] W. Gao and W. Snelgrove. "A 950 MHz IF second-order integrated LC bandpass delta-sigma modulator". *IEEE Journal of solid state circuits*, May 1998.

[2] Ut-Va Koc and Jaesik Lee. "Direct RF Sampling Continuous-Time Bandpass Δ-Σ A/D Converter Design For 3G Wireless Applications". *IEEE International Symposium on Circuits and Systems, ISCAS*, 2004.

[3] Sabrina Azrouf Frédéric Gourgue, Maurice Bellanger and Vincent Bruneau. "A Bandpass Subsampled Δ-Σ Modulator for Narrowband Cellular Mobile Communications". *IEEE International Symposium on Circuits and Systems, ISCAS*, 1994.

[4] W.Khun A.Hussein. "Bandpass Σ Δ Modulator Employing Undersampling of RF Signals for Wireless Communication ". *IEEE Transactions on circuits and systems II*, vol. 47:614–620, July 2000.

[5] Robert M. Gray. "Quantization Noise Spectra". *IEEE Transactions on information theory*, vol.36(No. 6):1220–1244, November 1990.

[6] Gabor C. Temes Steven R. Norsworthy, Richard Schreier. *"Delta-Sigma Data Converters Theory, Design and Simulation"*. IEEE PRESS, 1996.

[7] Richard Schreier. The delta sigma toolbox for matlab. *Oregon State University.*

[8] H. Aboushady. *"Conception en vue de la réutilisation de convertisseurs analogiques-numériques $\Sigma\Delta$ temps continu mode courant "*. PhD thesis, L'université Paris VI, 2002.

[9] M.M. Louërat H. Aboushady. "Systematic Approach for Discrete Time to Continuous-Time Transformation of Σ Δ Modulators". *IEEE International Symposium on Circuits and Systems, ISCAS*, May 2002.

[10] G.C. Temes J.C Candy. *"Oversampled Delta Sigma Converters"*. IEEE PRESS, 1992.

[11] O.Shoaei. *"Continuous Time Delta Sigma A/D Converters for High Speed Applications "*. PhD thesis, Carleton University, Ottawa,Canada, 1995.

[12] M.J Hawksford A.M Thurston, T.H Pearce. "Bandpass implementation of the Sigma Delta A-D conversion technique". *IEEE A/D and D/A International Conference*, pages 81–86, Septembre 1991.

[13] B.Zhang R.Schreier. "Delta Sigma Modulators Employing Continuous Time circuitry". *IEEE transactions on Circuits and Systems -I*, vol. 43:324–332, April 1996.

[14] Peter Mole R.Maurinom. "A 200-MHz IF 11 bit Fourth-Order Bandpass $\Sigma Delta$ ADC in SiGe". *IEEE journal of Solid State Circuits*, vol. 35(No. 7):614–620, July 2000.

[15] W. Martin Snelgrove Omid Shoaei. "A multi feedback design for LC bandpass $\Sigma\Delta$ modulators". *Proc. ISCAS-95*, vol. 1:171–174, April 1995.

[16] M.M. Louërat N. Beilleau, H. Aboushady. "Using Finite Impulse Response Feedback DAC To design $\Sigma\Delta$ modulators based on LC filters". *MWSCAS'05*, August 2005.

[17] M.M. Louërat H. Aboushady. "Loop delay compensation in bandpass continuous time sigma delta modulators without additional feedback coefficients ". *IEEE International Symposium on Circuits and Systems, ISCAS*, May 2004.

[18] Hae-Seung Lee Susan Luschas, Richard Schreier. "Radio Frequency Digital to Analog Converter". *IEEE journal of solid-state circuits*, vol. 39, Septembre 2004.

[19] Nicolas Beilleau Anis Latiri, Hassan Aboushady. "Design of Continuous-Time $\Sigma\Delta$ modulators with sine-shaped Feedback DAC's". *IEEE International Symposium on Circuits and Systems, ISCAS*, 2005.

[20] Hae-Seung Lee Susan Luschas. "High-Speed $\Sigma\Delta$ Modulators With Reduced Timing Jitter Sensitivity". *IEEE transactions on circuits and systems*, vol. 49, Novembre 2002.