Time based quantizers

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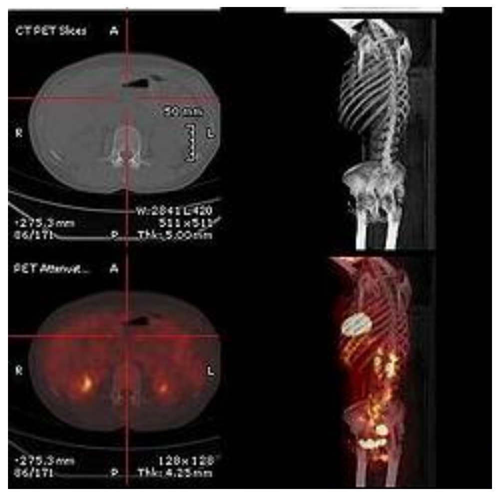
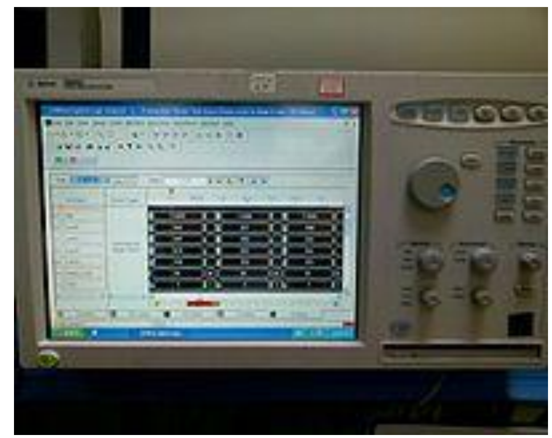
Time to digital Converters (TDC)

Applications

- Commercial time-of-flight applications such as Laser range-finding
- Positive electron temography medical imaging technology
- Logic Analyzers





Circuit & Systems

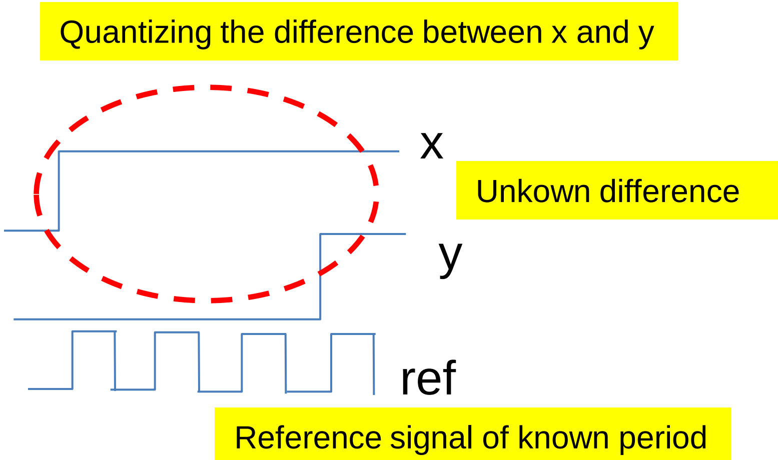
A fundemental element in systems made of closed loop integrated circuits that needs precise control and alignement of timing signals such as :

- Phase Locked Loop (PLL)
- Delay Locked Loop (DLL)
- Clock Data Recovery (CDR)

Types of Time to Digital Converters

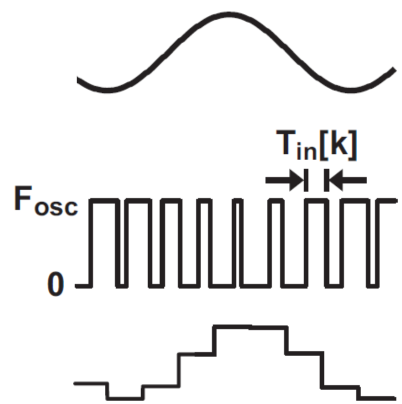
1) Classical TDC

Quantizing the difference in time between 2 signals
(PLL, DLL, CDR)



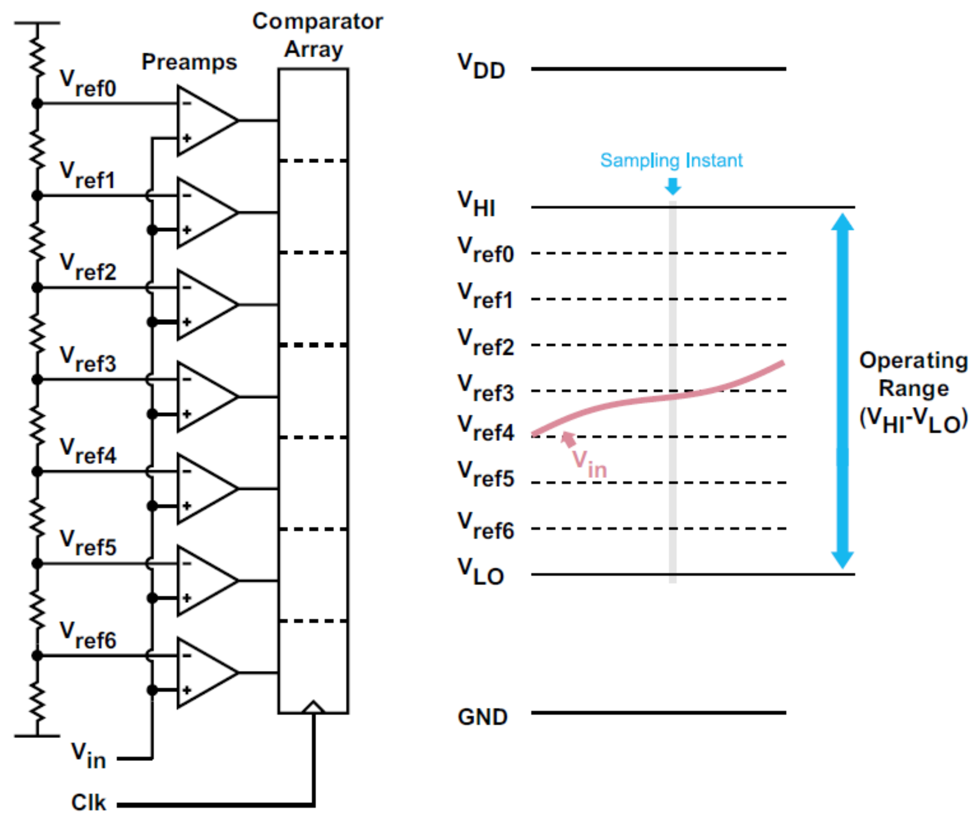
2) TDC as analog signal quantizers

A replacement for traditional voltage quantizers
(High resolution wideband ADC)



Technology Scaling Challenges

Multi-bit quantization using conventional Flash voltage quantizer



<u>Reduced supply & dimensions</u>

- Higher Ft ✓
- Lower Vref accuracy ✗
- Metastability ✗

<u>Motivation for TDC as ADC</u>

Detecting an edge transition from gnd to Vdd is easier than a voltage step of Vdd/(2^N)

- Only Vdd and gnd are used (low supply compatible)
- High precision detecting transitions (Resolution)
- Mostly digital implementations benefits of tech scaling in terms of power and area

Concept of TDC

The count of cycles of the reference signal represents the quantized value of Tin

$$T_{out}[k] = Out[k]\,T_q$$

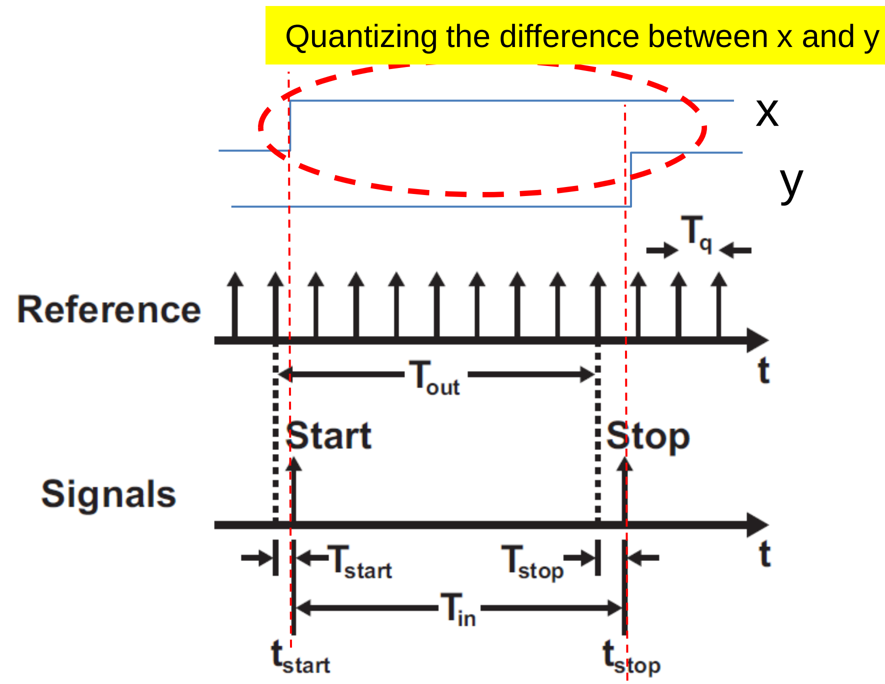
Quantized value of Tin

Count of Tq during Tin

$$T_{error}[k] = T_{stop}[k] - T_{start}[k].$$

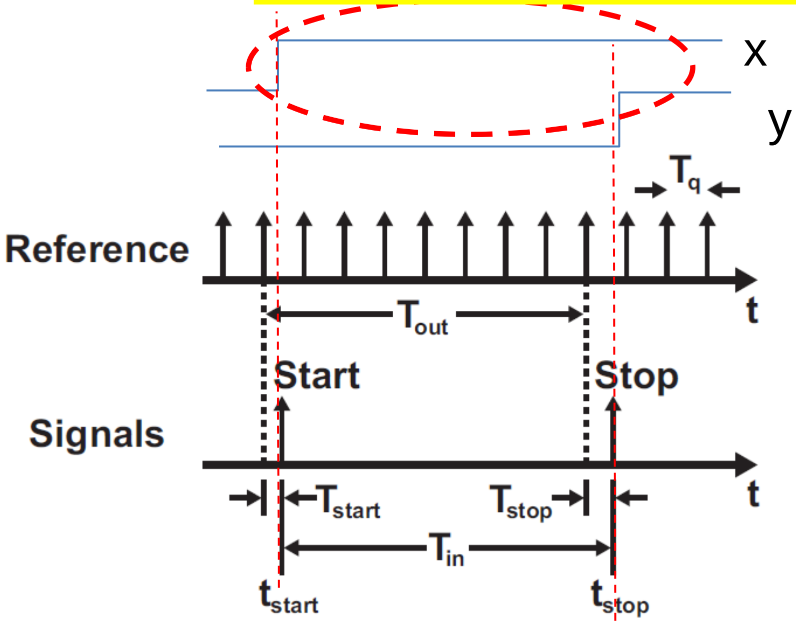
$$T_{out}[k] = T_{in}[k] - T_{error}[k],$$

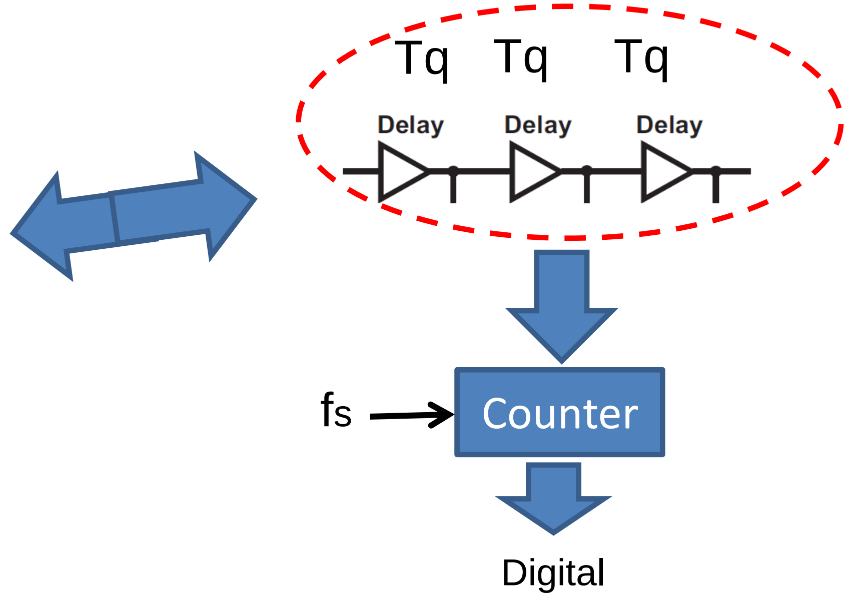
$$Out[k] = \frac{T_{in}[k] - T_{error}[k]}{T_q}.$$



Concept of TDC

Quantizing the difference between x and y





Definitions:

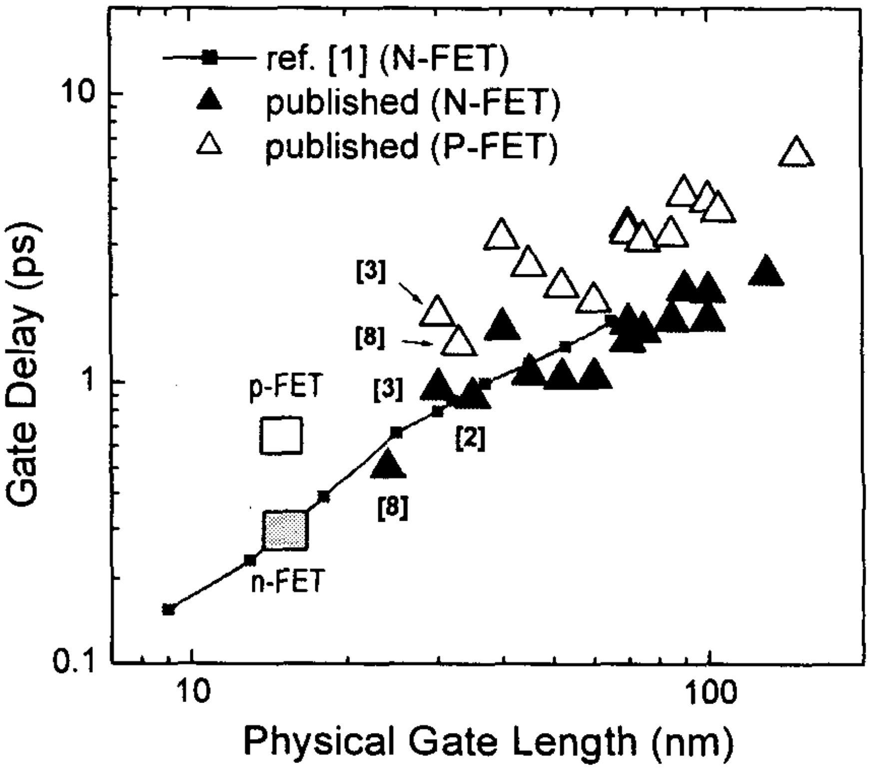
TDC resolution : Tq (reference signal period) ----- Limited by Technology Min gate delay

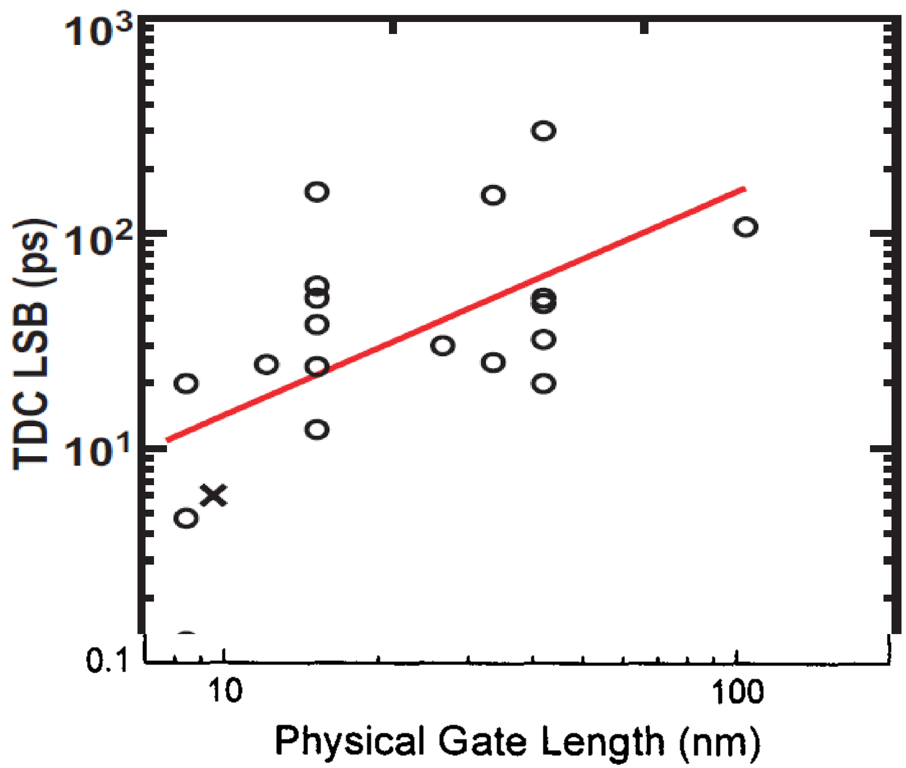
TDC Dynamic range: Max_count* Tq ----- Limited by fs

To enhance the TDC resolution:

1) Technology advancement to lower Technology min gate delay
2) Special design techniques to go below Technology min gate delay

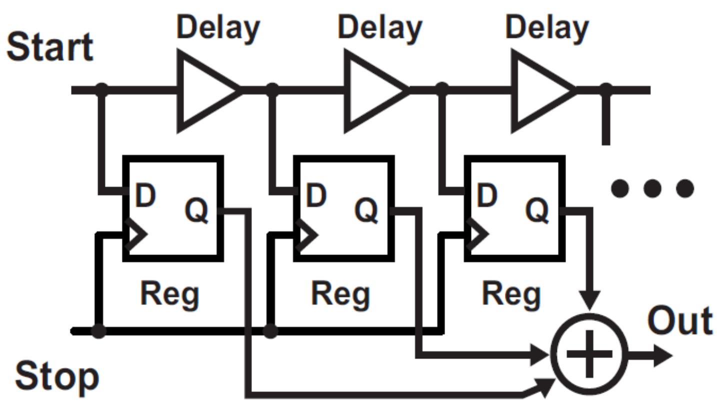
Technology Scaling and TDC resolution

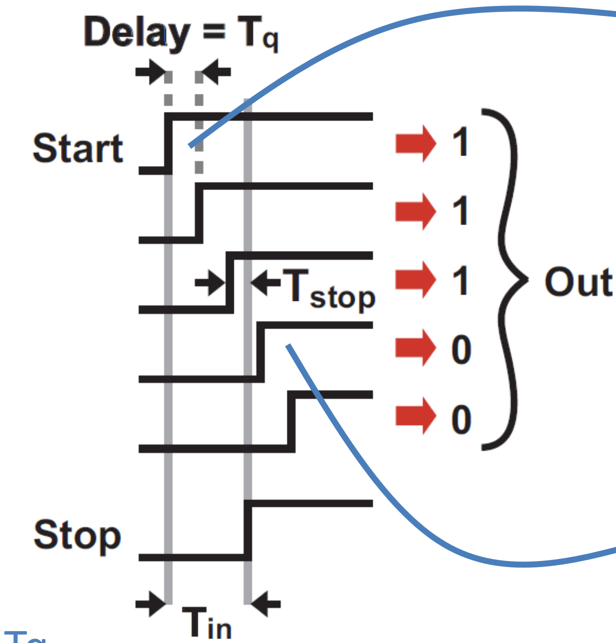




Gate Delay decreases in new technologies and so is the TDC (LSB)

1a) Inverter chain based





No error

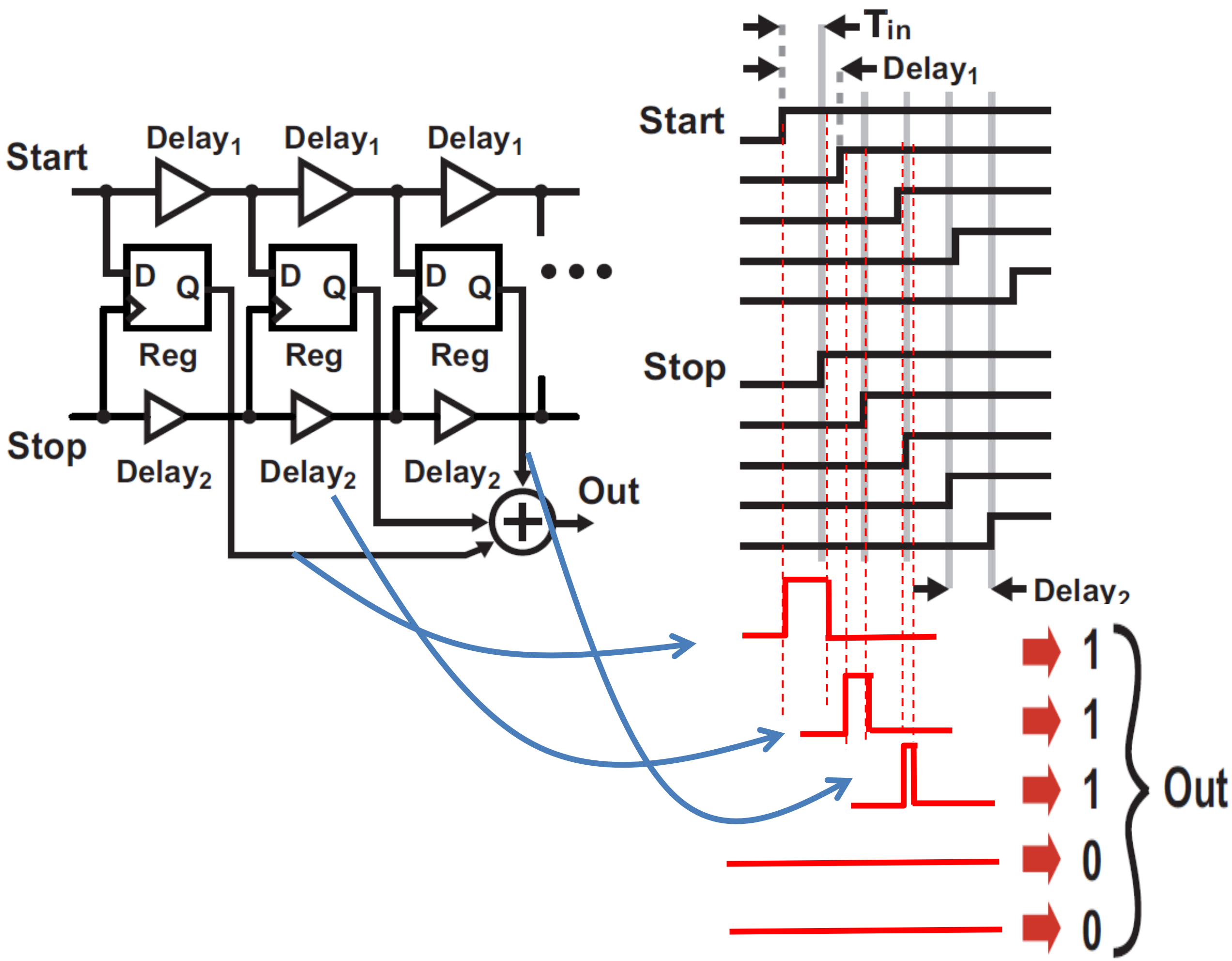
Output is thermometer

$$T_{error}[k] = T_{stop}[k].$$

- Line of delay elements generating Tq
- Tq propagates through the line
- Registers clocked by the stop signal hold the final value of each delay (thermometer)
- Addition of the registers output gives the quantized value of Tin

<u>For N-bit resolution, the number of delay elements = 2^N</u>
- High Cost (area)
- High Power

1b)Vernier based ($T_{start} - T_{stop} <$ delay1)



delay1> delay2

Tq=delay1- delay2

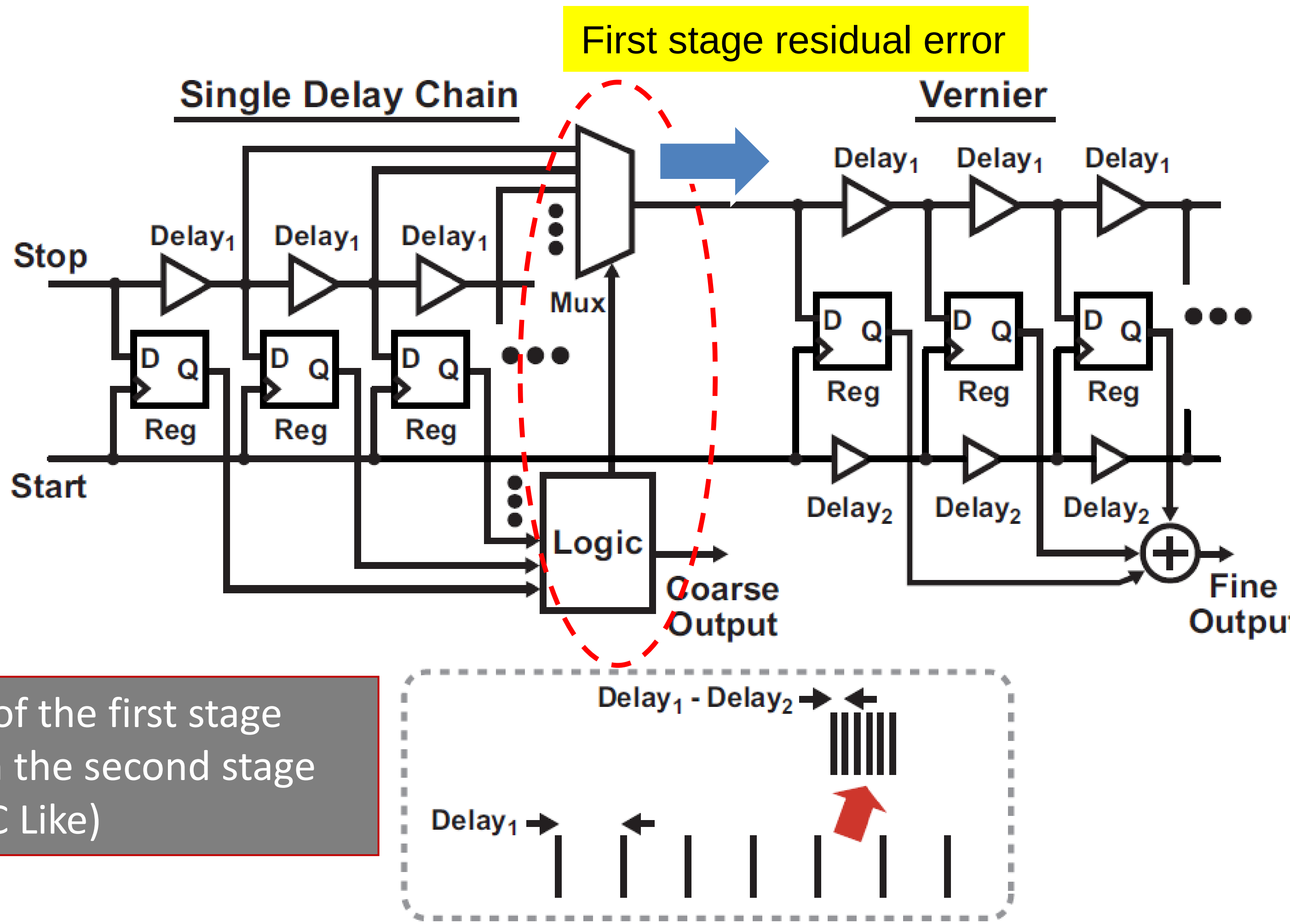
Output is thermometer

$$T_{error}[k] = T_{stop}[k].$$

Varying width pulse

- Better resolution at the same technology gate delay ✓
- Relatively large number of delay elements ✗

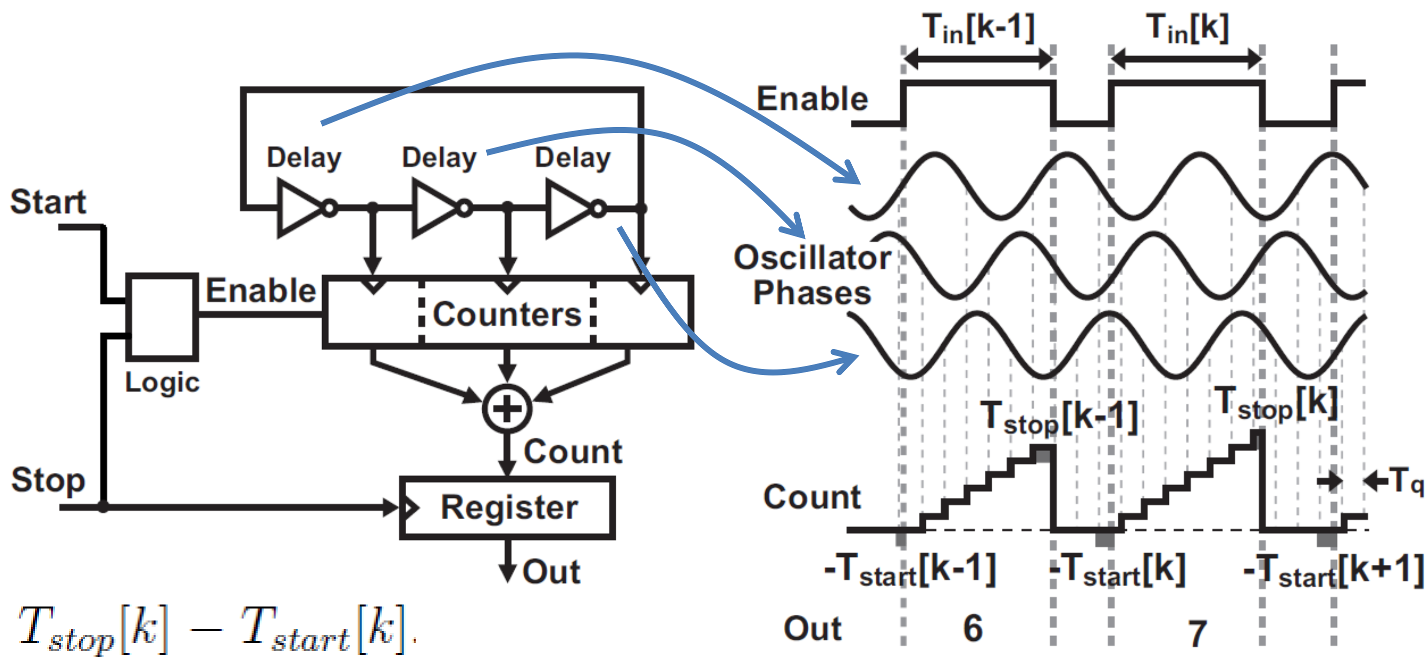
1c)Dual Step TDC



Amplifies the error of the first stage
And quantize it with the second stage
(Two-step Flash ADC Like)

Compromise Resolution and number of delay elements ✓

2a) Oscillator based TDC

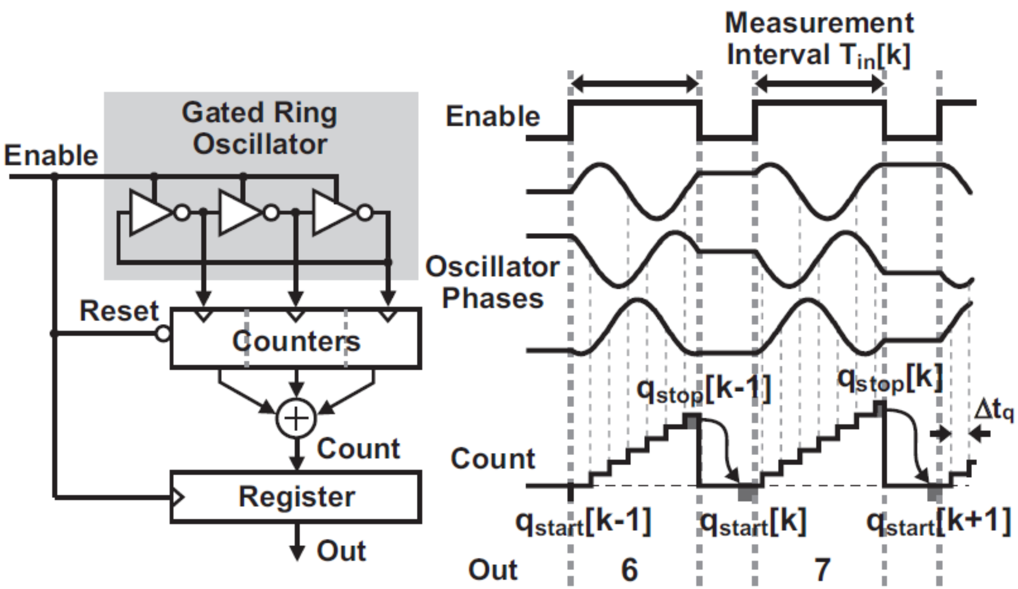


$$T_{error}[k] = T_{stop}[k] - T_{start}[k].$$

Least number of delay elements w.r.t preceding topologies ✓

Can we have better ?

2b) Gated Ring Oscillator based TDC



Theoretical approach !!
Not easy to implement

$$T_{start}[k] = T_{stop}[k-1]$$

$$T_{error}[k] = T_{stop}[k] - T_{stop}[k-1]$$

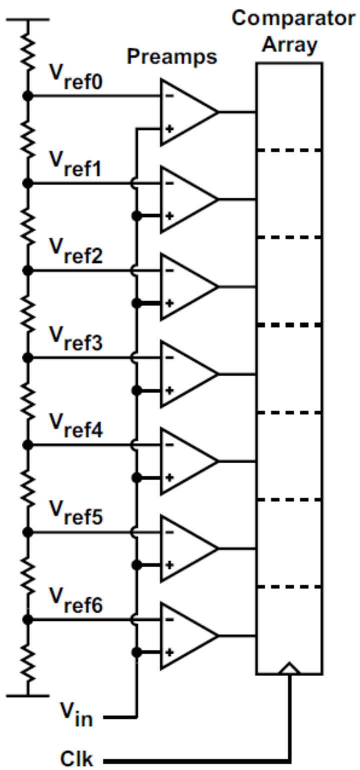
Doubling OSR adds 9dB of SQNR
Like a first order SigmaDelta

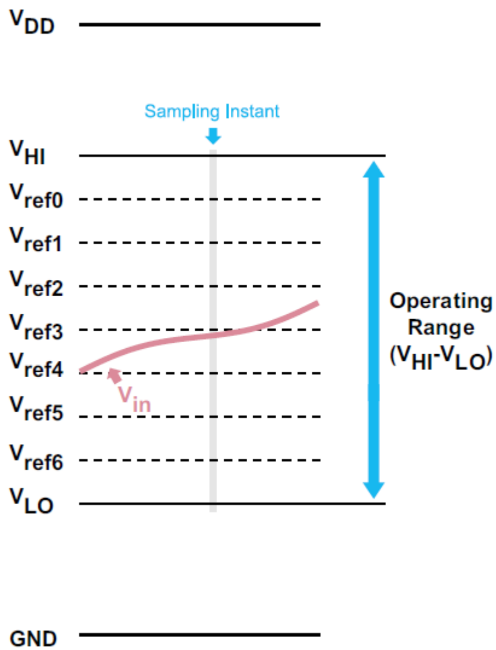
- First Order Noise Shaping for both Q and mismatch
- Quantization noise is white and performance then is enhanced by oversampling

Time domain quantizers in ADC

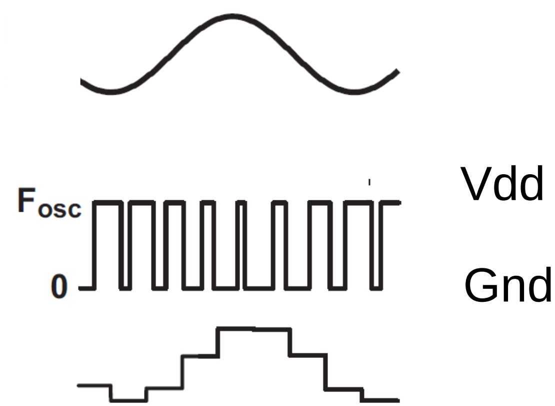
Multi-bit quantization using

(1) conventional Flash voltage quantizer





(2) Time Domain Quantizer

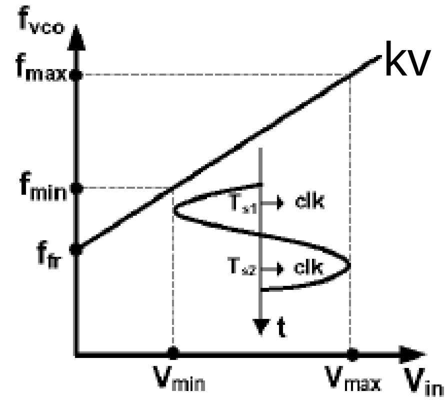


Motivation for TDC as ADC

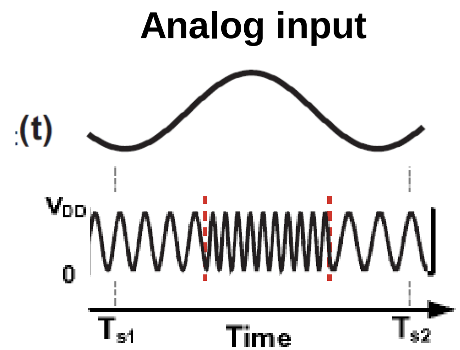
Detecting an edge transition from gnd to Vdd is easier than a voltage step of Vdd/(2^N)

3)VCO-based ADC principle

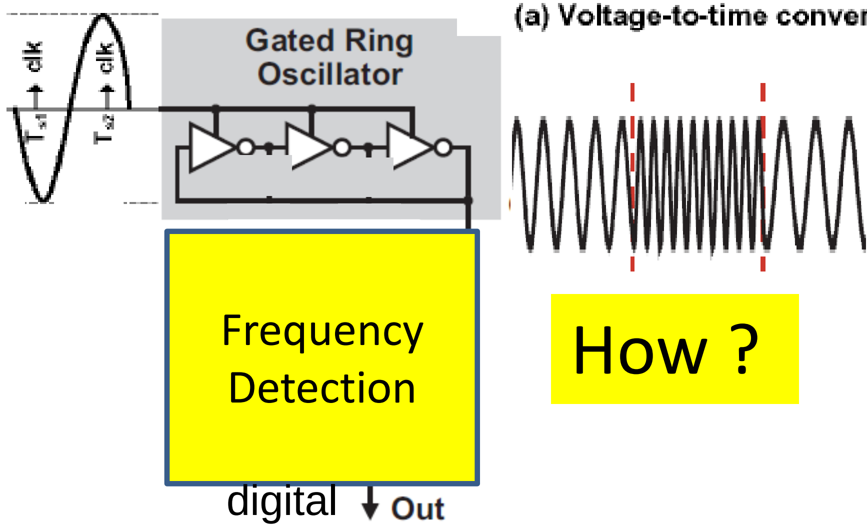
May be seen as two Operations:
- Voltage to frequency (Time) conversion
- Time to digital conversion



(a) Voltage-to-time conversion



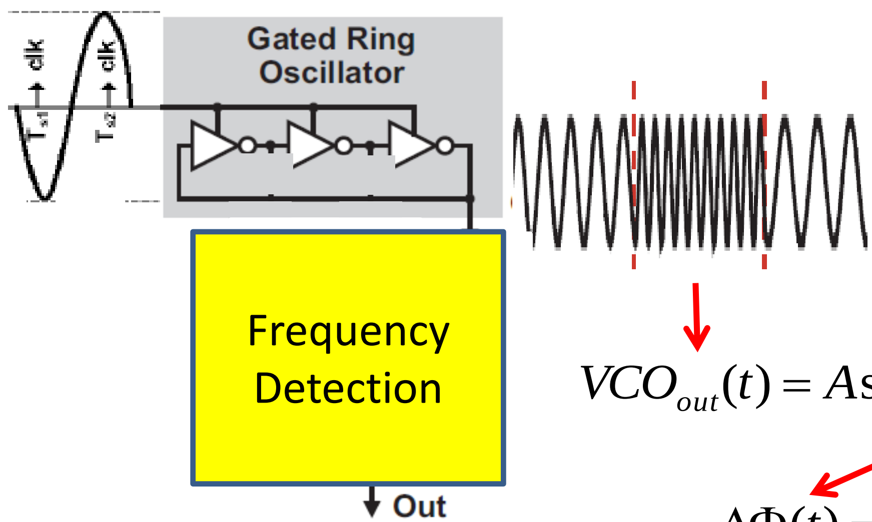
(b) VCO output in time domain



How ?

Differences with gated ring oscillator
- The enable signal replaced by analog continuous voltage to be converted
- The oscillator is always running since the input is continuously varying

3)VCO-based ADC principle



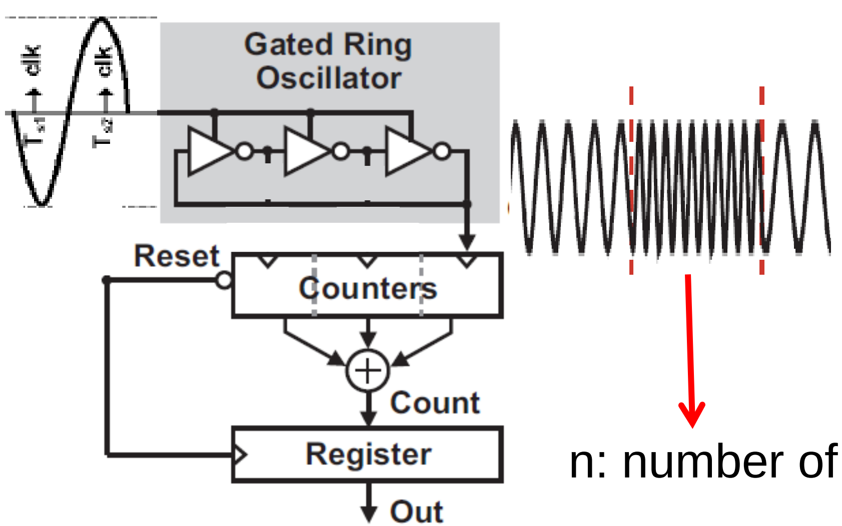
$$VCO_{out}(t) = A\sin(2\pi\int(K_v v_{tune}(t) + f_{fr})dt)$$

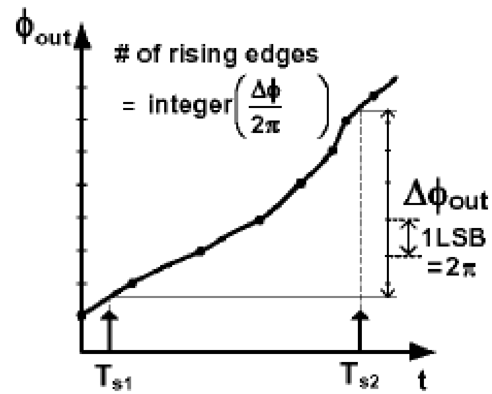
$$\Delta\Phi(t) = 2\pi\int(K_v v_{tune}(t))dt$$

$$f_{VCO} = \frac{\Delta\Phi(t)}{\Delta t} = \frac{d}{dt}(2\pi\int(K_v v_{tune}(t))dt)$$

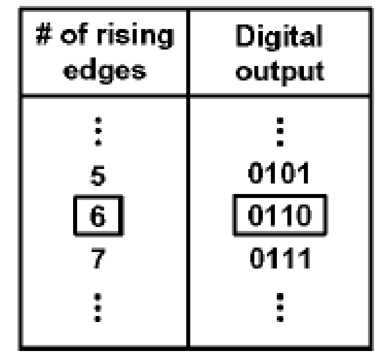
How to implement this ?

3)VCO-based ADC operation





(c) Phase quantization



(d) Digital code generation

n: number of rising edges

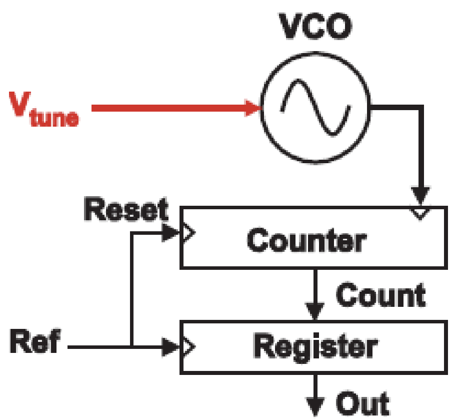
$$\Delta\Phi(t) = 2\pi * n$$

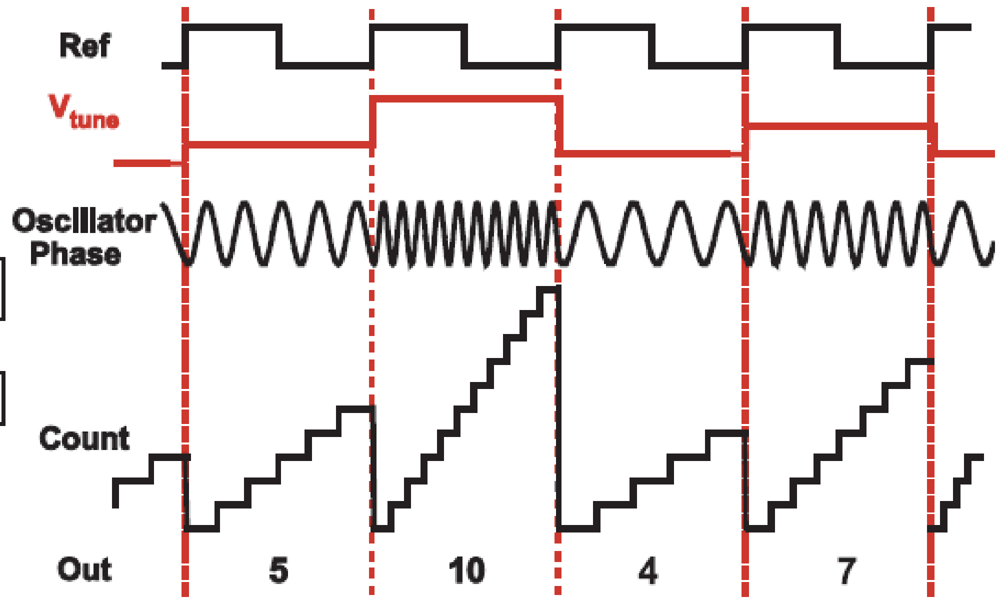
Quantization step (LSB) = 2π

$$f_{VCO} = \frac{\Delta\Phi(t)}{\Delta t} = \frac{\Delta\Phi(t)}{T_S} = \Delta\Phi(t)\, f_S$$

Quantized ← $f_{VCO} = 2\pi * f_S * n$

3a)Single phase VCO-based Quantizer





N: number of rising edges

$$f_{VCO} = K * n$$

Quantization step (LSB) = 2π

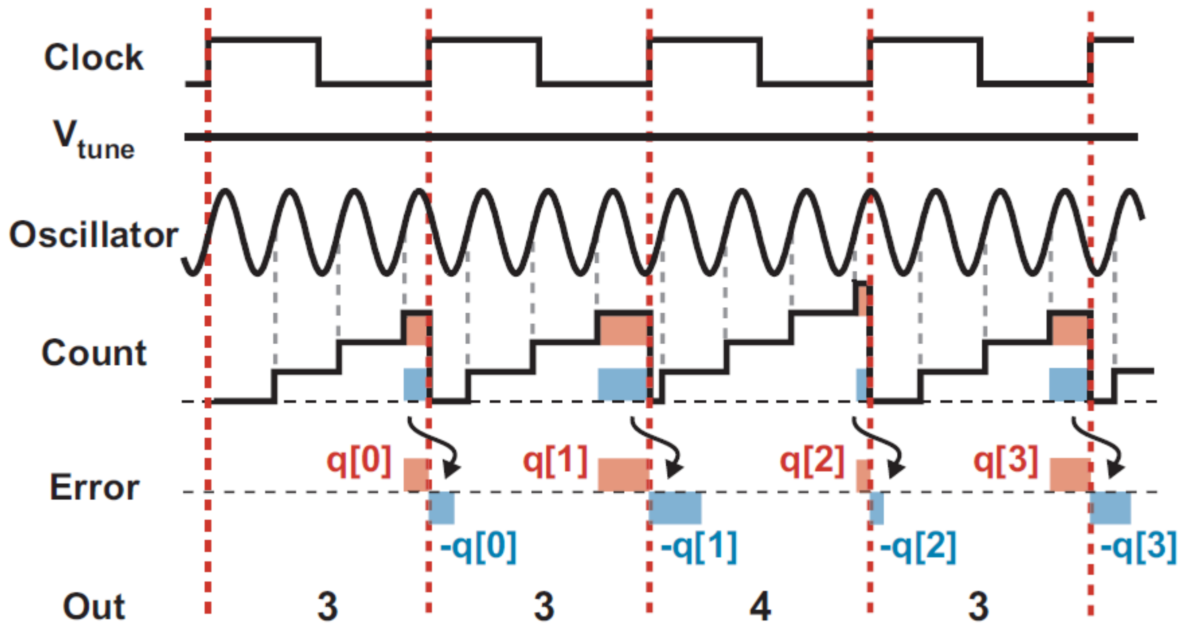
$$f_{VCO} = 0, fs, 2*fs, \ldots, (2^{N}-1)*fs$$

For high resolution, Fvco gets very high to be feasible

n : quantizer resolution

Noise shaping of VCO-based Quantizer

Constant input and Output is toggling due to residual error memorization



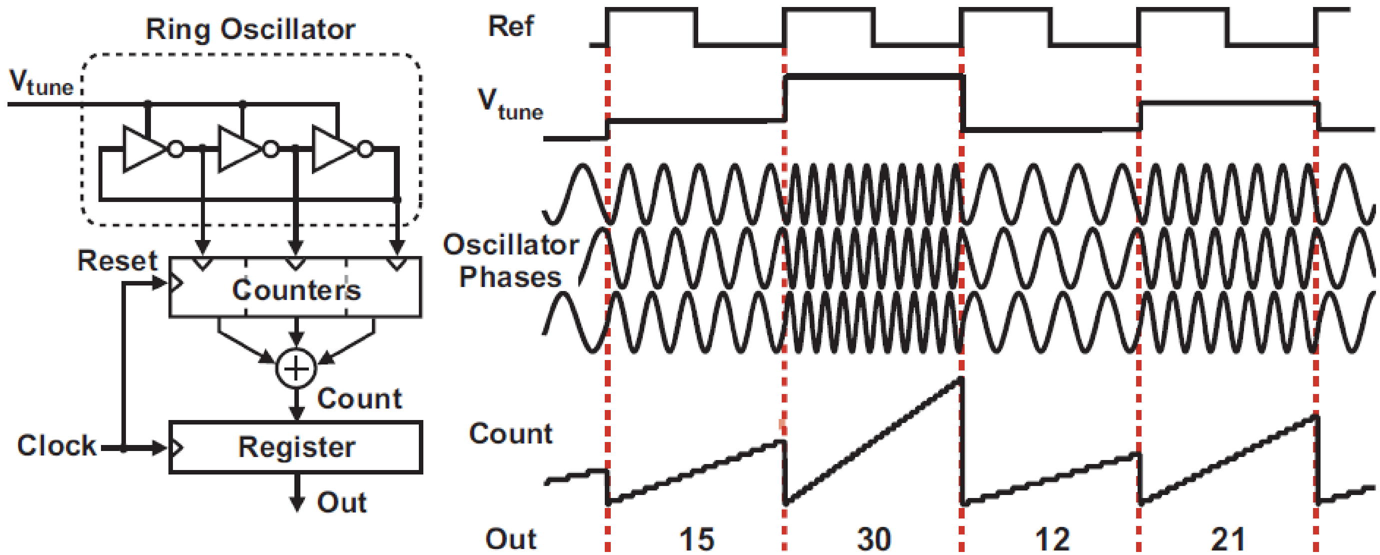
First-order noise shaping of a classical VCO-based ADC

$$Error[k] = q[k] - q[k-1],$$

Doubling OSR adds 9dB of SQNR

Like a first order Sigma Delta Modulator (SDM°

3b)Multi-phase VCO-based Quantizer



$$f_{VCO} = 0, \frac{fs}{m}, \frac{2*fs}{m}, \ldots, \frac{(2^N-1)}{m} * fs$$

n : quantizer resolution
m: inverter stages

$$f_{VCO} = K_2 * n \qquad K_2 = (2\pi/m) * f_S$$

Quantization step (LSB) = $(2\pi/m) * fs$

Selecting m= 2^N-1 → fvco_max=fs

3b)Multi-phase VCO-based Quantizer

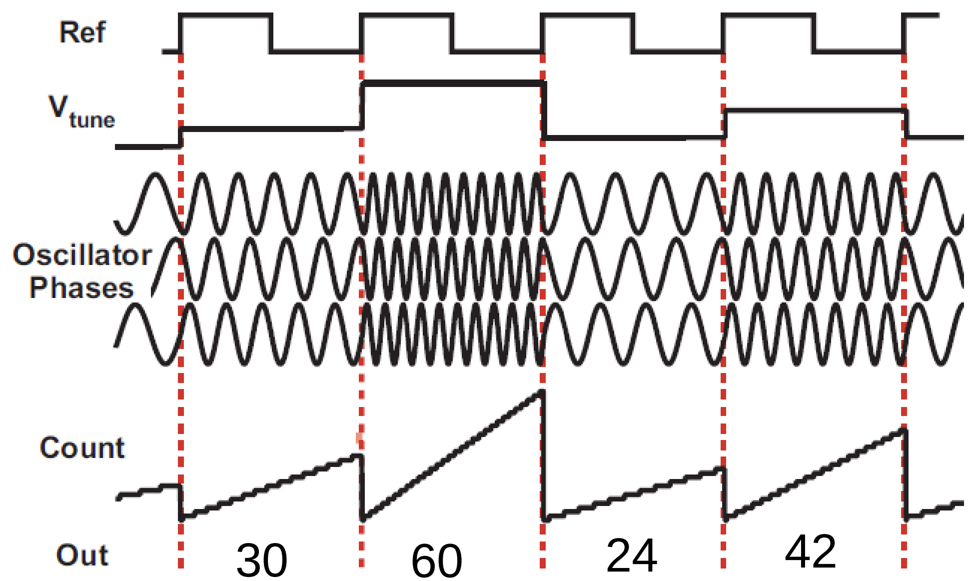
$$f_{VCO} = \frac{0xfs}{2(2^N - 1)}, \frac{1xfs}{2(2^N - 1)}, ..., \frac{(2^N - 1)xfs}{2(2^N - 1)}$$

No of inverters= $2^N - 1$

$$\mathbf{f_{vco}(max)} = \mathbf{f_s/2}$$

Further decrease f_{VCO} for the same resolution

Counting rising and falling edges

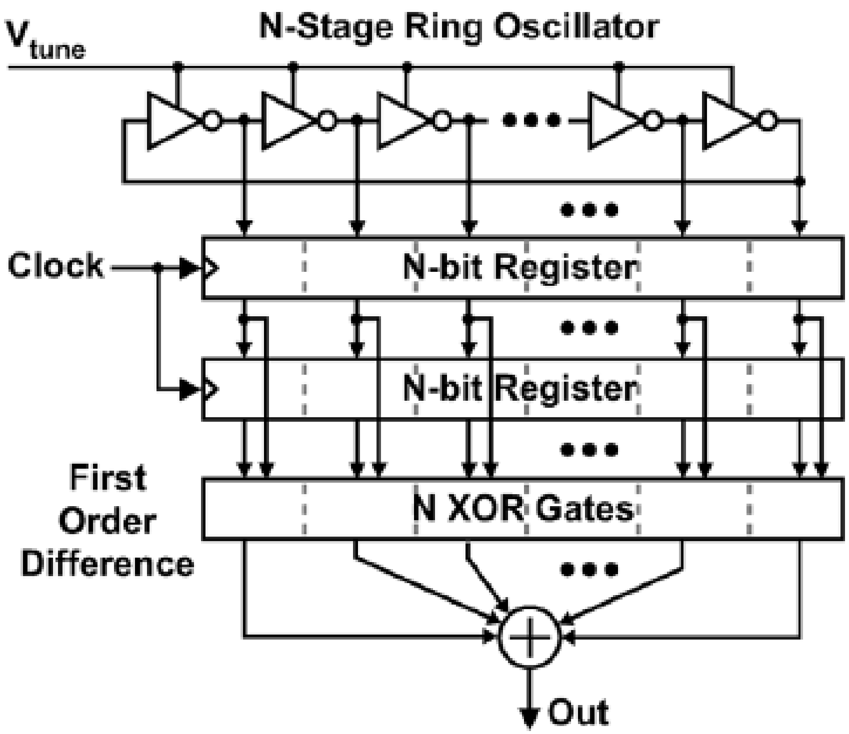


Drawbacks

1) Reset pulse can coincide with Ring Clock Pulse(Asynchronous with Reset) , Noise shaping will vanish
2) Complex implementation for higher OSR and more quantization levels (counters)

3c)Quantizer Efficient implementaion

Eliminating the Counters reset problem



$$f_{VCO} = \frac{\Delta\Phi(t)}{\Delta t} = \frac{d}{dt}\Phi(t)$$

<u>Frequency Detection</u>

Number of inverters switching state between two sampling instances is a count of the zero crossings during this time

<u>Example</u>

1 0 1 0 1 0 0 1 0

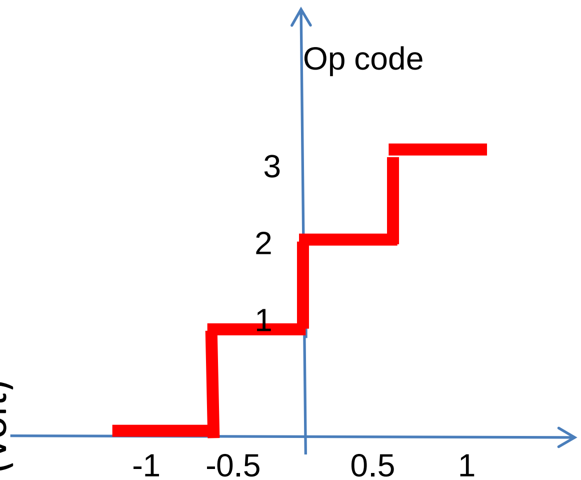
XOR

0 1 1 0 1 0 1 0 1

1 1 0 0 0 0 1 1 1

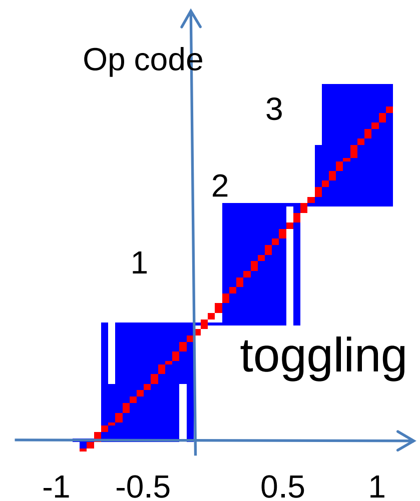
5 transitions detected by XOR

VCO-based Quantizer toggling



O/P voltage (Volt)

2-bit Flash Quantizer



2-bit VCO Quantizer

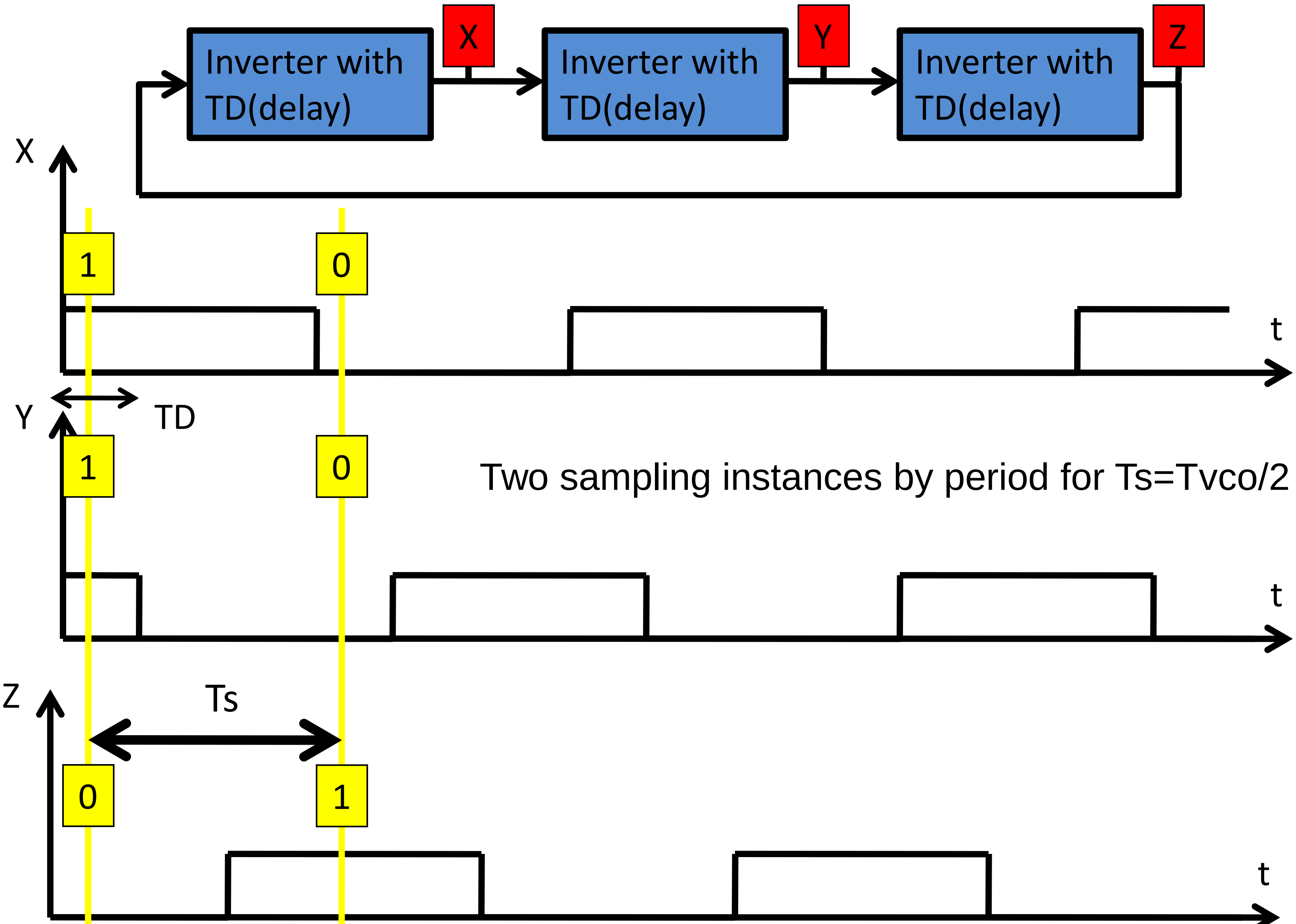
Vin	o/p code
-1 to -0.5	0
-0.5 to 0	1
0 to 0.5	2
0.5 to 1	3

Time(sec)

Vtune	Fvco	o/p(code)
-1	0	0
-1/3	Fs/6	1
1/3	Fs/3	2
1	Fs/2	3

Frequencies (k*fs/2m) have zero quantization error

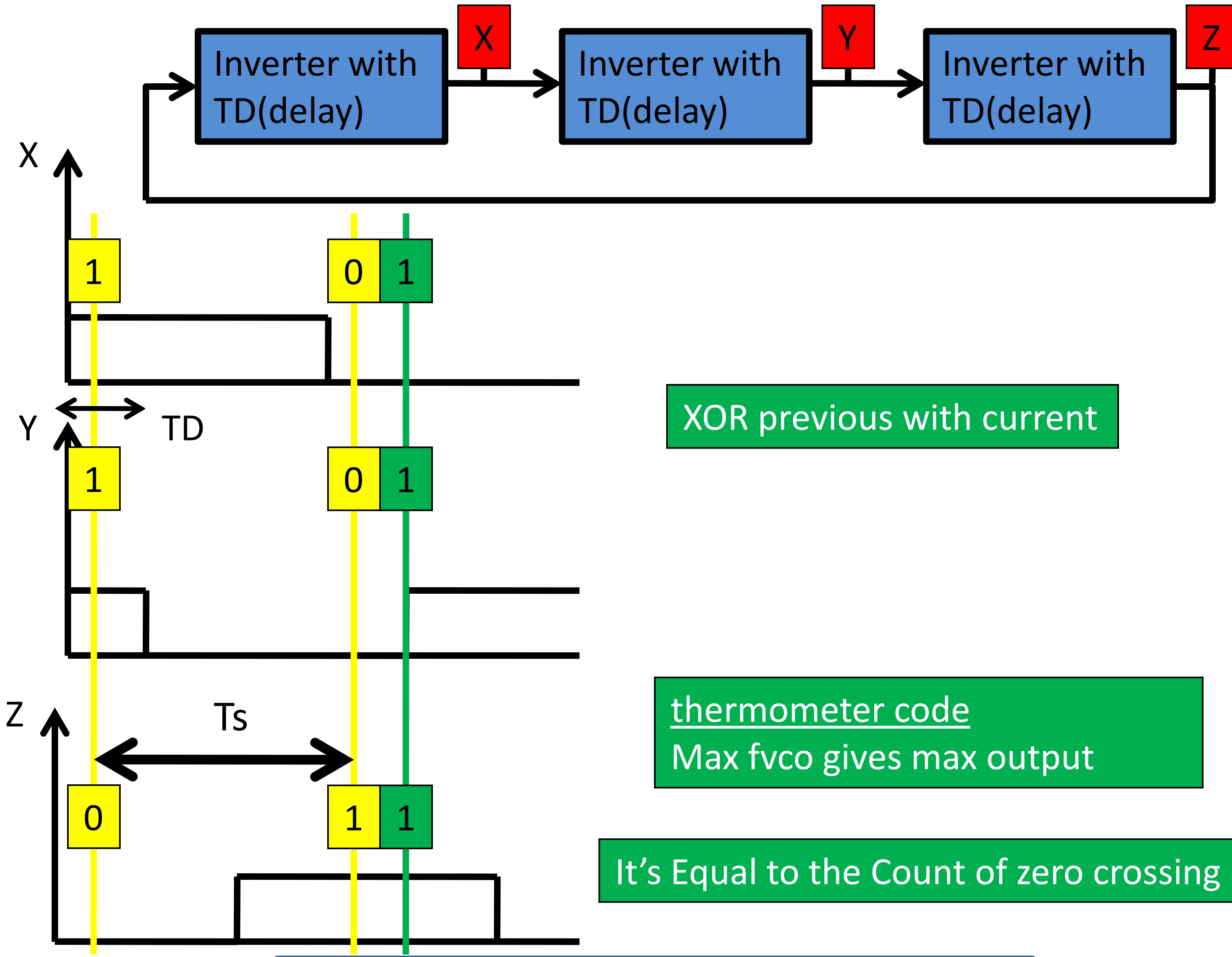
Ex1:Quantizing Vtune=1V (fvco=fs/2)



Two sampling instances by period for Ts=Tvco/2

Conversion with zero quantization error

Ex1:Quantizing Vtune=1V (fvco=fs/2)



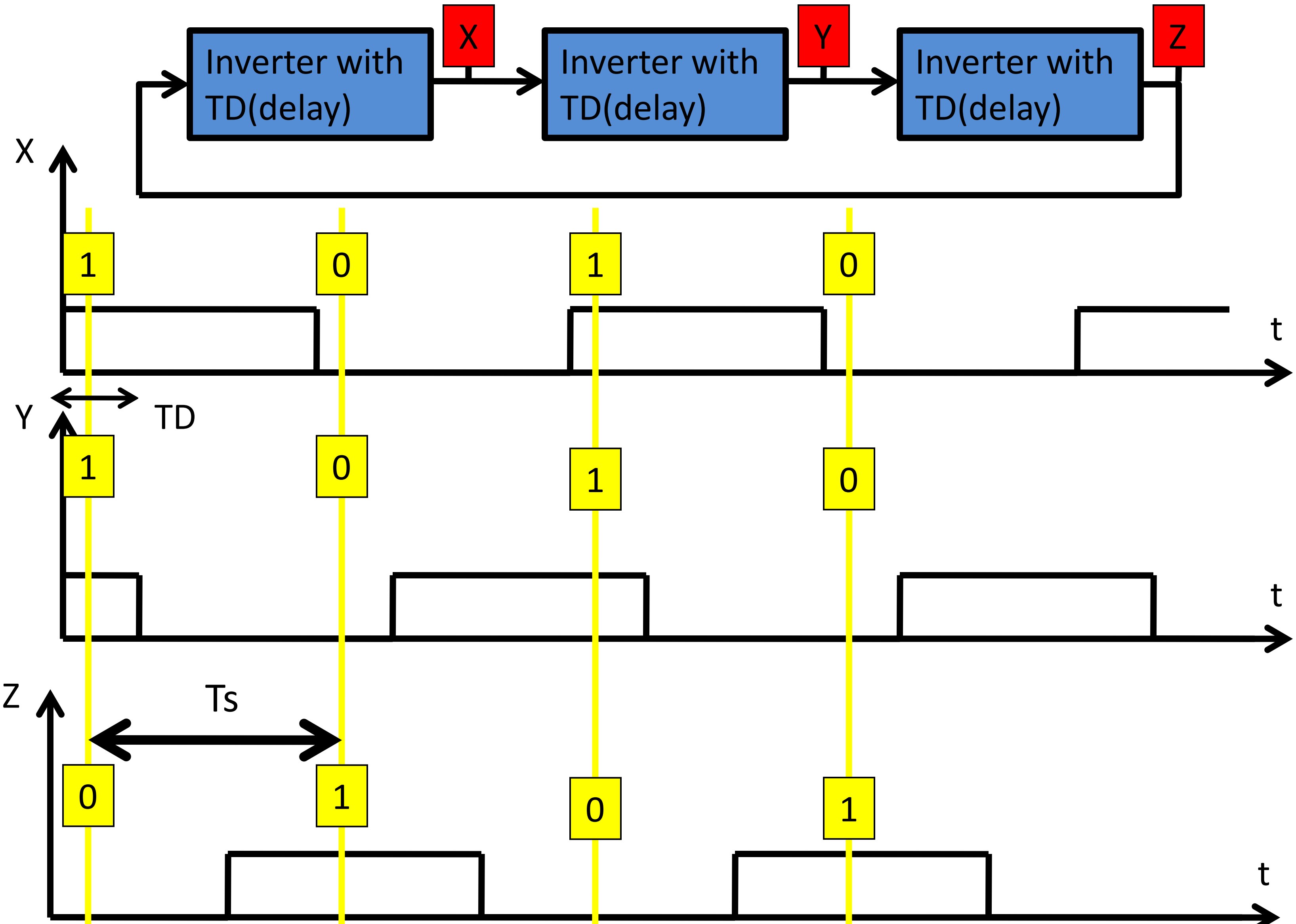
XOR previous with current

thermometer code
Max fvco gives max output

It's Equal to the Count of zero crossing

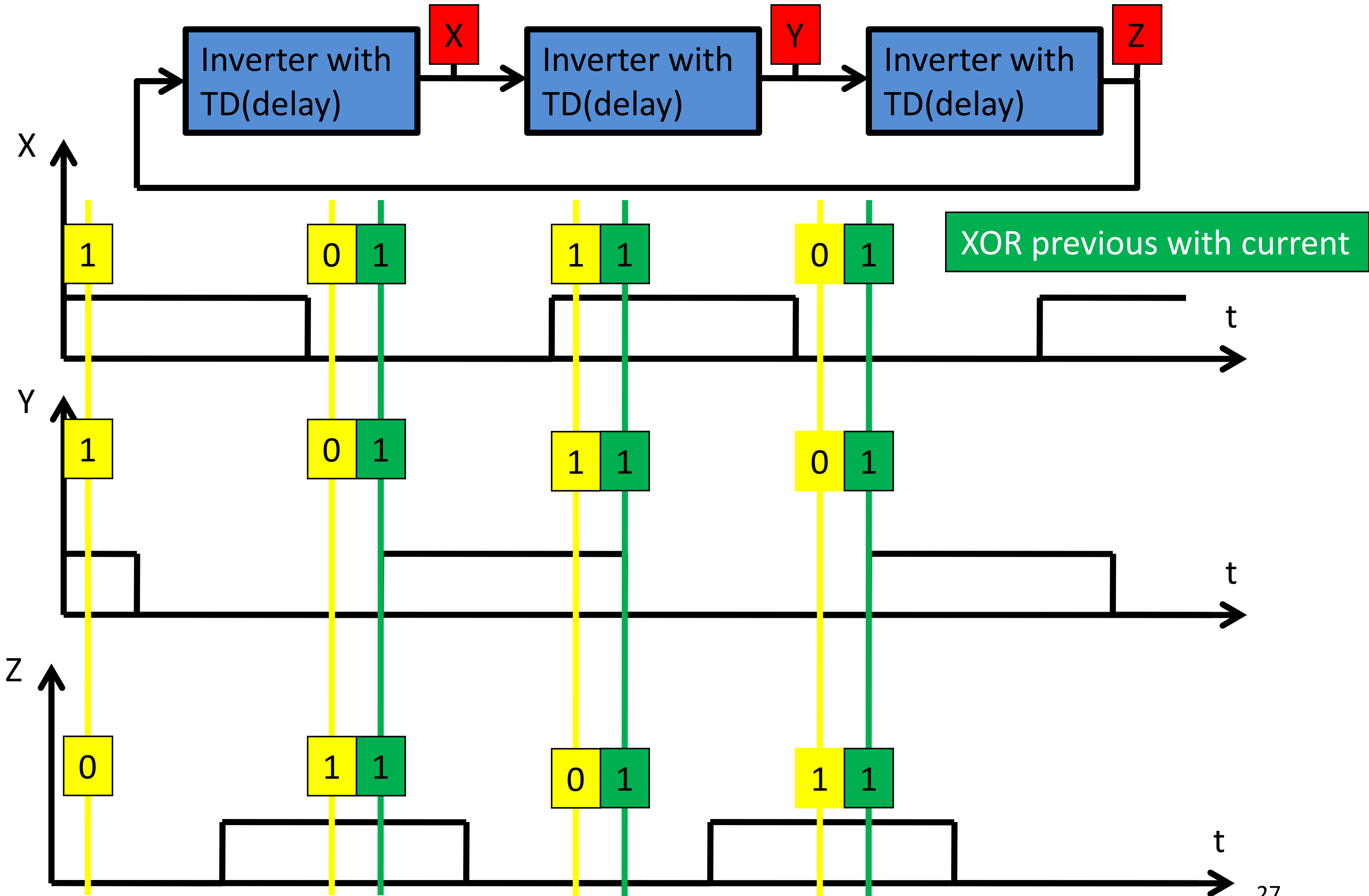
Conversion with zero quantization error

Ex1:Quantizing Vtune=1V (fvco=fs/2)



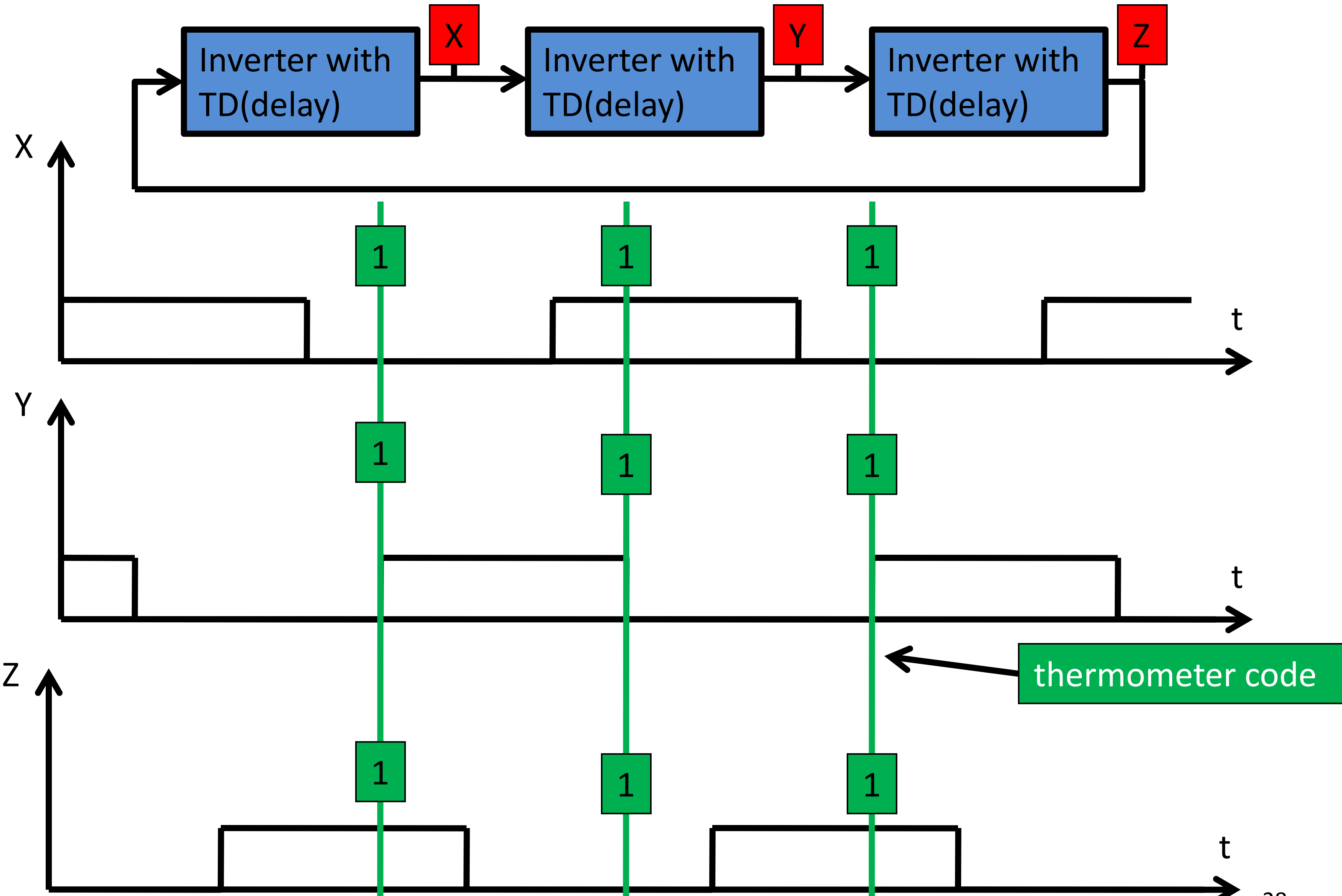
Conversion with zero quantization error

Ex1:Quantizing Vtune=1V (fvco=fs/2)



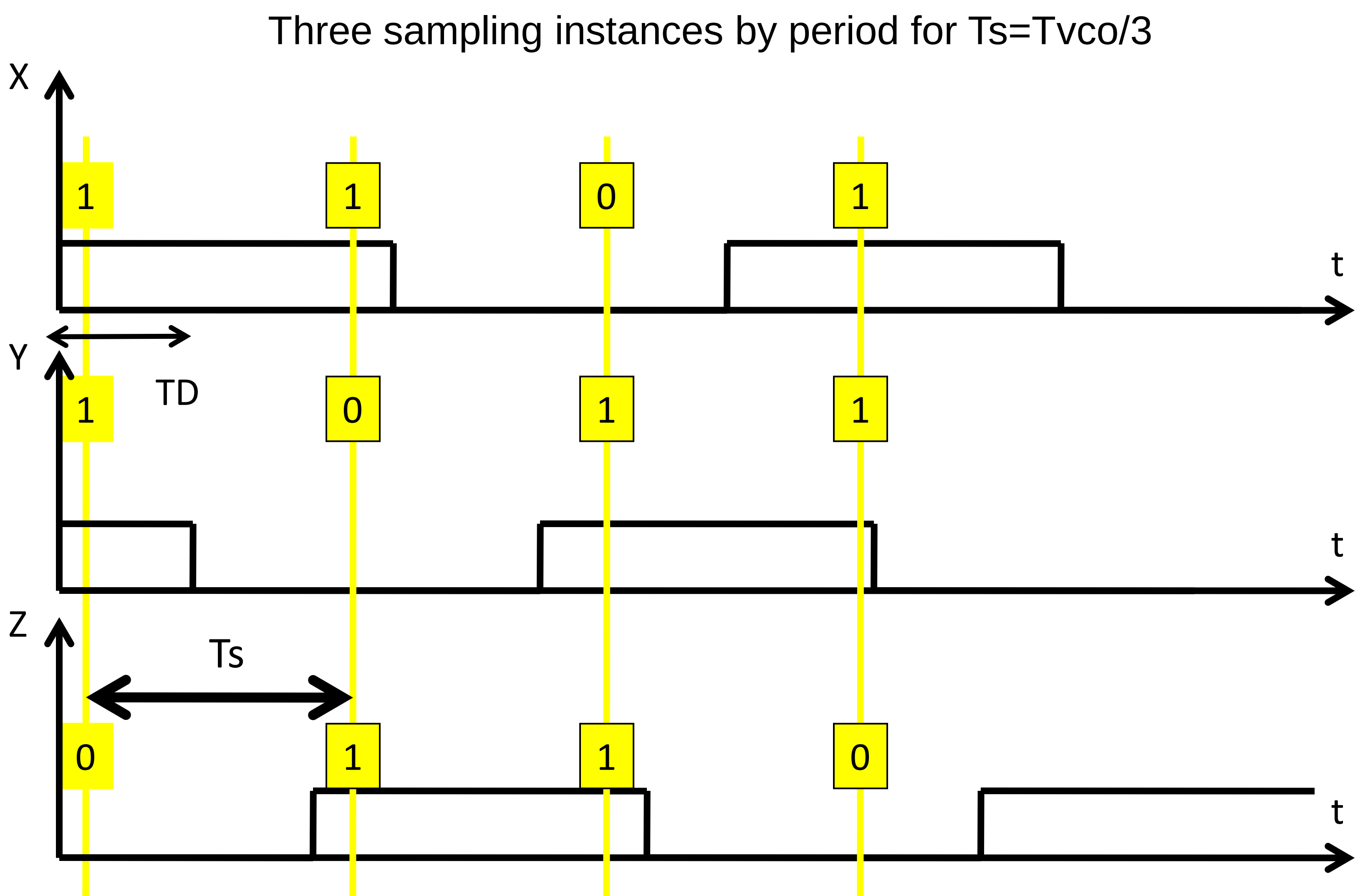
Conversion with zero quantization error

Ex1:Quantizing Vtune=1V (fvco=fs/2)



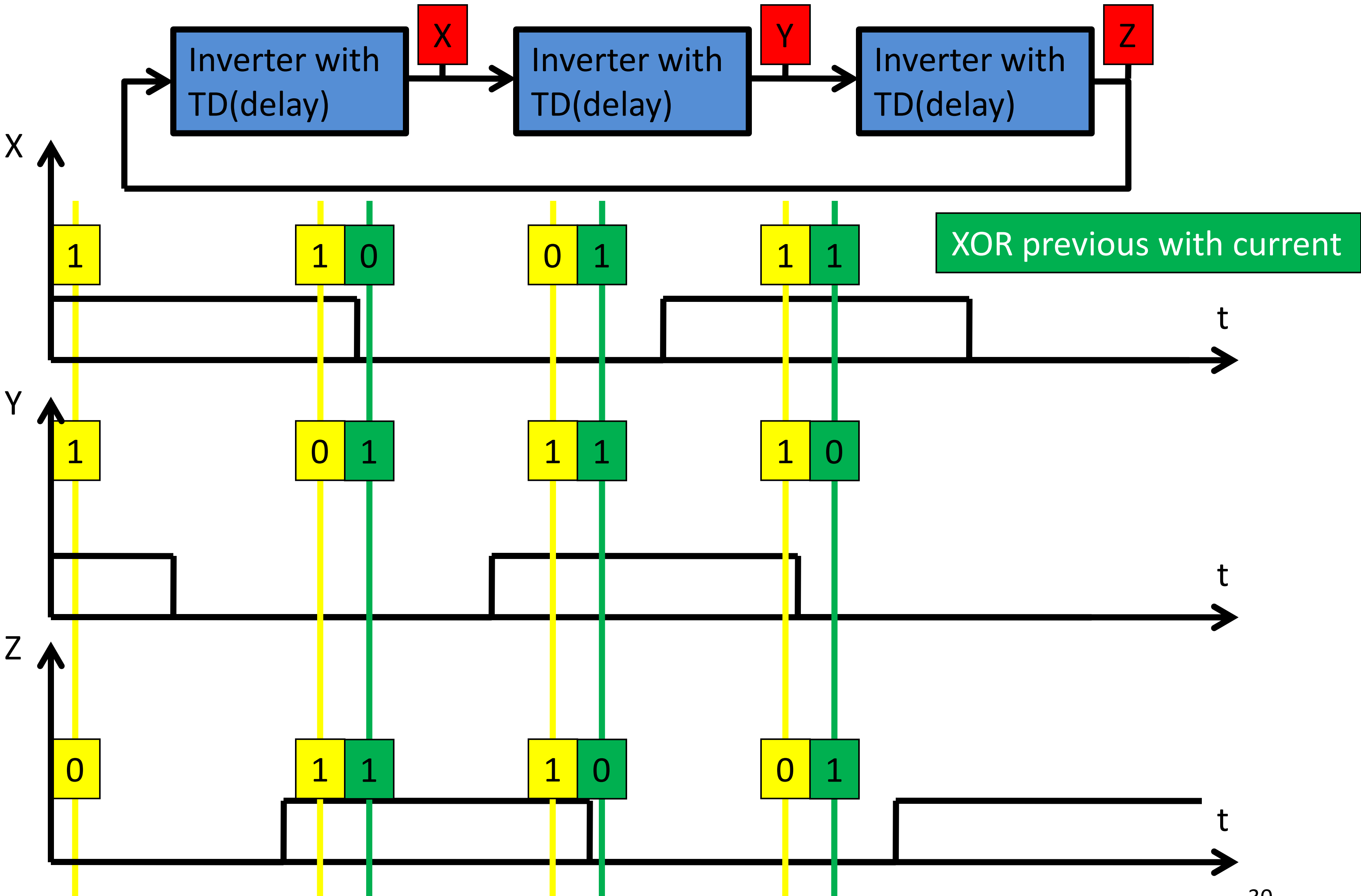
Conversion with zero quantization error

Ex2:Quantizing Vtune=1/3V (fvco=fs/3)



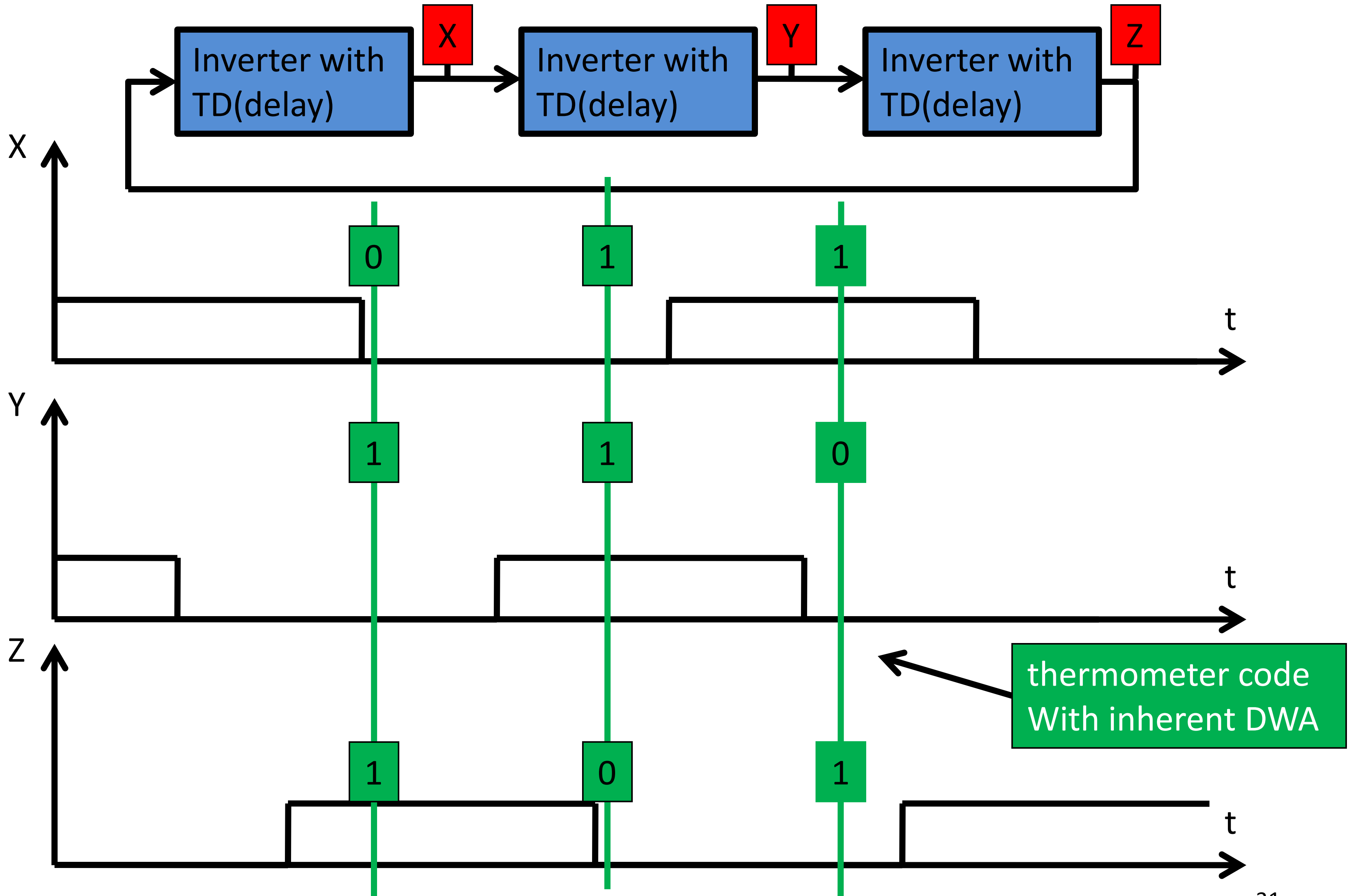
Conversion with zero quantization error

Ex2:Quantizing Vtune=1/3V (fvco=fs/3)



Conversion with zero quantization error

Ex2:Quantizing Vtune=1/3V (fvco=fs/3)

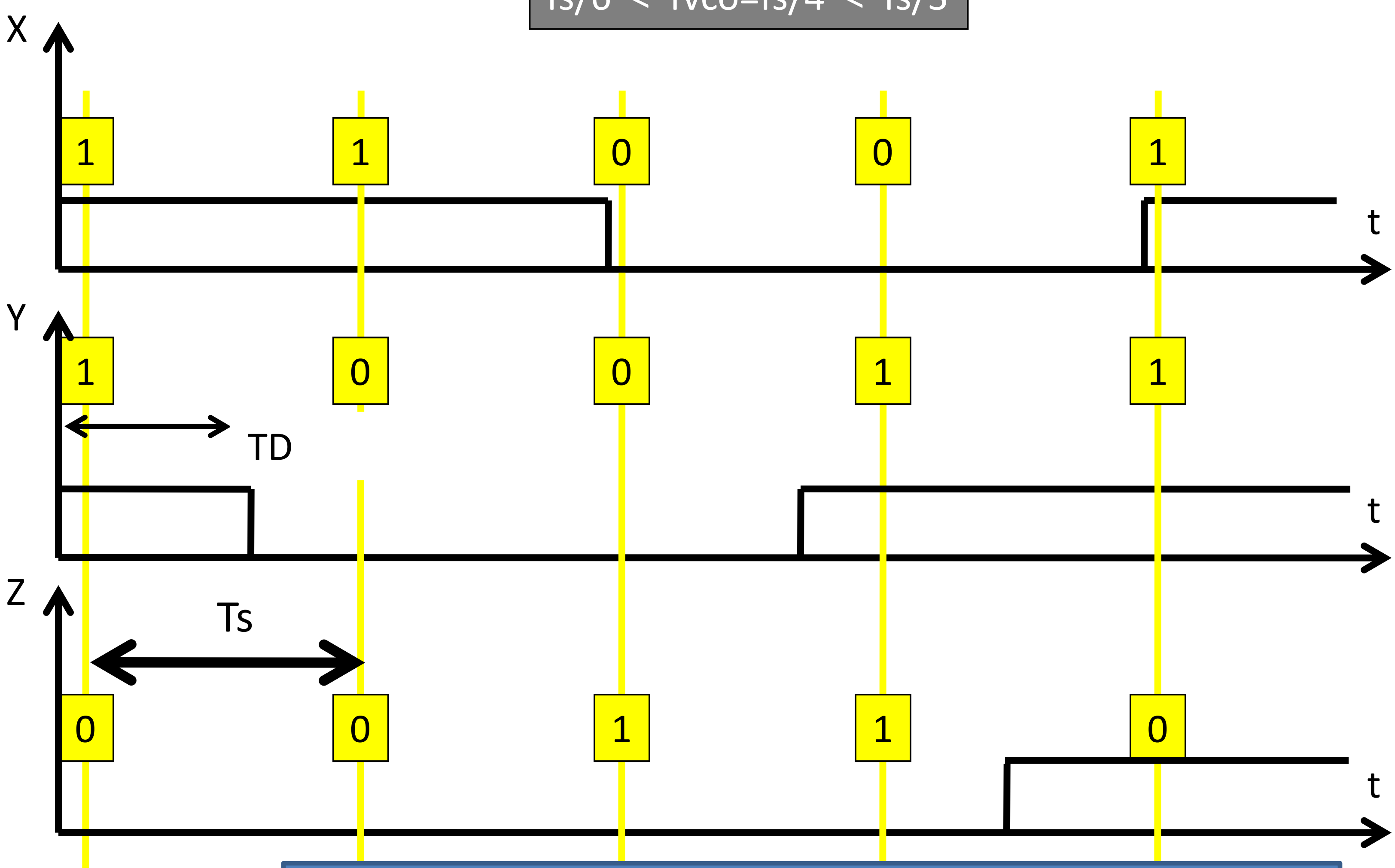


Conversion with zero quantization error

Ex3:Quantizing Vtune=1/4V (fvco=fs/4)

Four sampling instances by period for Ts=Tvco/4

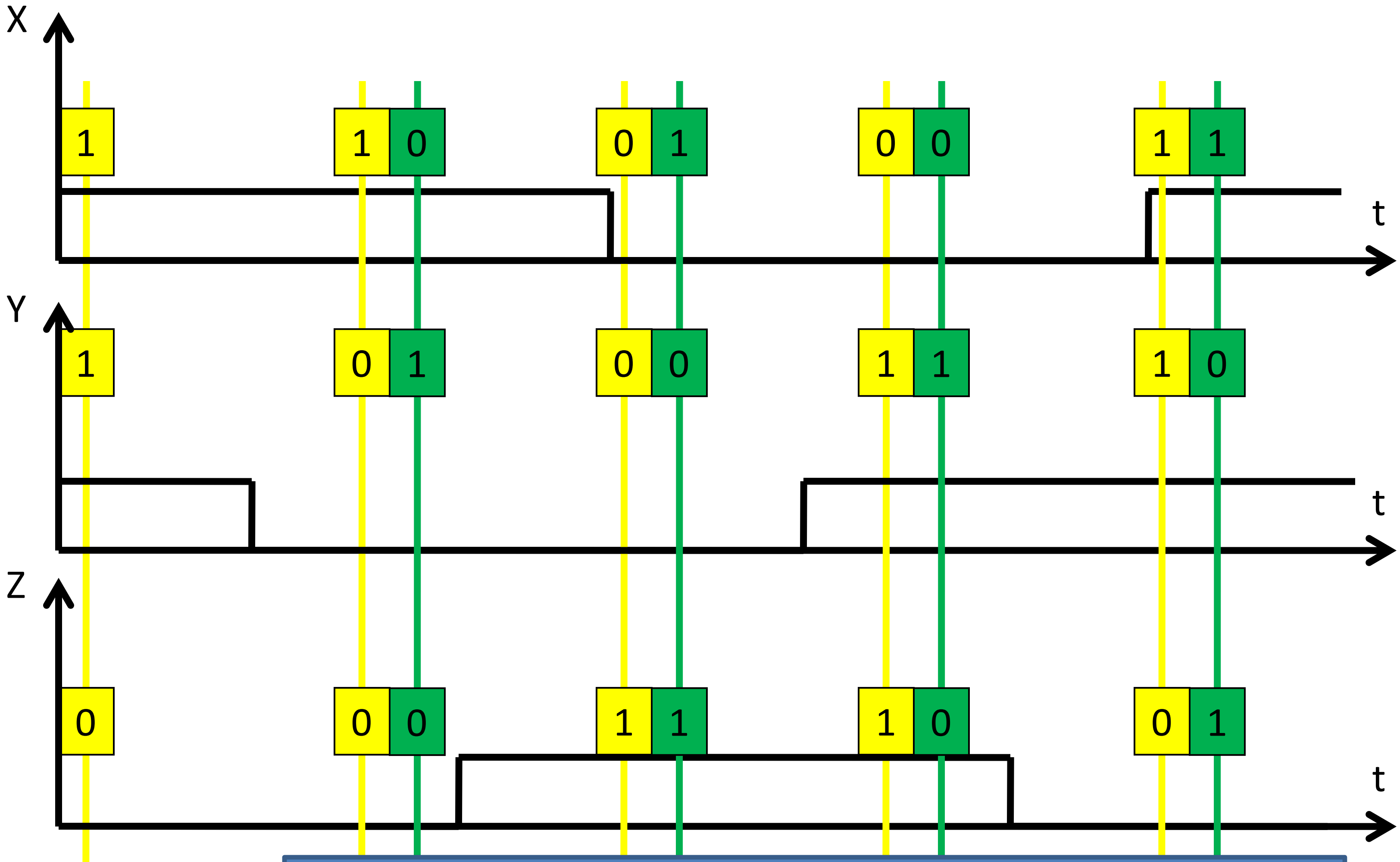
fs/6 < fvco=fs/4 < fs/3



Conversion with noise shaping for quantization error

Ex3:Quantizing Vtune=1/4V (fvco=fs/4)

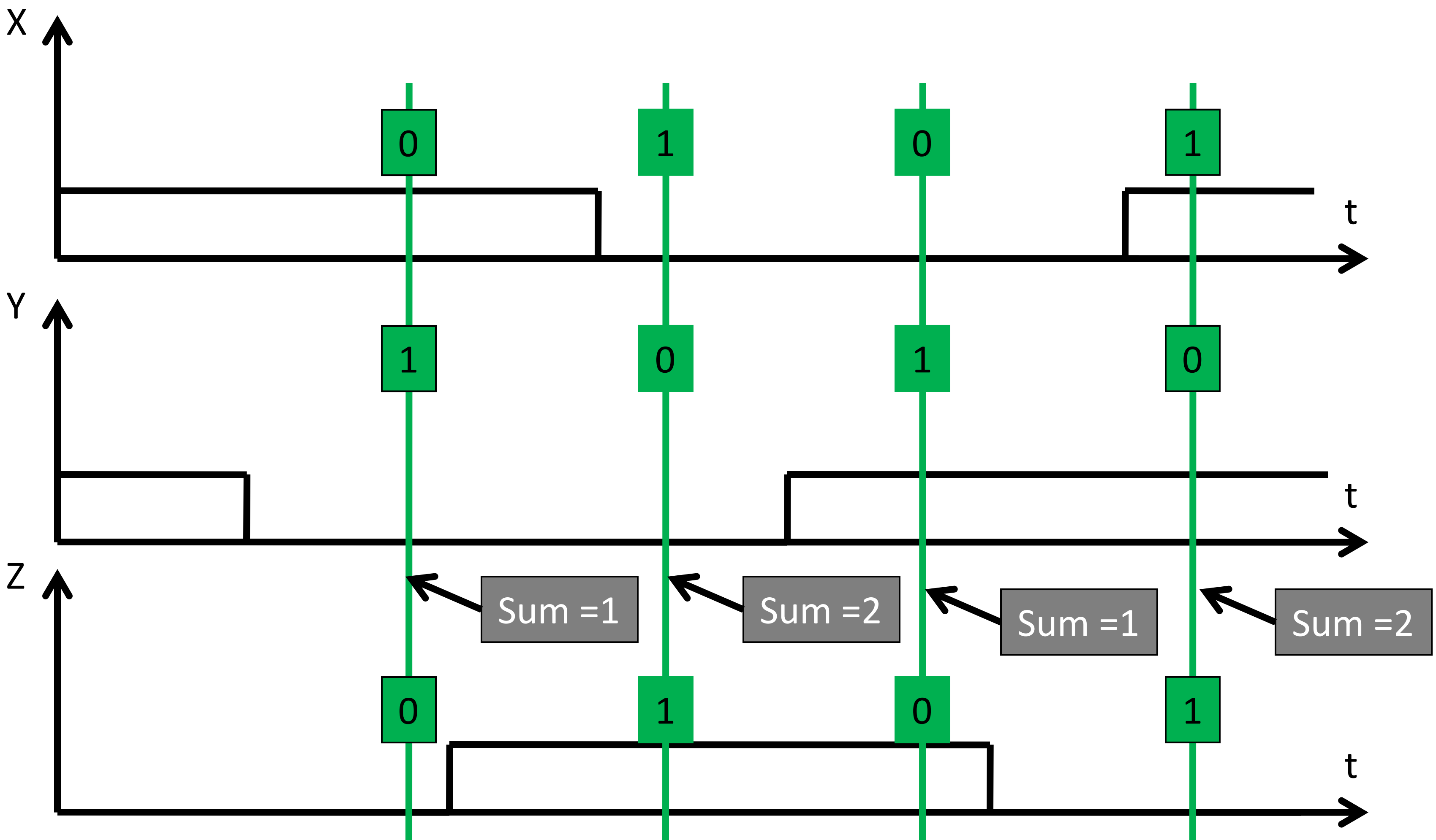
XOR previous with current



Conversion with noise shaping for quantization error

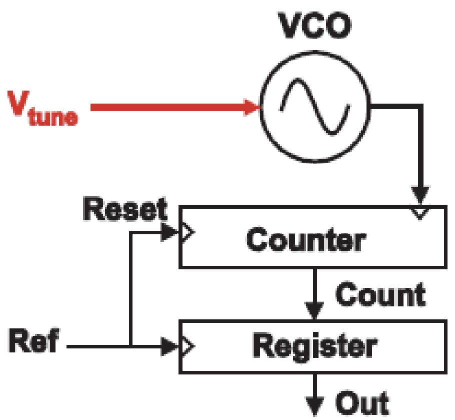
Ex3:Quantizing Vtune=1/4V (fvco=fs/4)

Noise shaping: output toggles between 2 values for a constant input



Conversion with noise shaping for quantization error

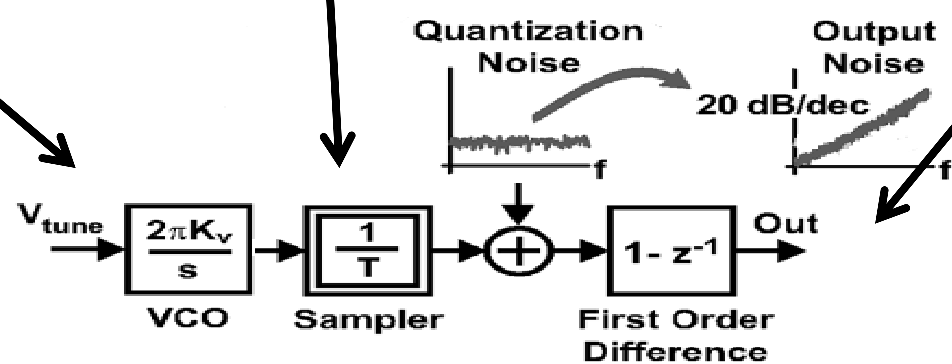
VCO-based quantizer Model



$$\Delta\Phi(t) = 2\pi\int (K_v v_{tune}(t))dt$$

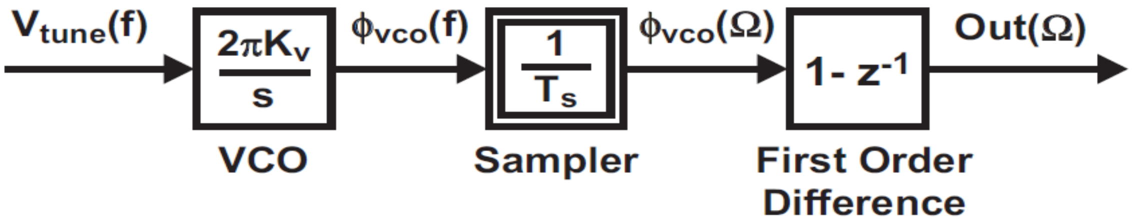
$$f_{VCO} = \frac{\Delta\Phi(t)}{\Delta t} = \frac{d}{dt}(2\pi\int (K_v v_{tune}(t))dt)$$

Vtune → Integration → Phase → Sampling → Quantized Phase → Differentiation → frequency



VCO-based quantizer Model validity

CT integrator and DT differentiator
Is it true that one is the inverse of the other ?



$$1 - z^{-1} = 1 - e^{-sT_S}$$

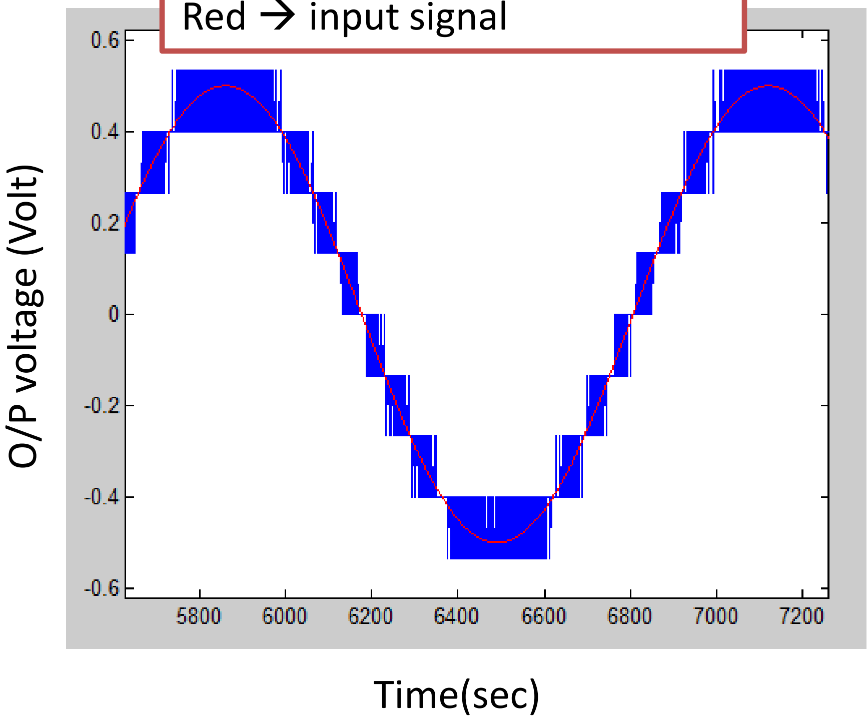
$$= 1 - \left(1 + \frac{(-sT_S)^1}{1!} + \frac{(-sT_S)^2}{2!} + \frac{(-sT_S)^3}{3!} + \ldots\ldots\right)$$

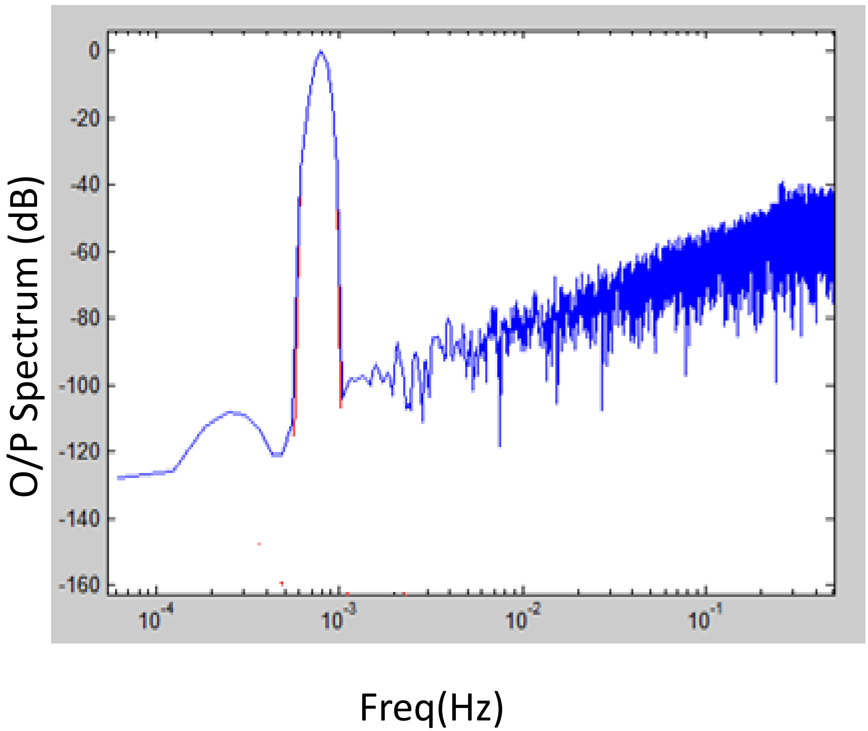
$$\approx sT_S$$ ⇒ $\omega \ll F_s.$

DT differentiation may be approximated as the inverse of the CT integration
Only for low frequencies with respect to Fs

VCO-based quantizer (4-bit)simulation

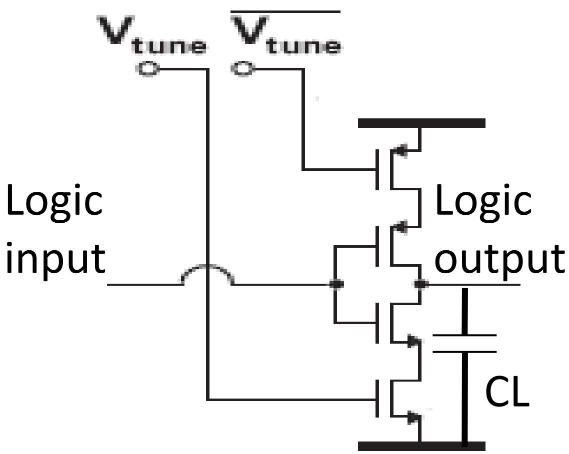
Blue→ output of quantizer
Red → input signal



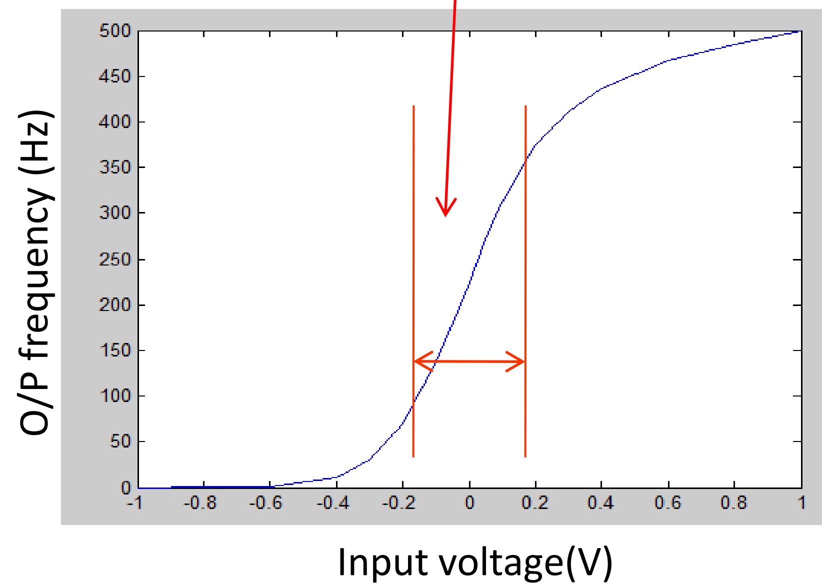


VCO-based quantizer Circuit drawbacks

VCO unit cell as two current sources



Small operation range



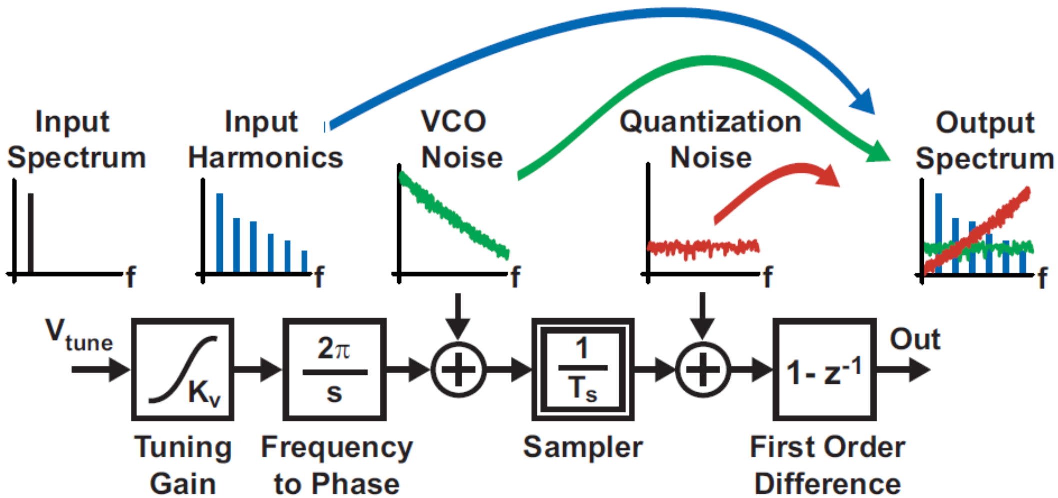
$$I_D = K(V_{gs} - V_t)^2$$

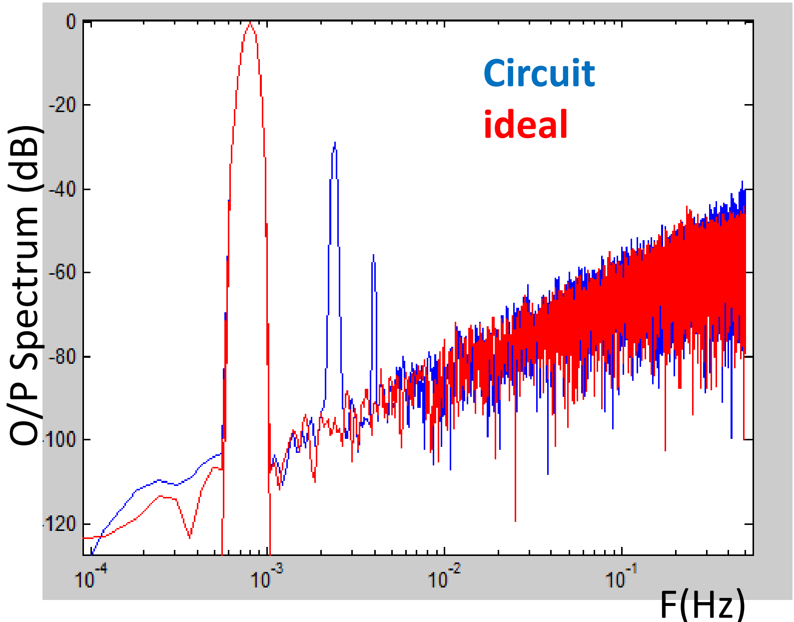
$$t_d = \frac{V_{swing} C_L}{I_D} \propto \frac{1}{V_{GS}^2}$$

$$f_{osc} = \frac{1}{2Nt_d}$$

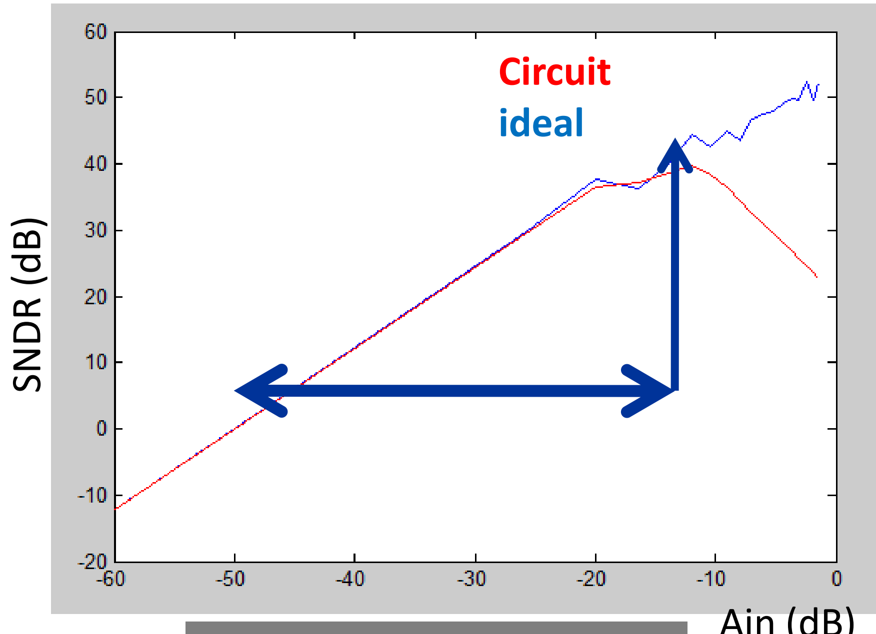
Non linear Relation and can be assumed linear on a small range

VCO-based quantizer Circuit drawbacks



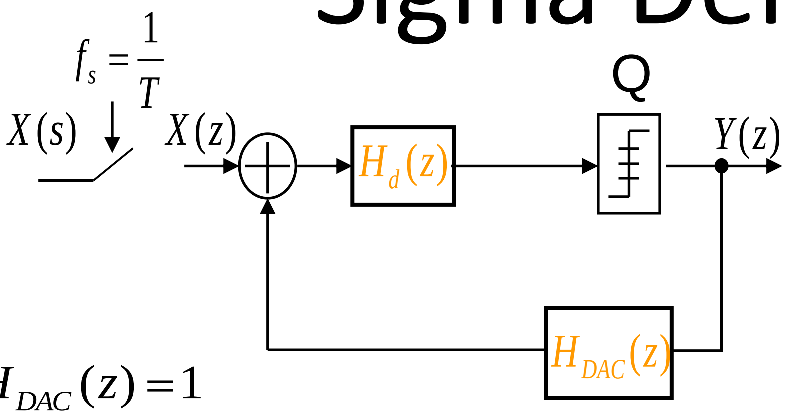


VCO-based quantizer spectrum



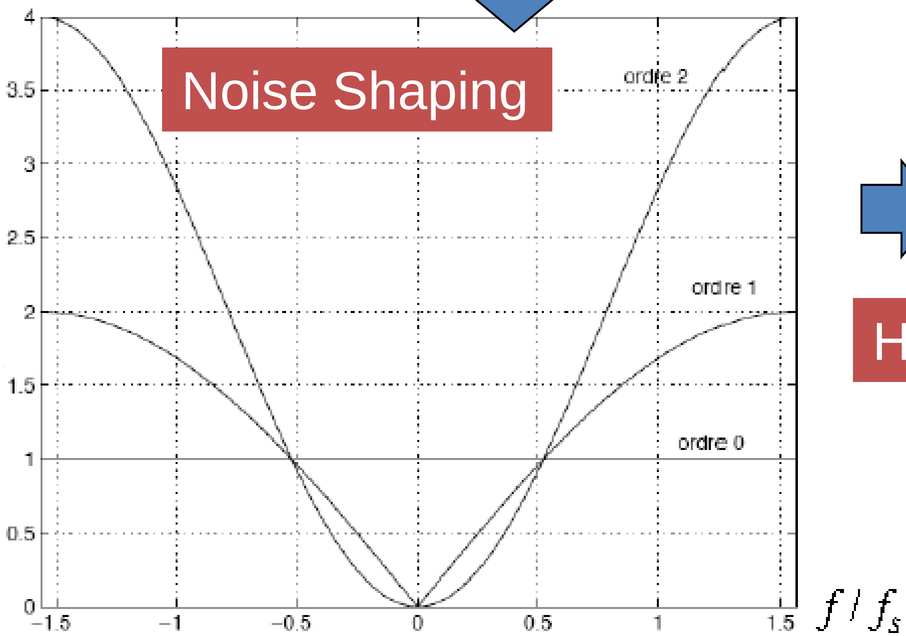
VCO quantizer(SNDR)

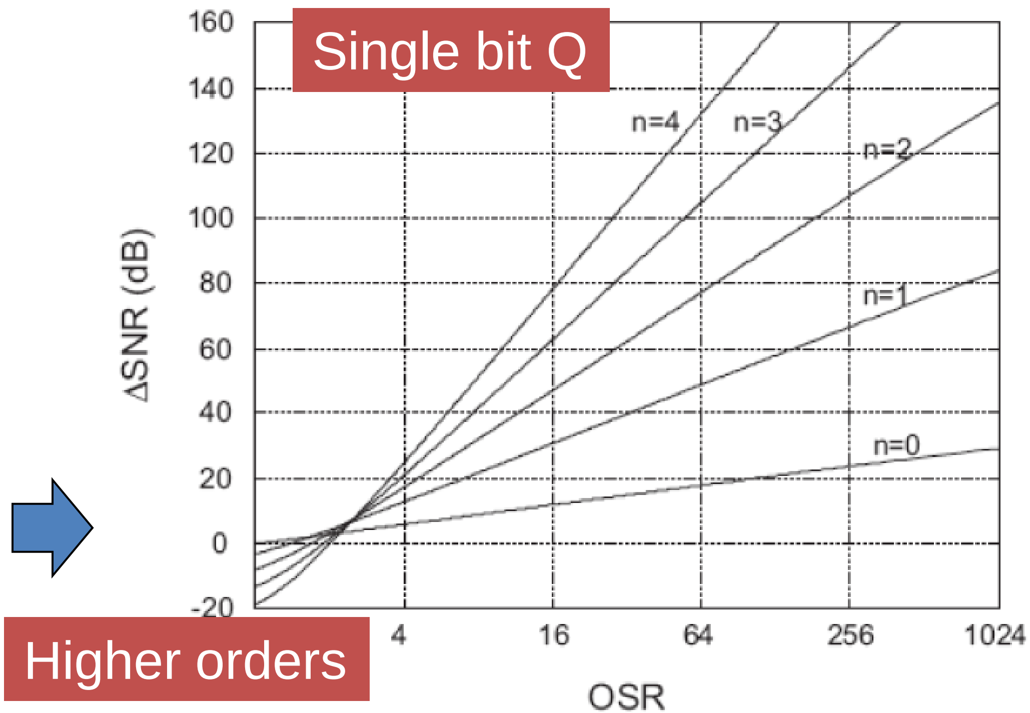
Sigma Delta ADC Review



$$H_{DAC}(z) = 1$$

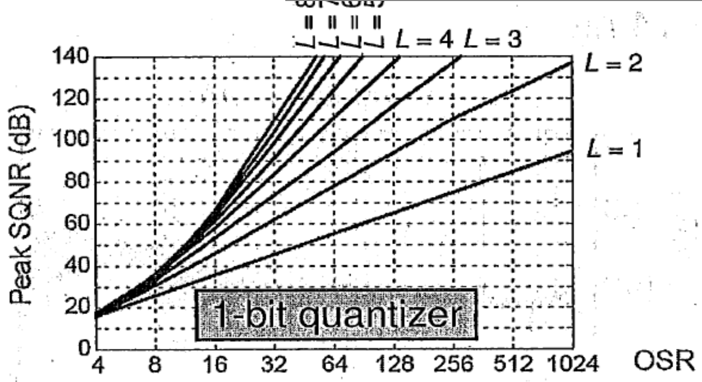
$$Y(z) = X(z)\frac{H_d(z)}{1+H_d(z)} + Q(z)\frac{1}{1+H_d(z)}$$

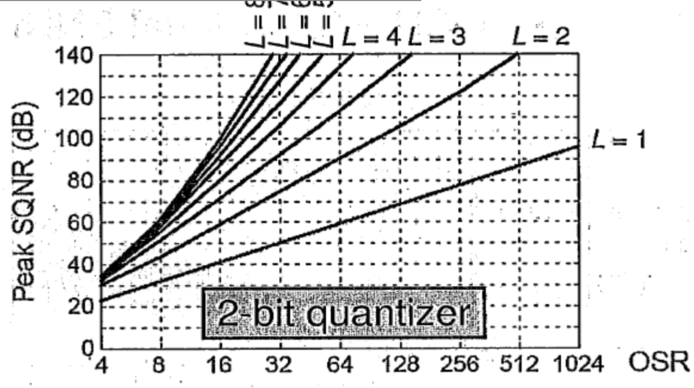


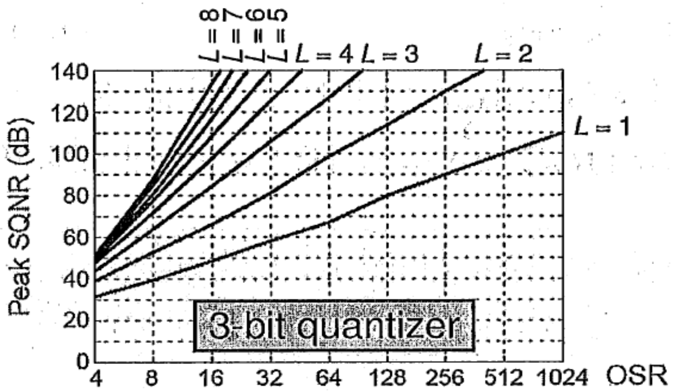


Multibit quantization

Higher SNR at lower OSR values







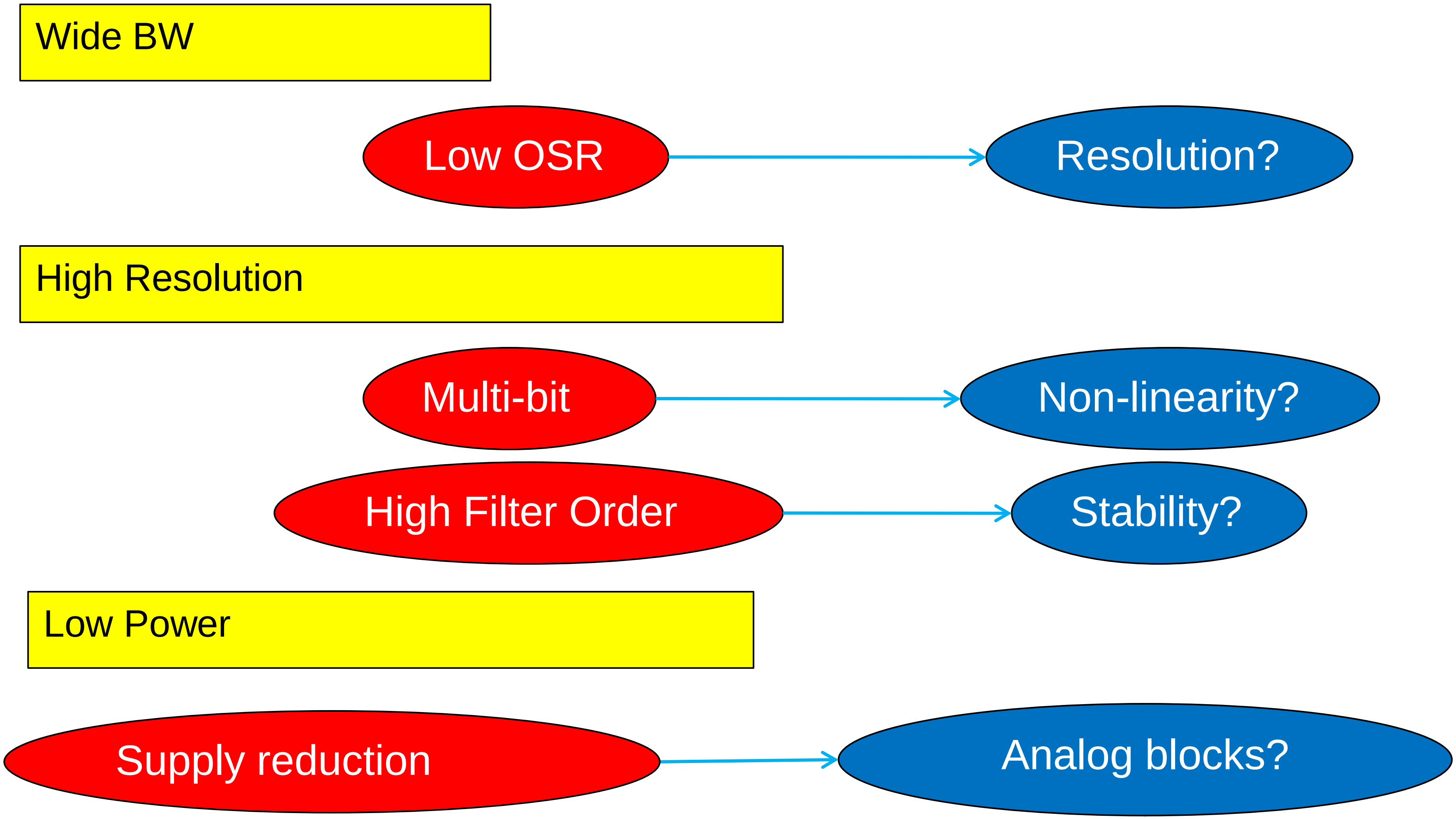
Estimated $$SNR = \frac{3}{2}\left(\frac{2n+1}{\pi^{2n}}\right)(2^{M}-1)^{2}OSR^{2n+1}$$

Order

Quantizer resolution

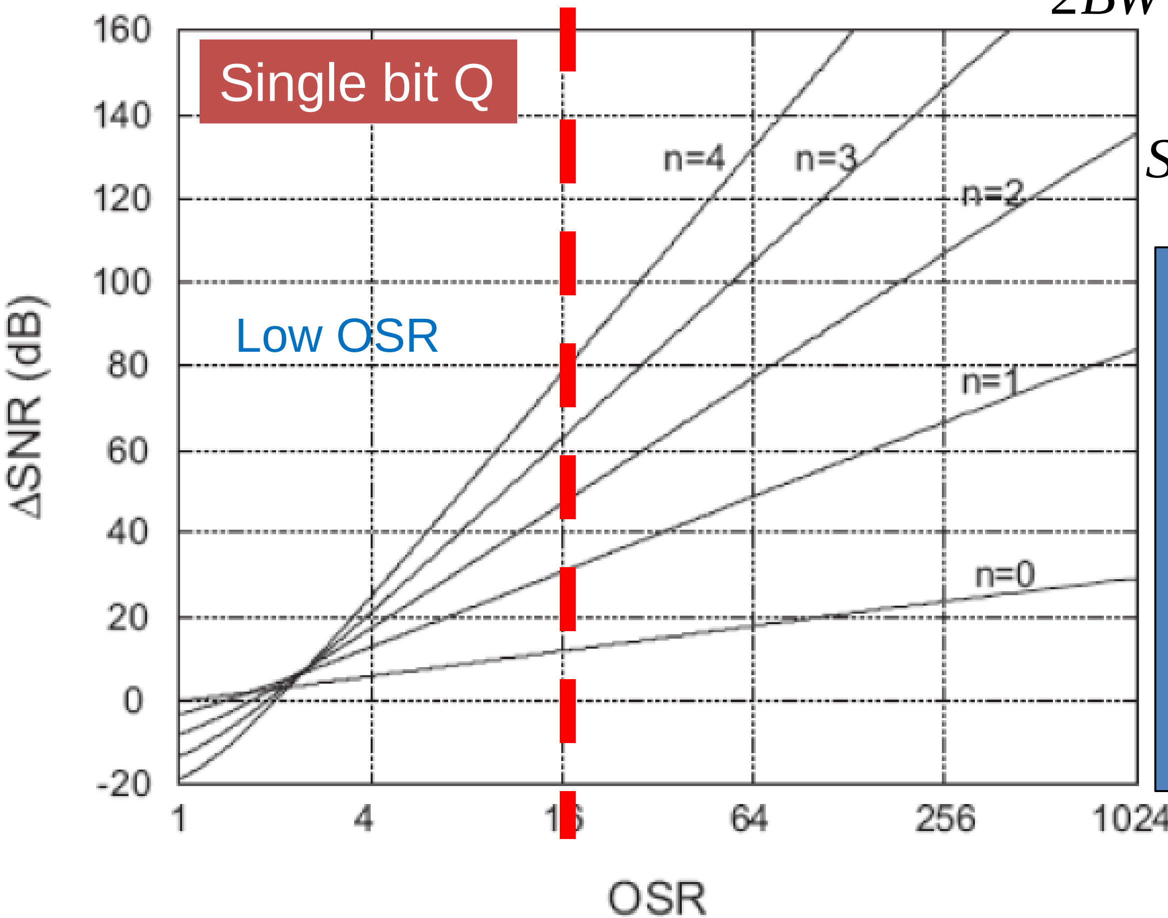
Over Sampling ratio

Sigma Delta Design challenges



Design Challenges: Low OSR

$$OSR = \left(\frac{fs}{2BW}\right)$$

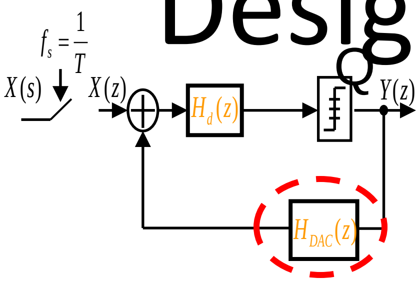


$$SNR = \frac{3}{2}\left(\frac{2n+1}{\pi^{2n}}\right)(2^M - 1)^2 OSR^{2n+1}$$

- Low OSR corresponds to lower SNR thus lower resolution

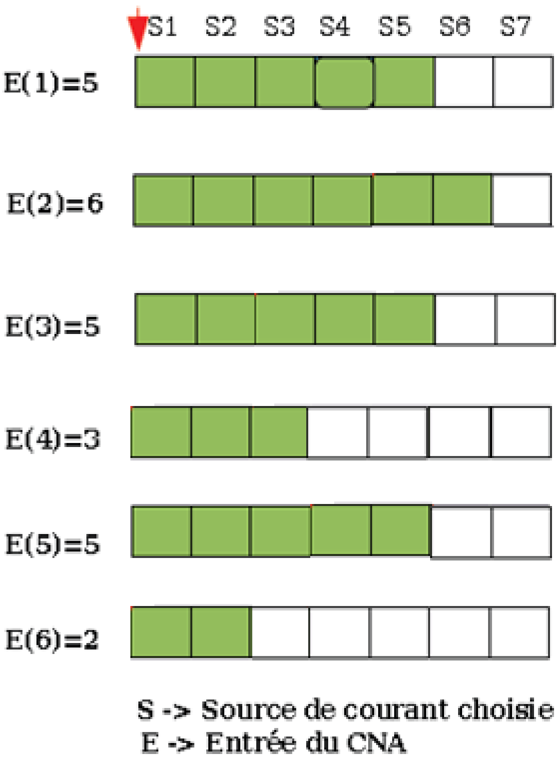
- Stabilized Single loop requires reducing NTF gain which will further decrease SNR

Design Challenge: Multibit DAC

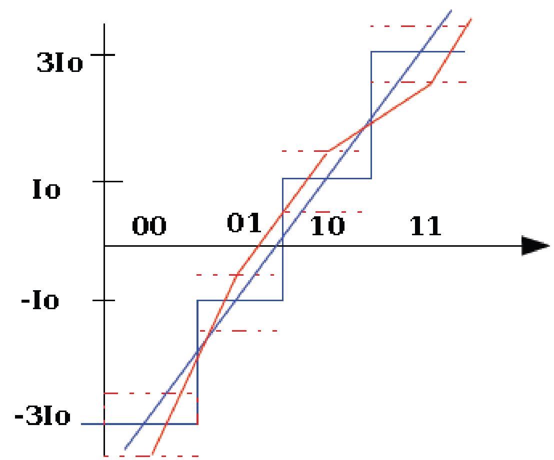


3bits DAC example

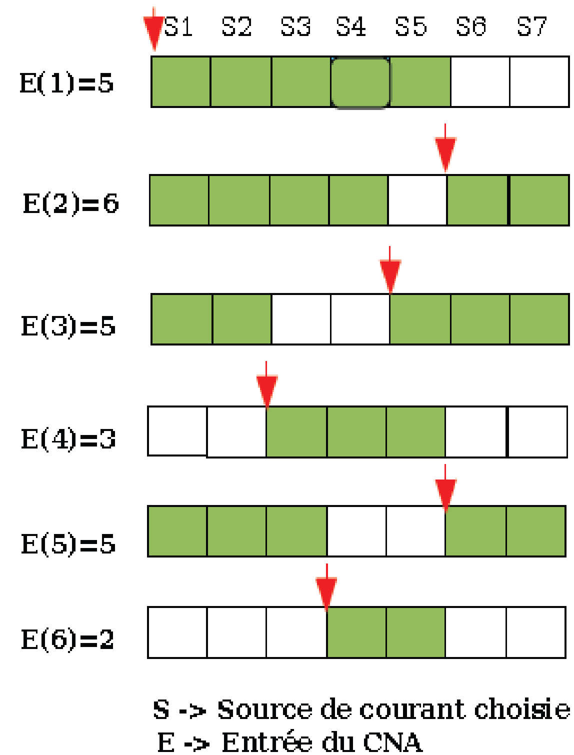
Thermometer code selecting DAC cells



Non linearity due to cell mismatch



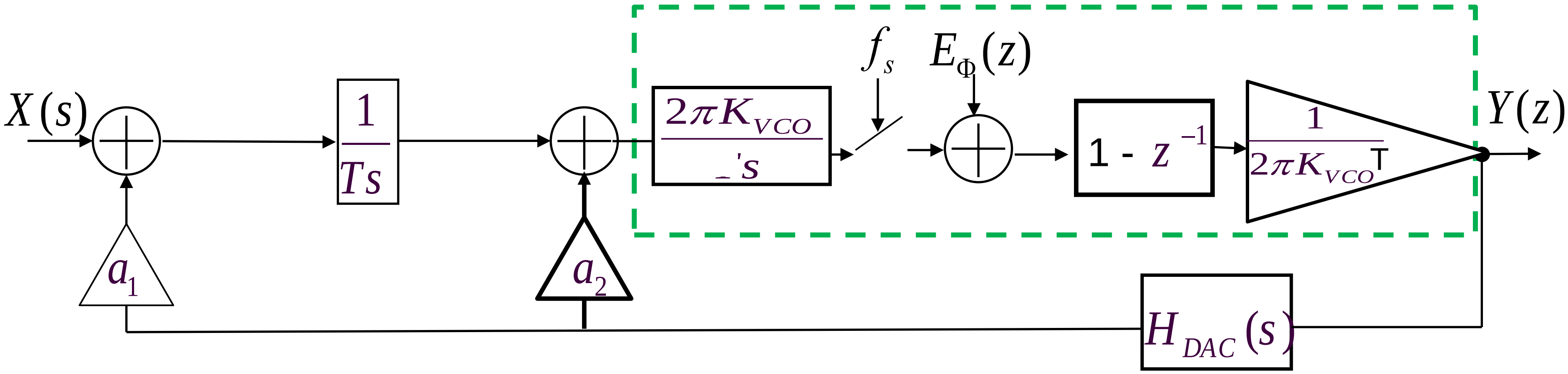
DWA algorithm



DWA: Data weighted averaging*

Second order SDM with VCO-based Quantizer

- Time Domain Quantization: Low Vdd (deep submicron) compatible
- No Comparators meta-stability, offsets and delay problems
- Inherent DWA without a dedicated circuit
- Saves an integrator (Mostly digitlal implementation)



SDM with VCO quantizer design(1)

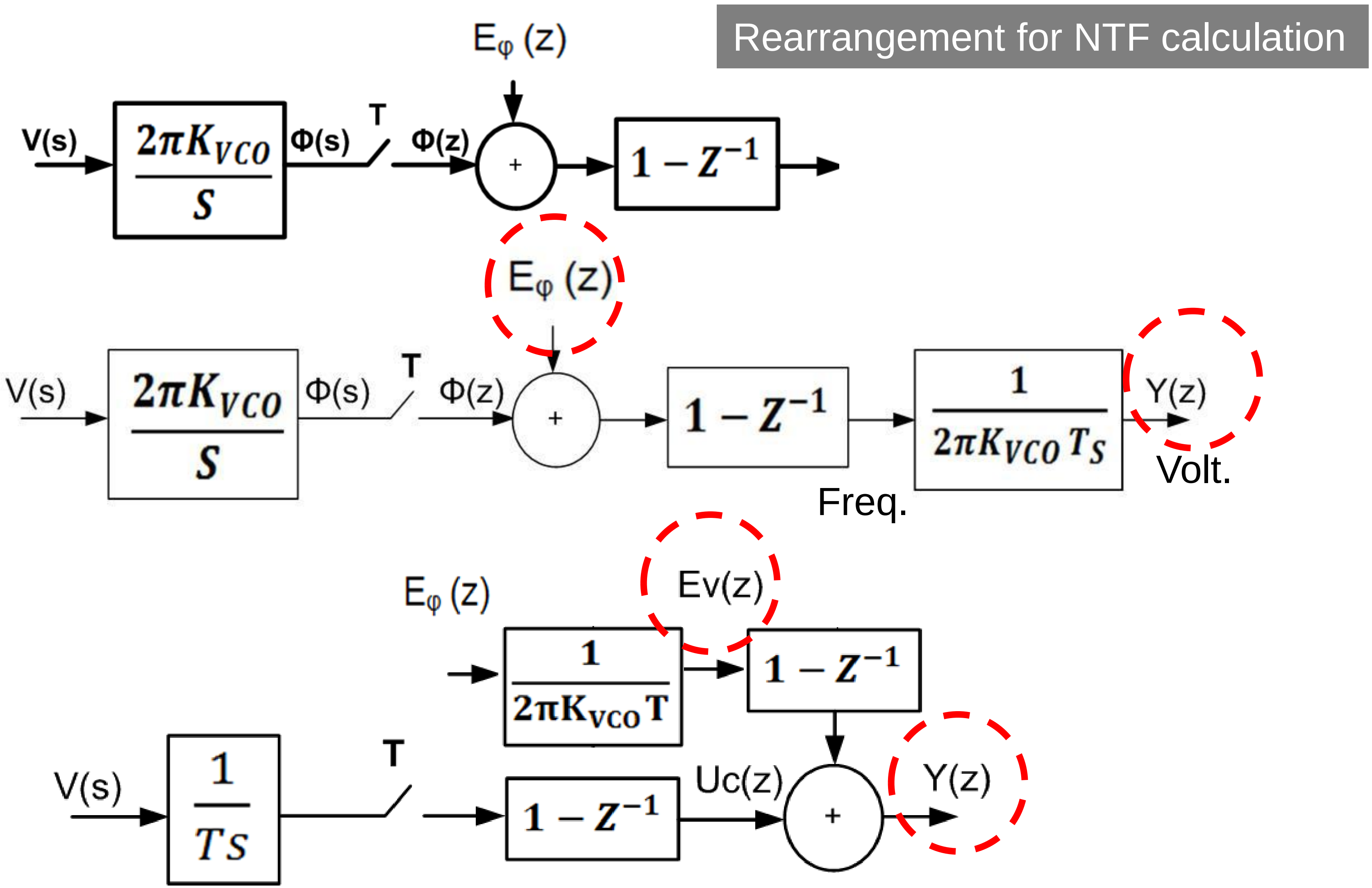
Exploit the 1st order noise shaping in the quantizer.

Transformation from Nth order DT to (N-1)th order CT with VCO quantizer

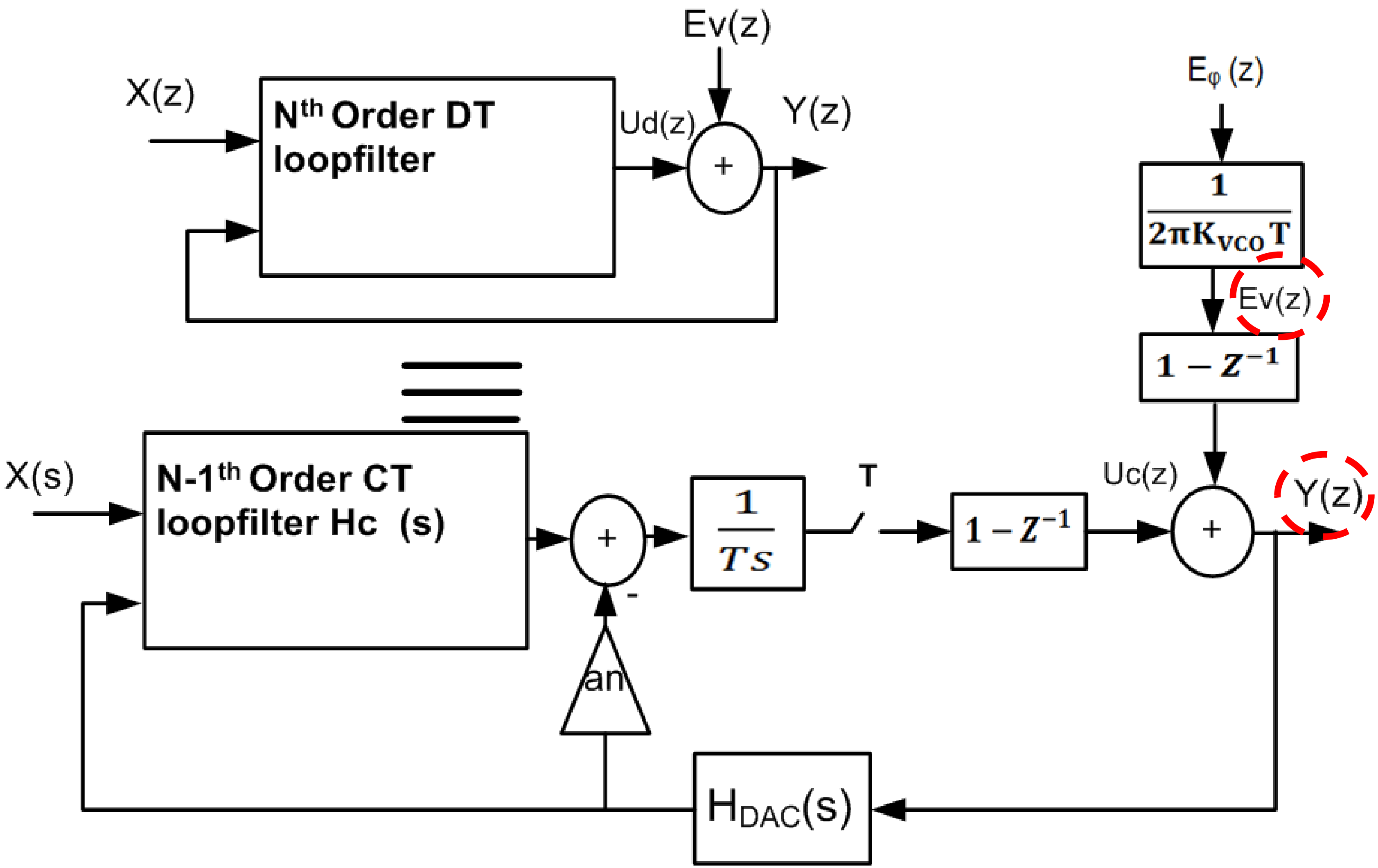
System Level Design

1) Get DT ΔΣ coefficients for Nth order Modulator (Schreier toolbox)
2) Get NTFd(z) and Gd(z) of the DT modulator
3) Get NTFc(z) and the corresponding loopgain Gc(z) of the CT modulator
4) Compare the two similar z orders in both NTF functions and to obtain the CT coefficients

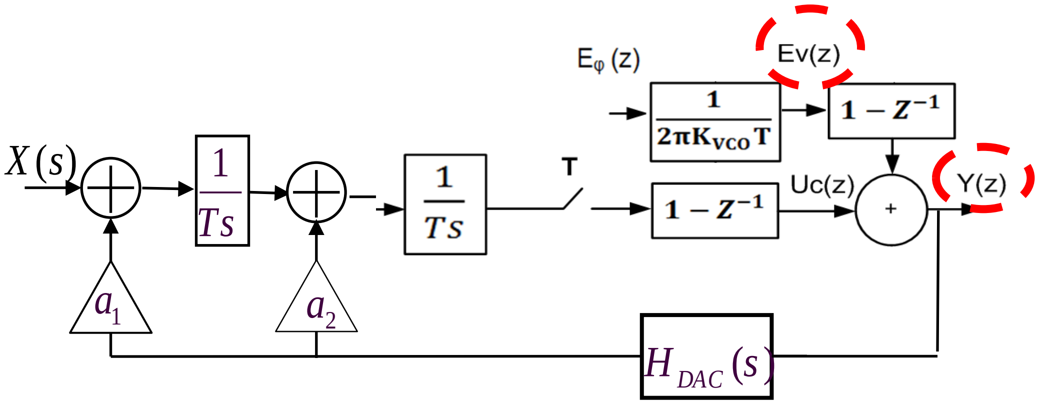
SDM with VCO quantizer design(2)

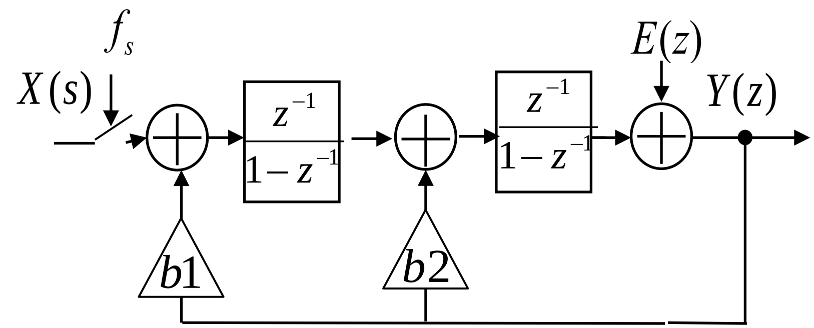


SDM with VCO quantizer design(3)



SDM with VCO quantizer design(4)



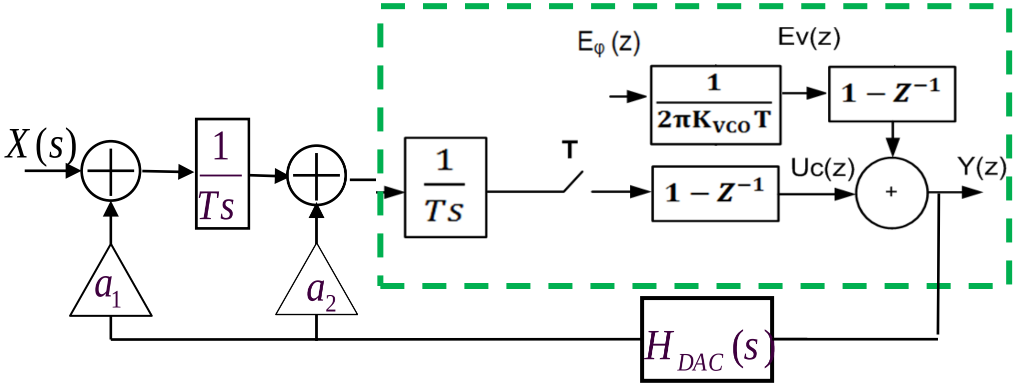


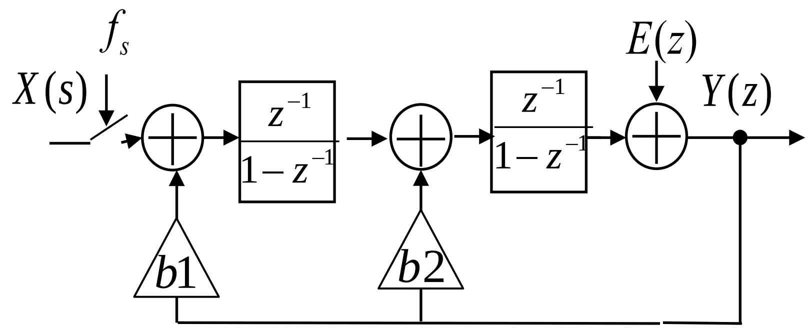
$$NTF_{VCO}(z)=\frac{Y(z)}{E_V(z)}=\frac{1-z^{-1}}{1-G_c(z)}=\frac{1}{1-G_c^{'}(z)}$$

$$G_c^{'}(z)=\frac{-z^{-1}}{1-z^{-1}}-Z\ \left\{H_{DAC}(s)H_C(s)\right\}$$

$$Z\ \left\{H_{DAC}(s)\left(\frac{a_2}{Ts}+\frac{a_1}{T^2s^2}\right)\right\}=Z\ \left\{\left(\frac{1-e^{-Ts}}{s}\right)\left(\frac{a_2}{Ts}+\frac{a_1}{T^2s^2}\right)\right\}$$

SDM with VCO quantizer design(4)





$$Z\left\{H_{DAC}(s)\left(\frac{a_2}{Ts}+\frac{a_1}{T^2s^2}\right)\right\}=Z\left\{\left(\frac{1-e^{-Ts}}{s}\right)\left(\frac{a_2}{Ts}+\frac{a_1}{T^2s^2}\right)\right\}$$

$$=(1-z^{-1})*Z\left\{\left(\frac{a_2}{Ts^2}+\frac{a_1}{T^2s^3}\right)\right\}$$

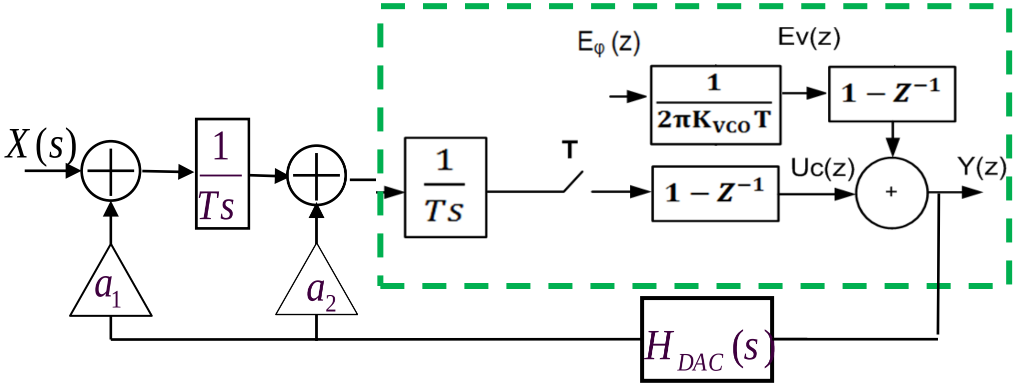
$$=(1-z^{-1})*\left(a_2\frac{-z}{(z-1)^2}-\frac{a_1}{2}\frac{z(z+1)}{(z-1)^3}\right)$$

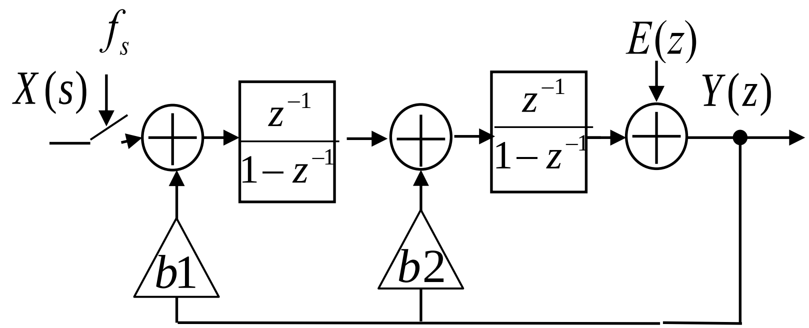
$$=(z-1)*\left(a_2\frac{-1}{(z-1)^2}-\frac{a_1}{2}\frac{(z+1)}{(z-1)^3}\right)$$

$$=\left(a_2\frac{-1}{(z-1)}-\frac{a_1}{2}\frac{(z+1)}{(z-1)^2}\right)$$

$$=\frac{(-a_2-a_1/2-1)z+(a_2-a_1/2+1)}{(z-1)^2}$$

SDM with VCO quantizer design(4)





$$NTF_{VCO}(z)=\frac{Y(z)}{E_V(z)}=\frac{1-z^{-1}}{1-G_c(z)}=\frac{1}{1-G_c^{'}(z)}$$

$$NTF_D(z)=\frac{Y(z)}{E(z)}=\frac{1}{1-G_d(z)}$$

$$G_c^{'}(z)=\frac{(-a_2-a_1/2-1)z+(a_2-a_1/2+1)}{(z-1)^2}$$

$$G_d(z)=\frac{-(b_2)z\ +b_2-b_1}{(z-1)^2}$$

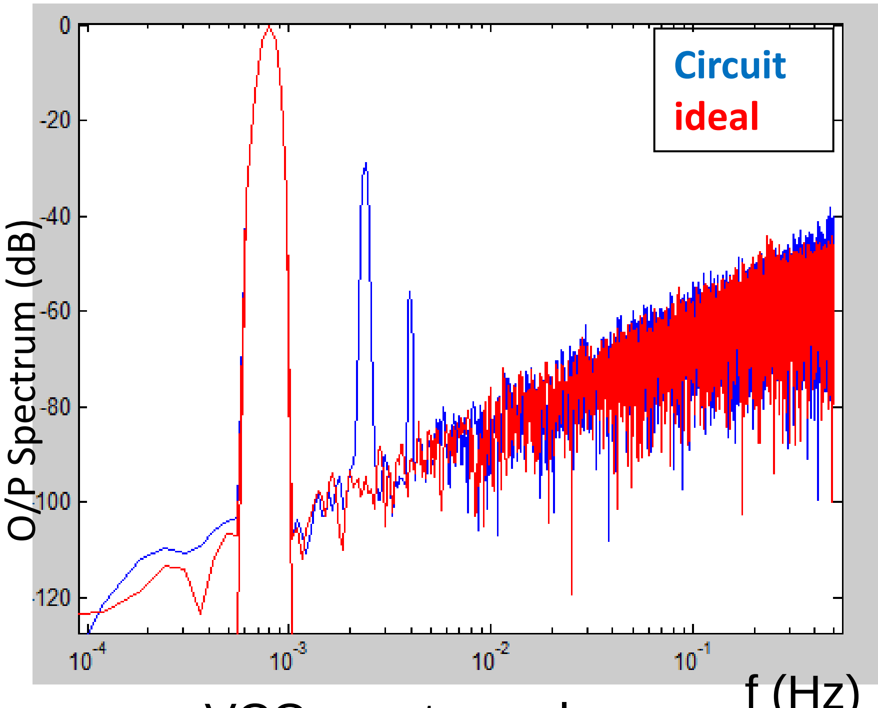
$$-b_2=-a_0-\frac{a_1}{2}-1$$

$$b_2-b_1=\quad a_2-\frac{a_1}{2}+1$$

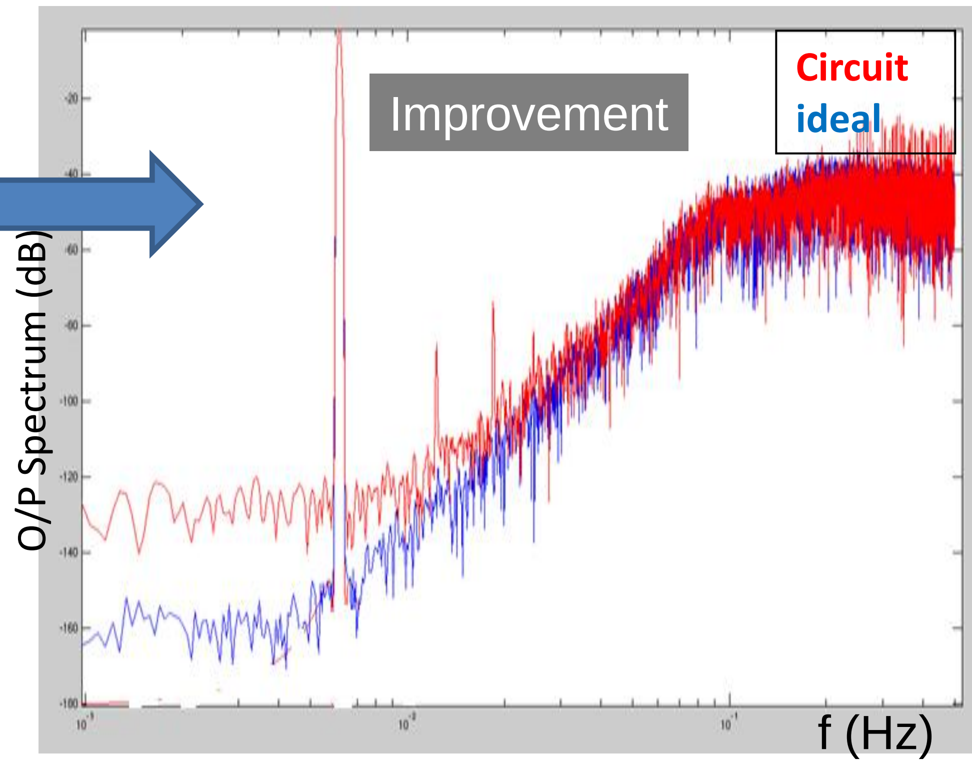
$$b_1=a_1$$

$$b_2-\frac{b_1}{2}-1=a_2$$

Non ideal VCO-based quantizer in SD

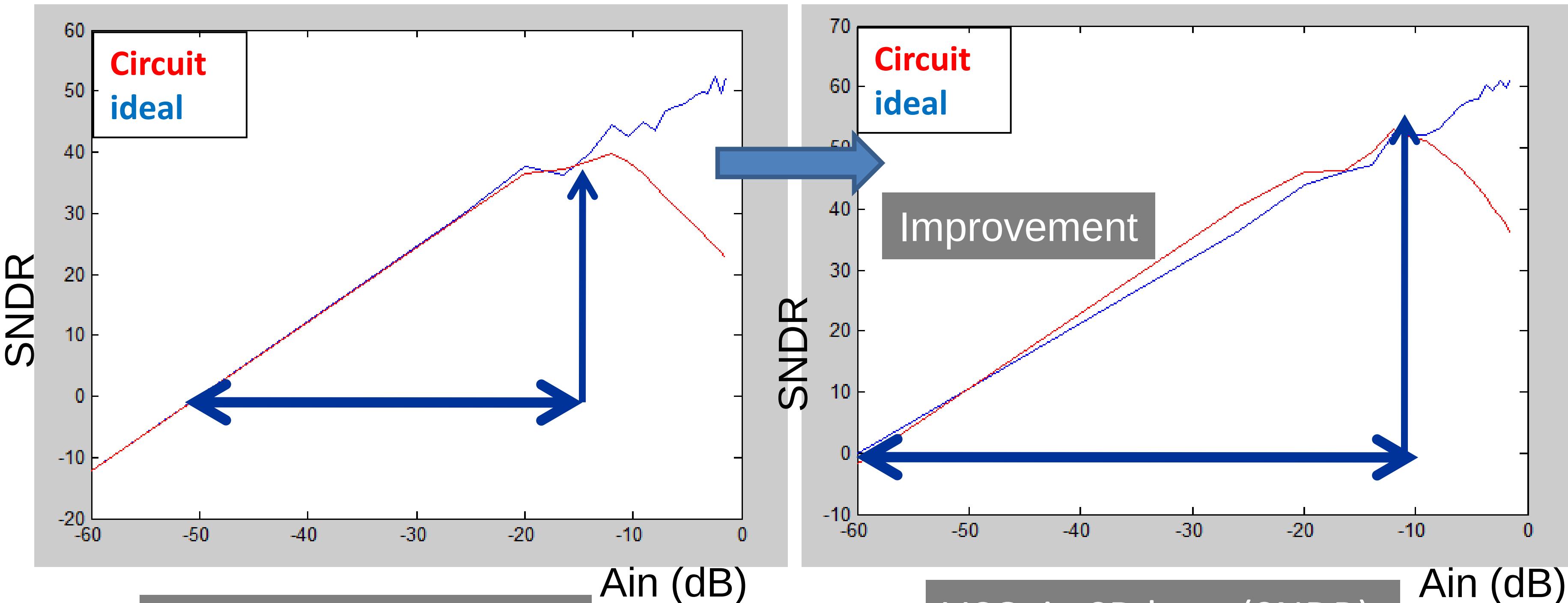


VCO spectrum alone



VCO spectrum in SD loop

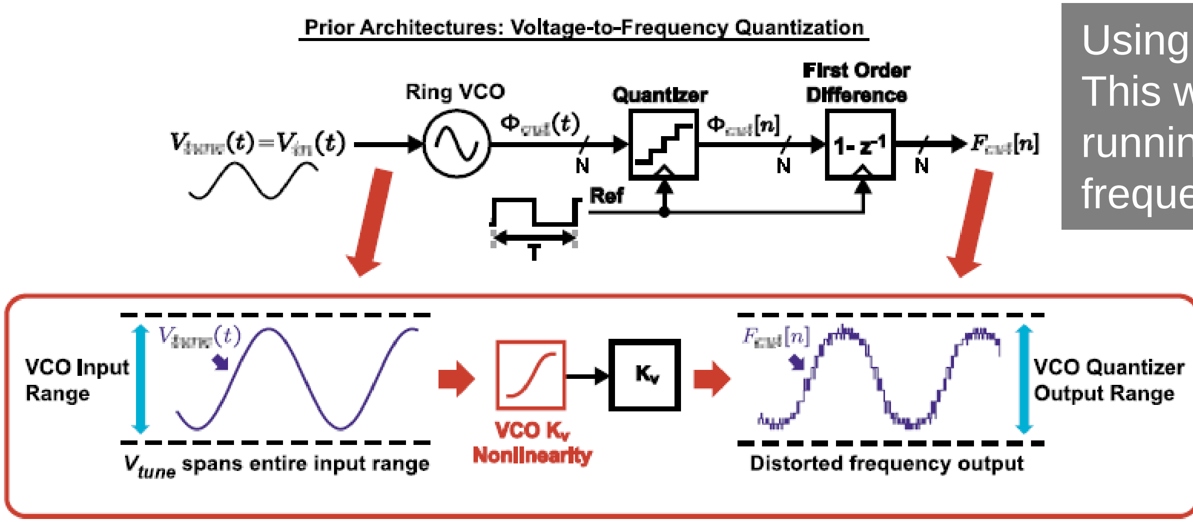
Non ideal VCO-based quantizer in SD



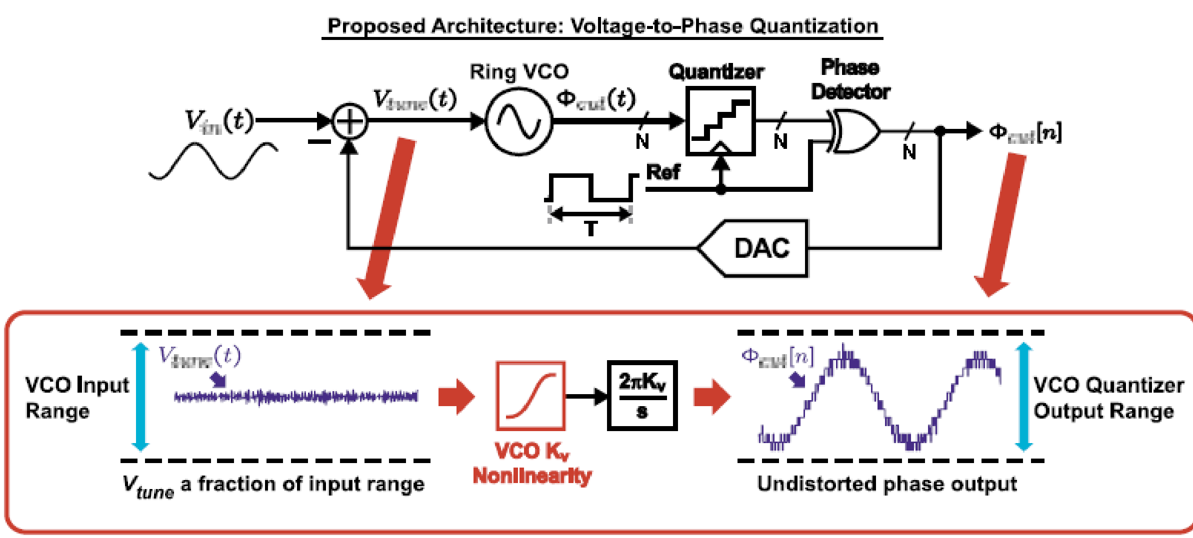
VCO quantizer(SNDR)

VCO in SD loop (SNDR)

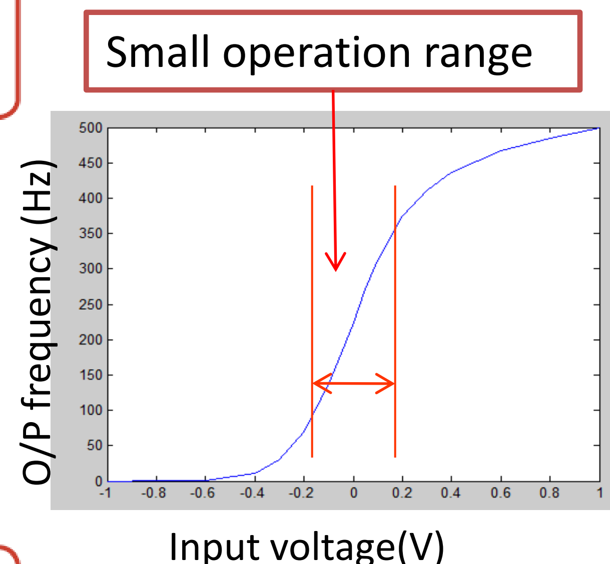
Linearization through feedback



(a)



Using Negative feedback
This will make the VCO always running very close to its free running frequency



Summary & Conclusion

- TDC are potential candidates for modern wide band ADC
- They achieve good resolution and BW efficiently (low power)
- They are compatible with technology scaling thus allowing further efficency in terms of power and area

- Using TDC techniques in ADC need analog to time conversion which is usually non-linear.
- VCO-based quantizer has an important noise shaping property
- The use of VCO-based quantizer as a multi-bit quantizer in SDM decreases the non-linearity due to the SDM loop filter gain.

- Further suppression of non-linearities is possible using Negative Feedback

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