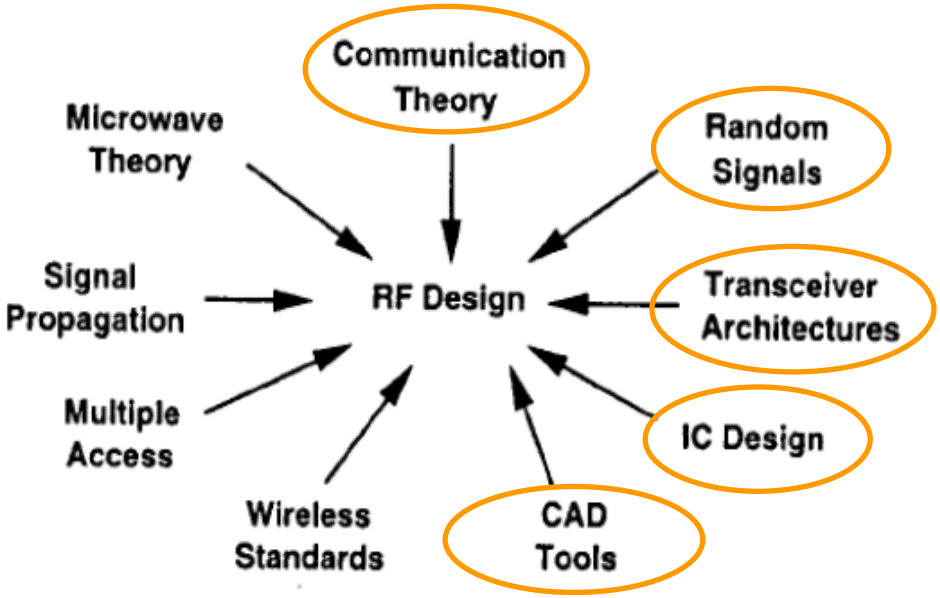
CIRF
Circuit Intégré Radio Fréquence

Low Noise Amplifier

Hassan Aboushady
Université Paris VI

Multidisciplinarity of radio design



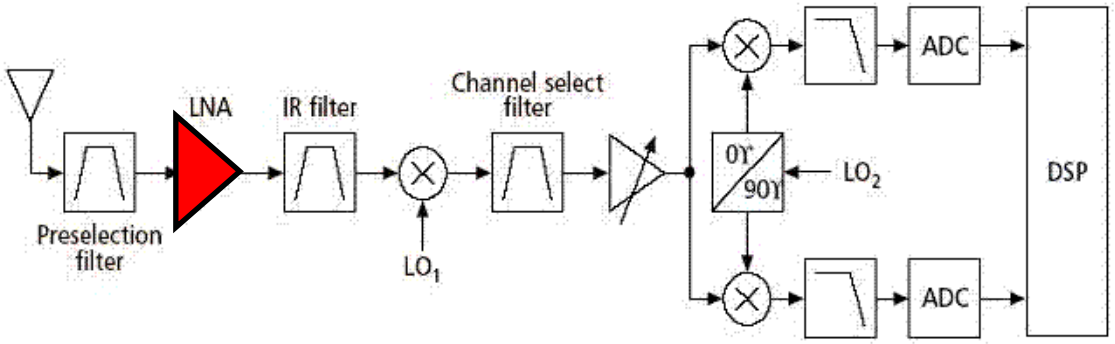
B. Razavi,
RF Microelectronics, Prentice Hall, 1998

References

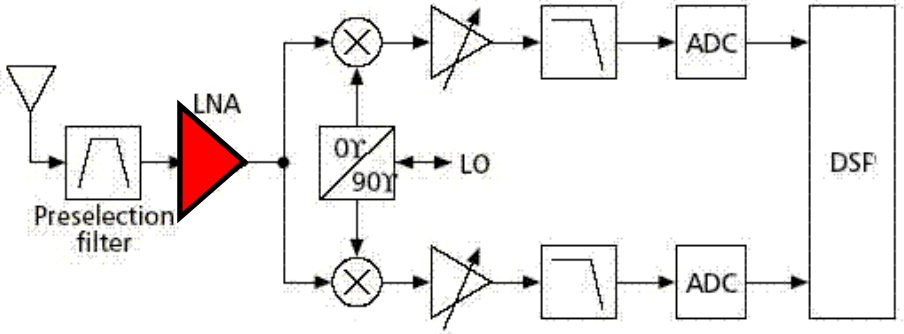
- M. Perrott, "High Speed Communication Circuits and Systems", M.I.T.OpenCourseWare, http://ocw.mit.edu/, Massachusetts Institute of Technology, 2005.
- D. Leenaerts, J. van der Tang, and C. Vaucher, "Circuit design for RF transceivers", Kluwer academic publishers, 2001.

LNA : 1st block of an RF Receiver

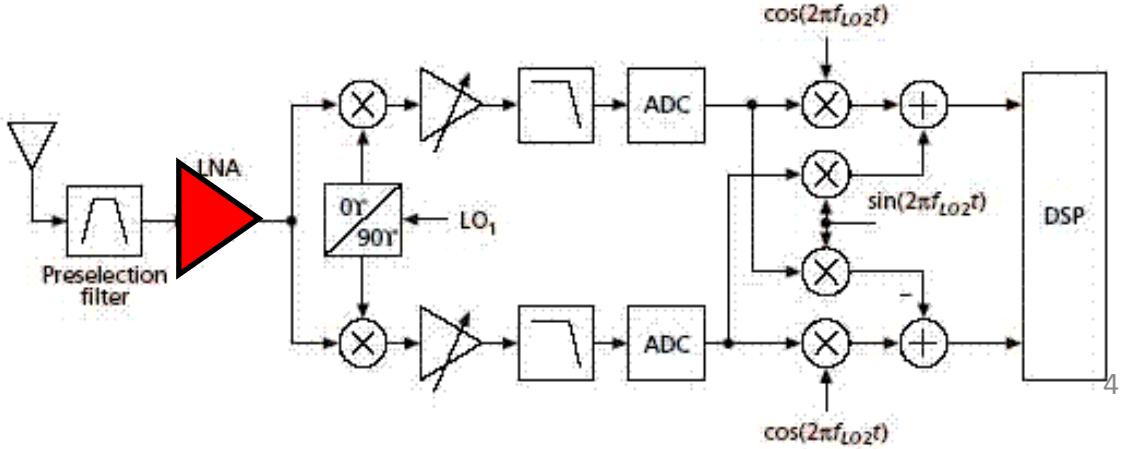
- **Heterodyne**



- **Homodyne (Direct conversion)**



- **Low-IF**



LNA Requirements: Noise

Noise Factor : $F = \frac{SNR_{in}}{SNR_{out}}$

Noise Figure : $NF = 10 \log_{10}(F)$

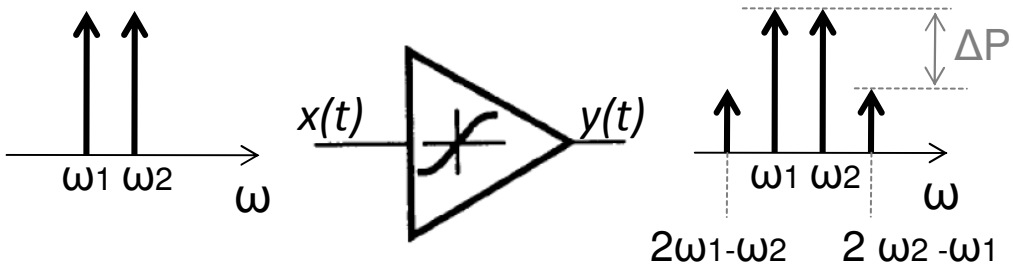
Friis Equation :

$$F = 1 + (F_1 - 1) + \frac{(F_2 - 1)}{G_1} + \frac{(F_3 - 1)}{G_1 G_2} + \ldots + \frac{(F_n - 1)}{G_1 G_2 \ldots G_{n-1}}$$

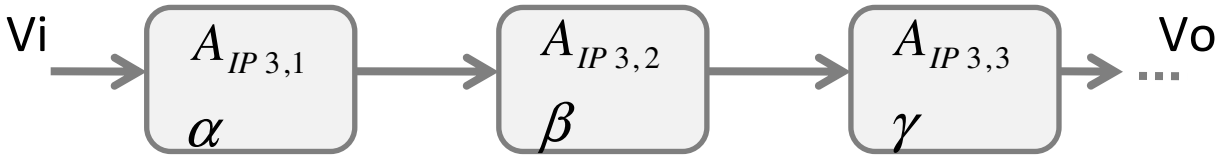
LNA Requirements to reduce the RF receiver overall Noise Factor:

- **Low Noise Factor, F_1**
- **High Gain, G_1**

LNA Requirements: Linearity



$$IIP3\big|_{dBm} = \frac{\Delta P\big|_{dB}}{2} + P_{in}\big|_{dBm}$$



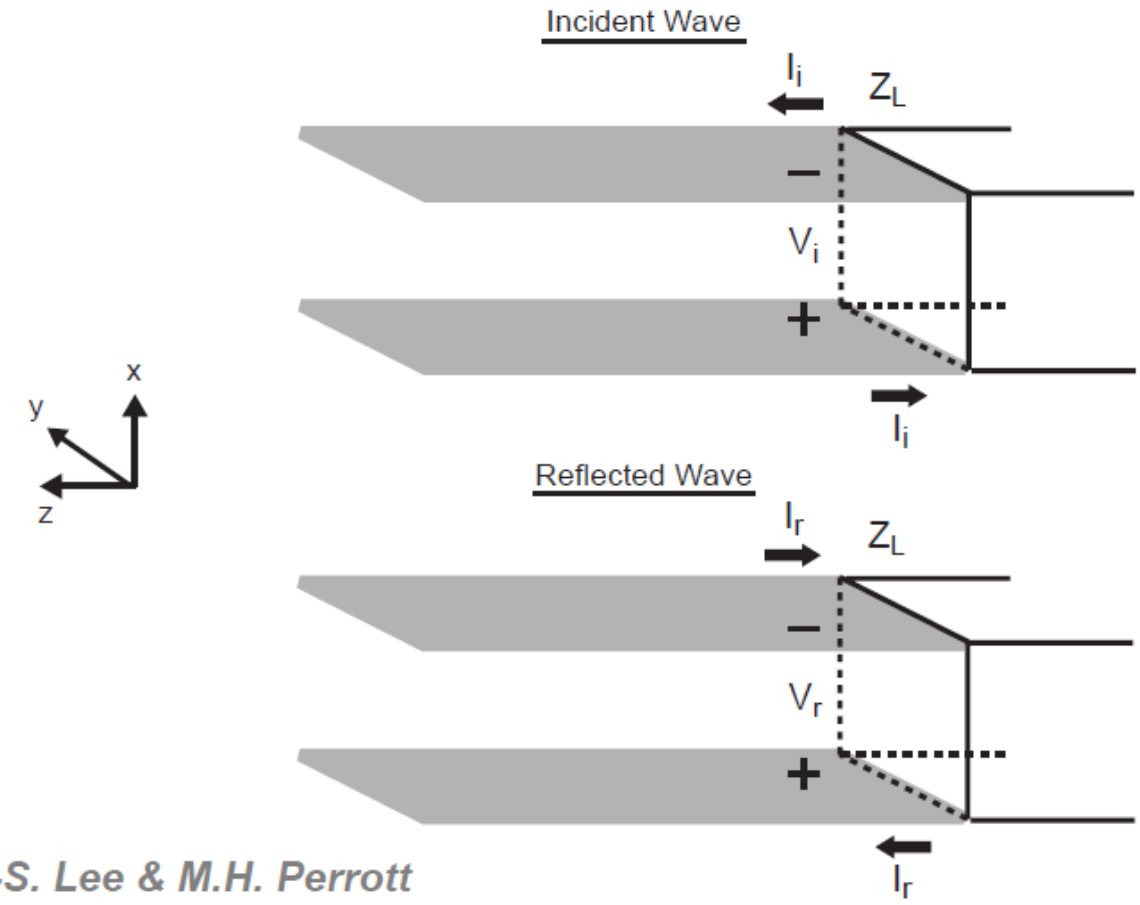
$$\frac{1}{A_{IP3}^2} \approx \frac{1}{A_{IP3,1}^2} + \frac{\alpha_1^2}{A_{IP3,2}^2} + \frac{\alpha_1^2 \beta_1^2}{A_{IP3,3}^2} + \ldots$$

LNA Requirements to improve the RF receiver overall linearity:

- **High $A_{IP3,1}$**
- **Low α_1**

What Happens At The Load Location?

- Voltage and currents at load are ratioed according to the load impedance



Voltage at Load

$$V_i + V_r$$

Current at Load

$$I_i - I_r$$

Ratio at Load

$$\frac{V_i + V_r}{I_i - I_r} = Z_L$$

Relate to Characteristic Impedance

- From previous slide

$$\frac{V_i + V_r}{I_i - I_r} = \frac{V_i}{I_i}\left(\frac{1 + V_r/V_i}{1 - I_r/I_i}\right) = Z_L$$

- Voltage and current ratio in transmission line set by it characteristic impedance

$$\frac{V_i}{I_i} = \frac{V_r}{I_r} = Z_o \quad \Rightarrow \quad \frac{I_r}{I_i} = \frac{V_r}{V_i}$$

- Substituting:

$$Z_o\left(\frac{1 + V_r/V_i}{1 - V_r/V_i}\right) = Z_L$$

Define Reflection Coefficient

- **Definition:** $\Gamma_L = \dfrac{V_r}{V_i}$
  - No reflection if $\Gamma_L = 0$
- **Relation to load and characteristic impedances**

$$Z_o\left(\frac{1+\Gamma_L}{1-\Gamma_L}\right) = Z_L$$

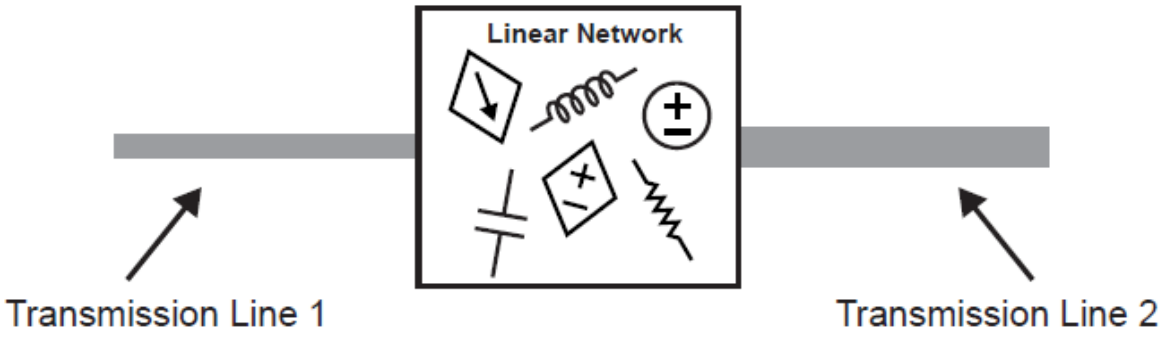
- **Alternate expression**

$$\Gamma_L = \frac{Z_L - Z_o}{Z_L + Z_o}$$

  - No reflection if $Z_L = Z_o$

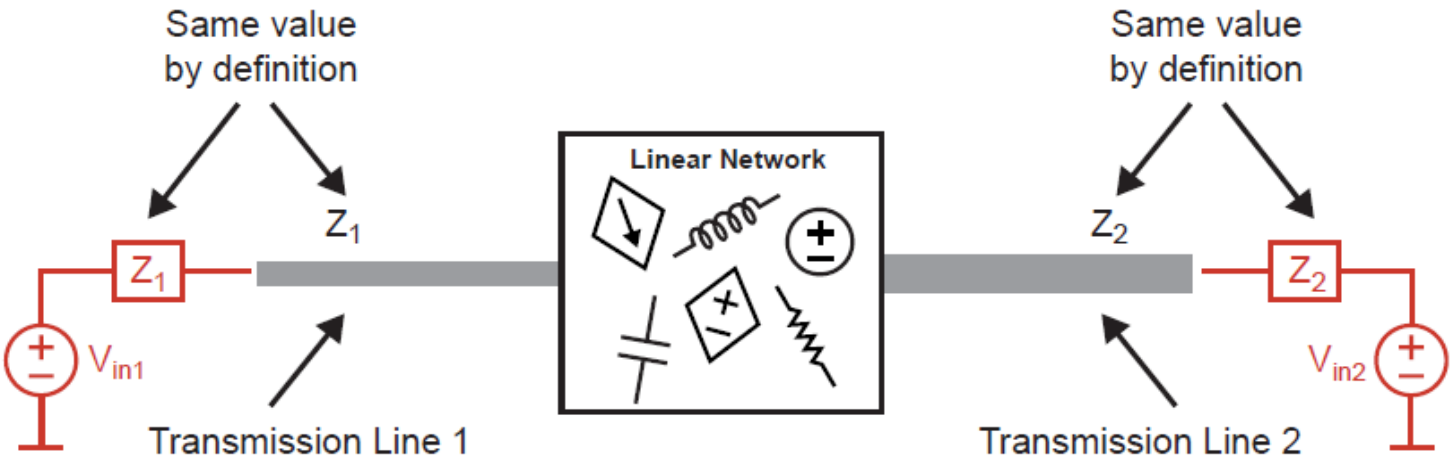
Parameterization of High Speed Circuits/Passives

- **Circuits or passive structures are often connected to transmission lines at high frequencies**
  - **How do you describe their behavior?**



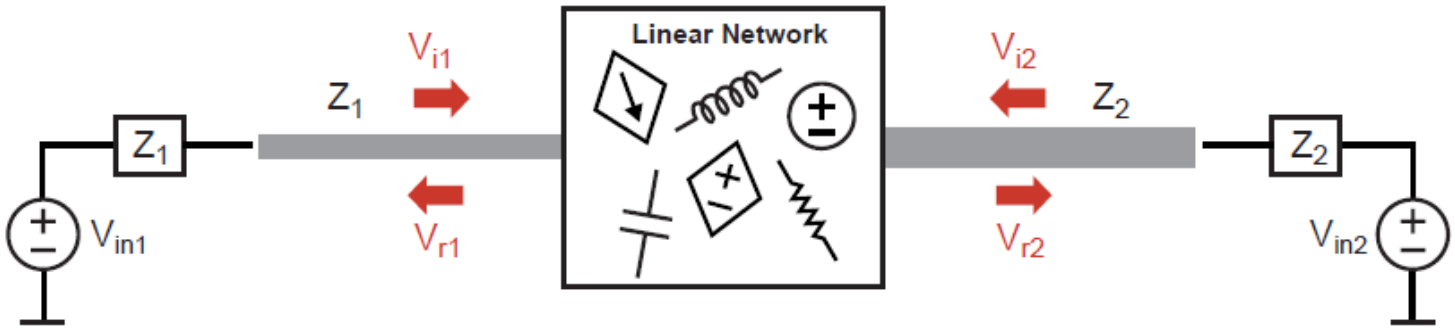
Calculate Response to Input Voltage Sources

- Assume source impedances match their respective transmission lines



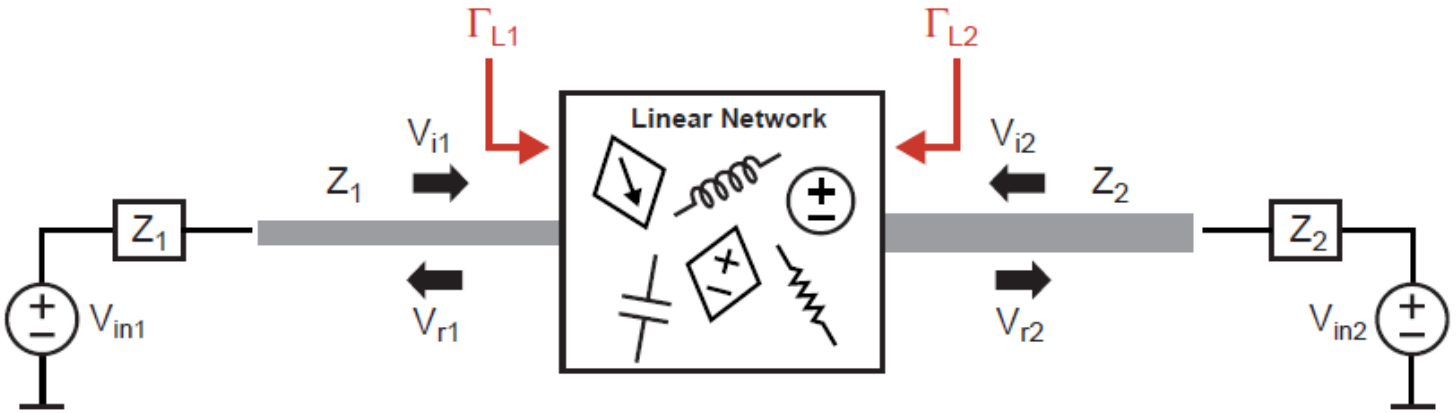
Calculate Response to Input Voltage Sources

- Sources create incident waves on their respective transmission line
- Circuit/passive network causes
  - Reflections on same transmission line
  - Feedthrough to other transmission line



Calculate Response to Input Voltage Sources

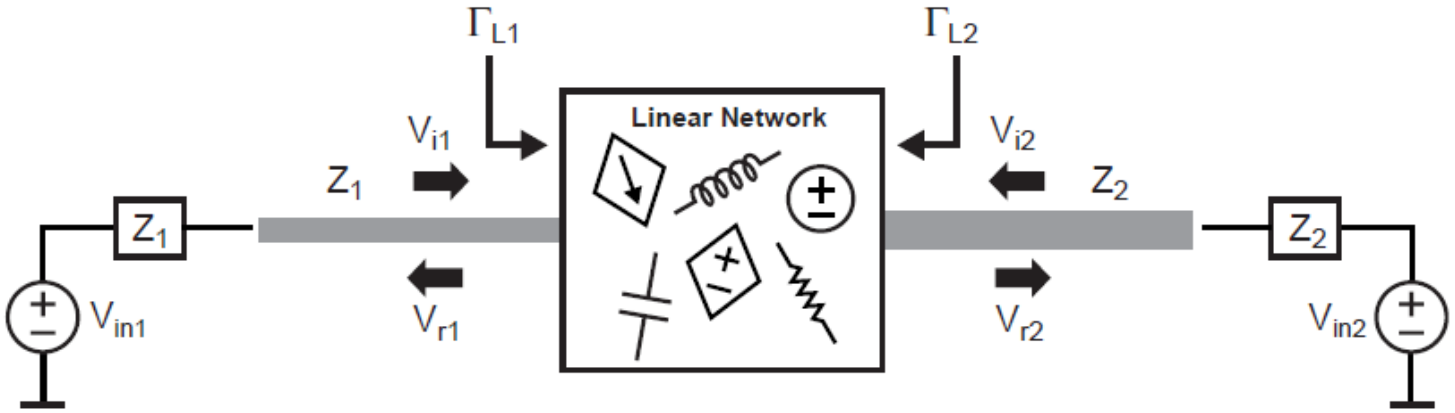
- Reflections on same transmission line are parameterized by Γ_L
  - Note that Γ_L is generally different on each side of the circuit/passive network



How do we parameterize feedthrough to the other transmission line?

S-Parameters – Definition

- Model circuit/passive network using 2-port techniques
  - Similar idea to Thevenin/Norton modeling

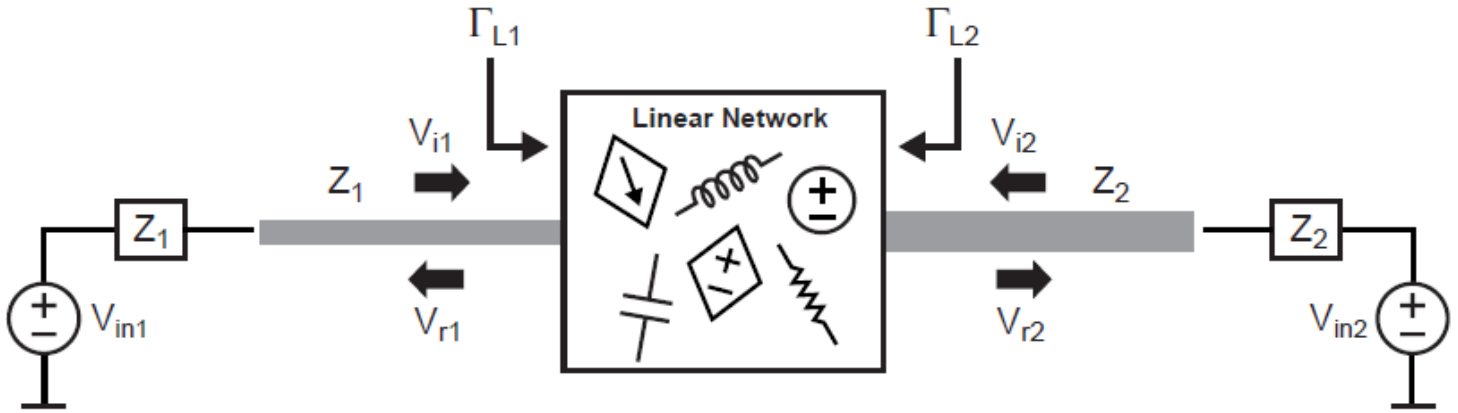


- Defining equations:

$$\frac{V_{r1}}{\sqrt{Z_1}} = S_{11}\frac{V_{i1}}{\sqrt{Z_1}} + S_{12}\frac{V_{i2}}{\sqrt{Z_2}}$$

$$\frac{V_{r2}}{\sqrt{Z_2}} = S_{21}\frac{V_{i1}}{\sqrt{Z_1}} + S_{22}\frac{V_{i2}}{\sqrt{Z_2}}$$

S-Parameters – Calculation/Measurement



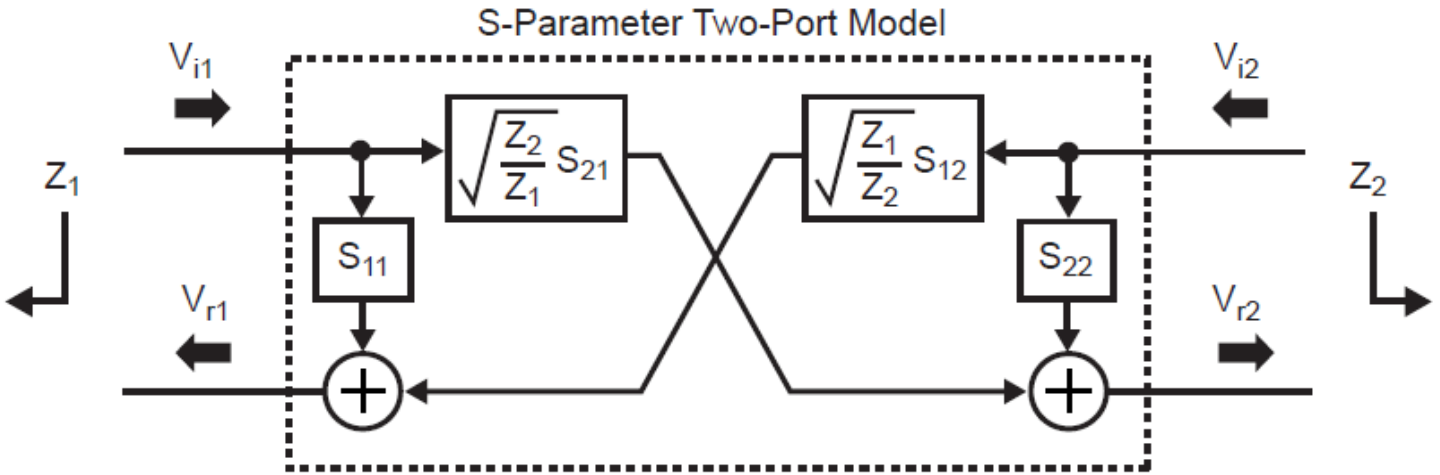
$$\frac{V_{r1}}{\sqrt{Z_1}} = S_{11}\frac{V_{i1}}{\sqrt{Z_1}} + S_{12}\frac{V_{i2}}{\sqrt{Z_2}} \qquad \frac{V_{r2}}{\sqrt{Z_2}} = S_{21}\frac{V_{i1}}{\sqrt{Z_1}} + S_{22}\frac{V_{i2}}{\sqrt{Z_2}}$$

set $V_{in2} = 0$ | set $V_{in1} = 0$

$$\Rightarrow S_{11} = \frac{V_{r1}}{V_{i1}} = \Gamma_{L1} \qquad \Rightarrow S_{22} = \frac{V_{r2}}{V_{i2}} = \Gamma_{L2}$$

$$\Rightarrow S_{21} = \sqrt{\frac{Z_1}{Z_2}}\left(\frac{V_{r2}}{V_{i1}}\right) \qquad \Rightarrow S_{12} = \sqrt{\frac{Z_2}{Z_1}}\left(\frac{V_{r1}}{V_{i2}}\right)$$

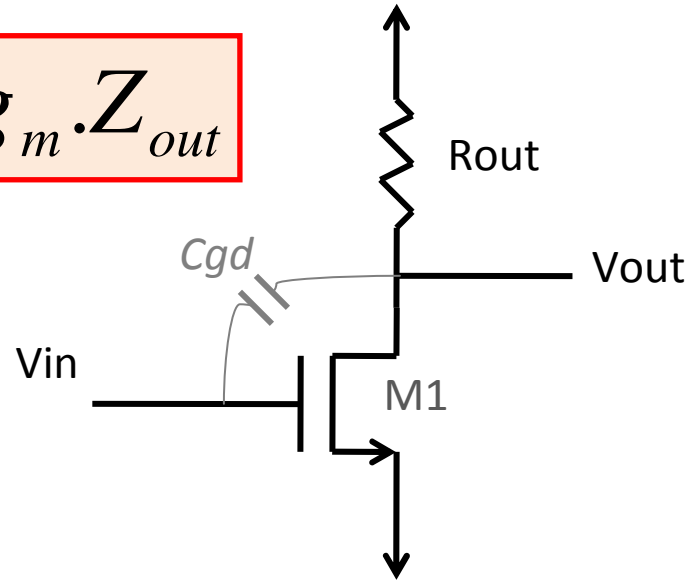
Block Diagram of S-Parameter 2-Port Model



- Key issue – two-port is parameterized with respect to the left and right side load impedances (Z_1 and Z_2)
  - Need to recalculate S_{11}, S_{21}, etc. if Z_1 or Z_2 changes
  - Typical assumption is that $Z_1 = Z_2 = 50$ Ohms

Common Source Amplifier

$$A_v = g_m . Z_{out}$$



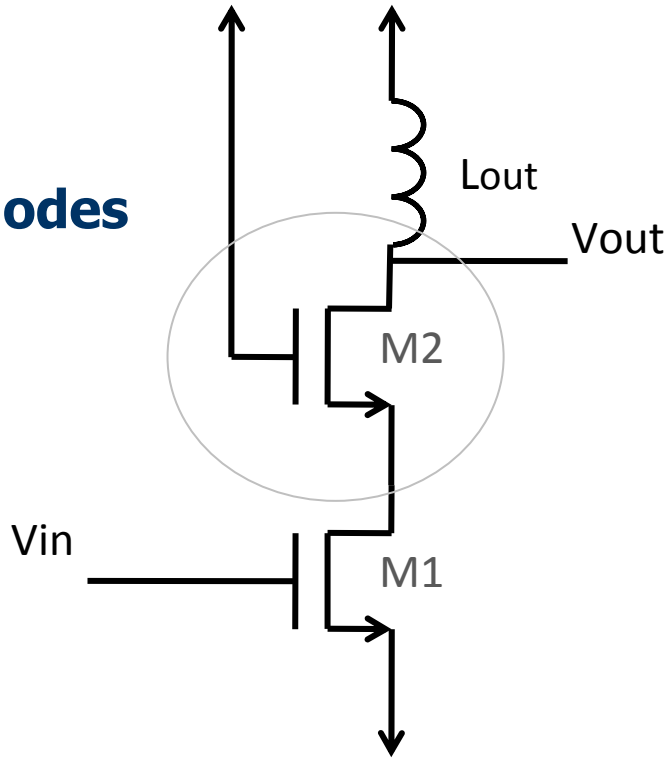
- **Parasitic capacitance *Cgd* between input and output nodes.**
- **Low Gain**
- **Complex Load Impedance**

$$(Z_{out} = R_{out} \| \; r_0 \| \; \frac{1}{j\omega C_{par}})$$

Common Source Cascode with Inductive Load

Benefits of Cascode

- Isolation between input and output nodes
- Higher Gain

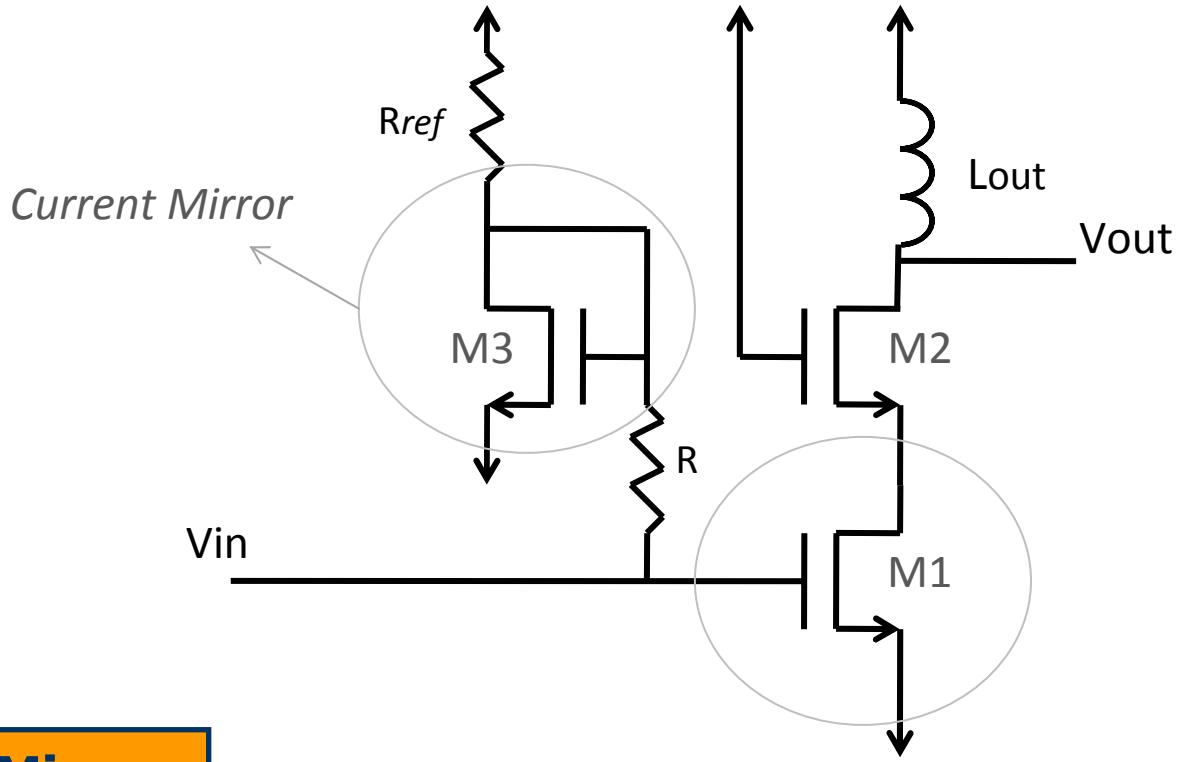


Purpose of Inductive Load

- Real Load Impedance can be obtained

$$(Z_{out} = r_{0cascode} \| \frac{1}{j\omega_0 C_{par}} \| j\omega_0 L_{out})$$

Biasing

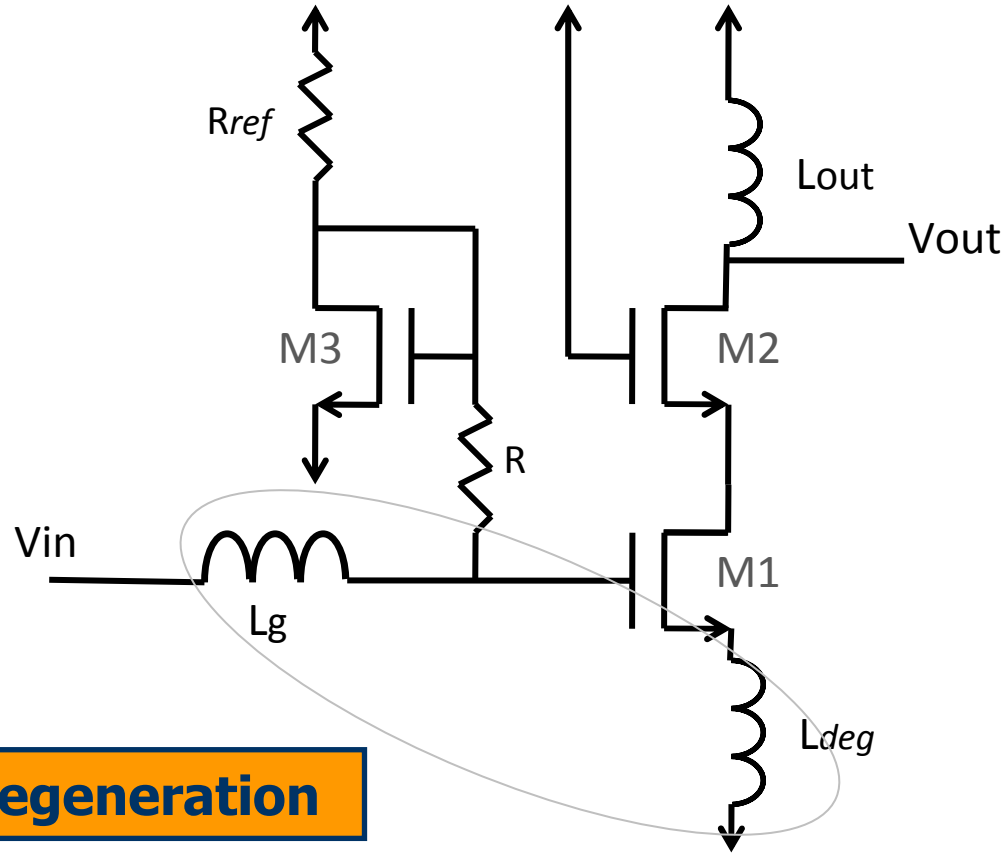


Current Mirror

- **The current in M1 is fixed by Rref and the ratio (W1/L1)/(W3/L3).**

- **R is to increase the impedance seen by the input signal.**

Matching Input Impedance

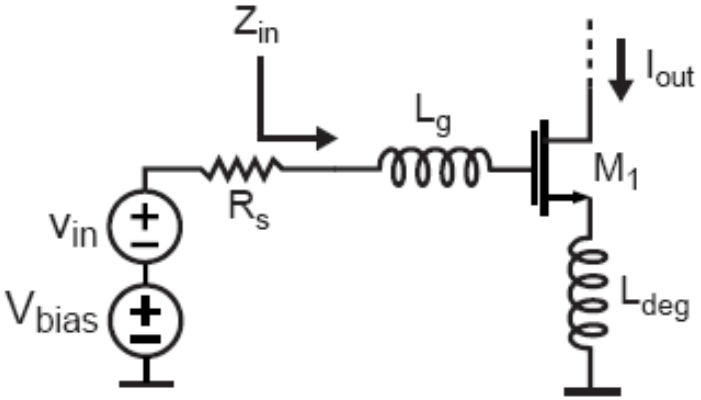


Inductive Degeneration

- **Lg compensates the complex impedance due to *Cgs1* .**

- **L*deg* adjusts the real part of the input impedance to 50 Ω .**

Ldeg and Lg (1)



- **Input Impedance**

$$Z_{in}(s) = \frac{1}{sC_{gs}} + s(L_{\deg} + L_g) + \frac{g_m}{C_{gs}} L_{\deg}$$

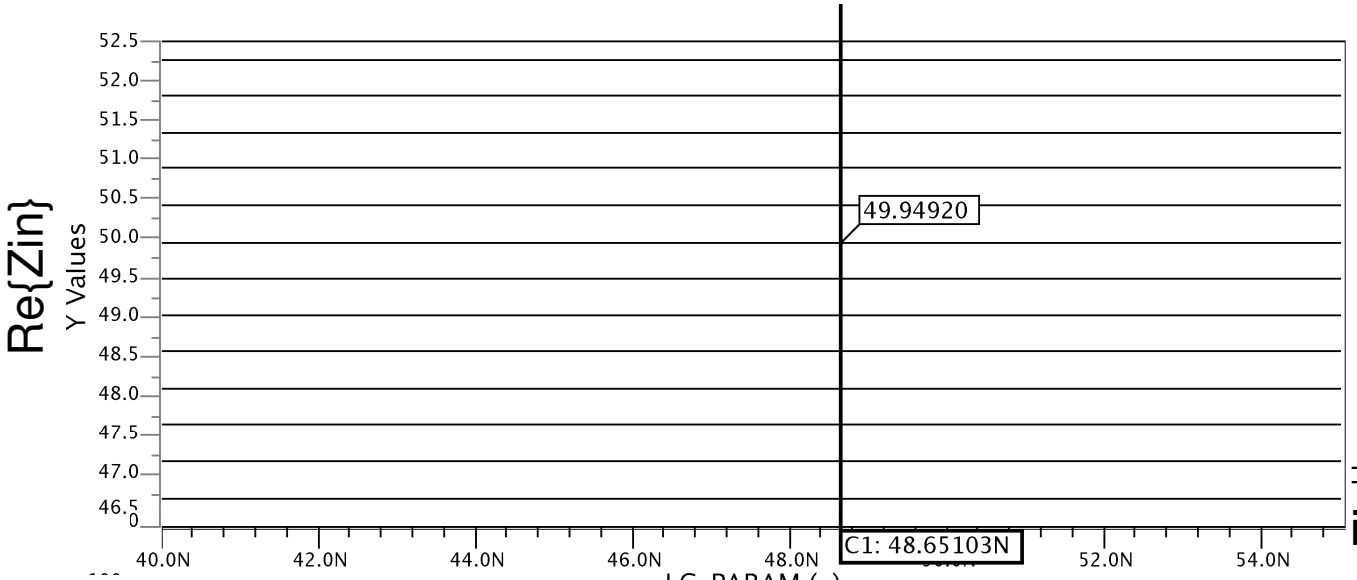
- **Matching Z_{in} to 50Ω**

$$R_s = \frac{g_m}{C_{gs}} L_{\deg}$$

- **For a Real Impedance @ ω_0**

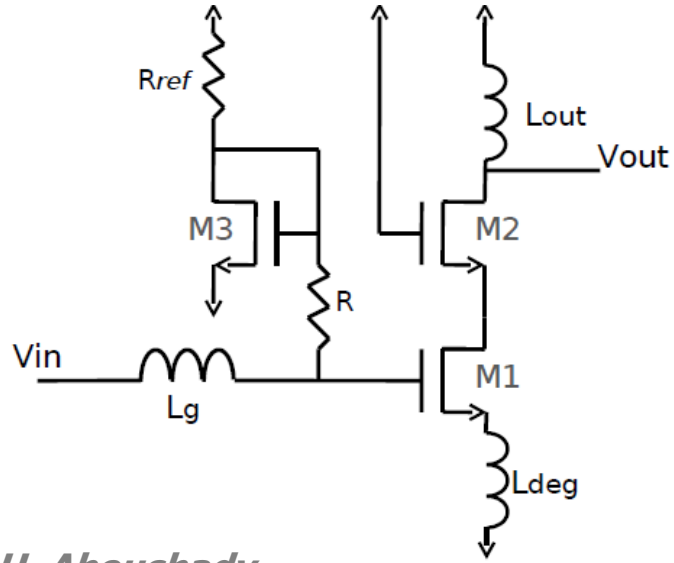
$$\omega_0 = \frac{1}{\sqrt{(L_g + L_{\deg})C_{gs}}}$$

Ldeg and Lg (2)

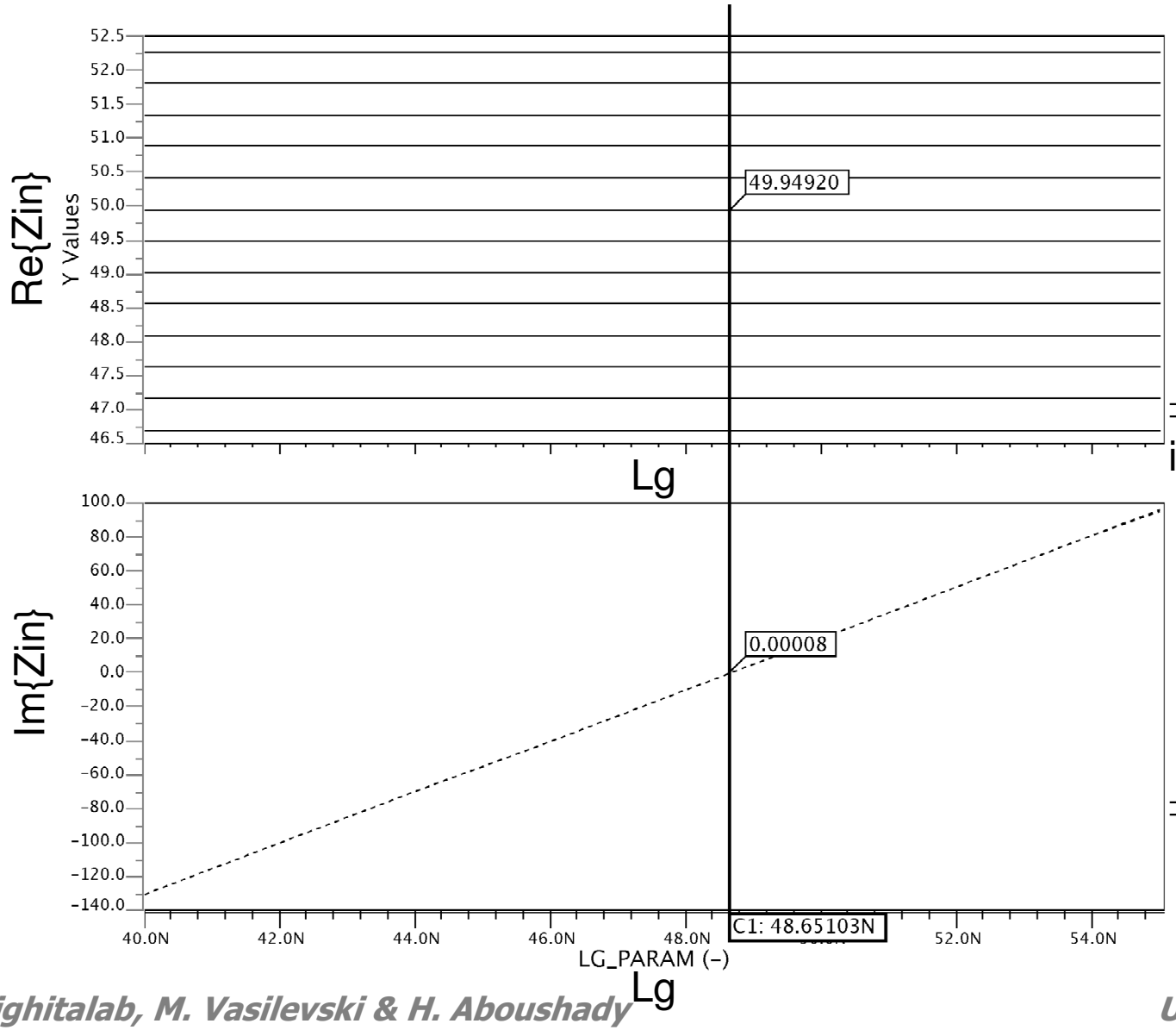


For different Ldeg values

⇒Re{Zin} independent of Lg



Ldeg and Lg (2)

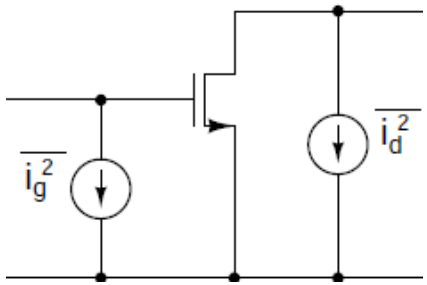


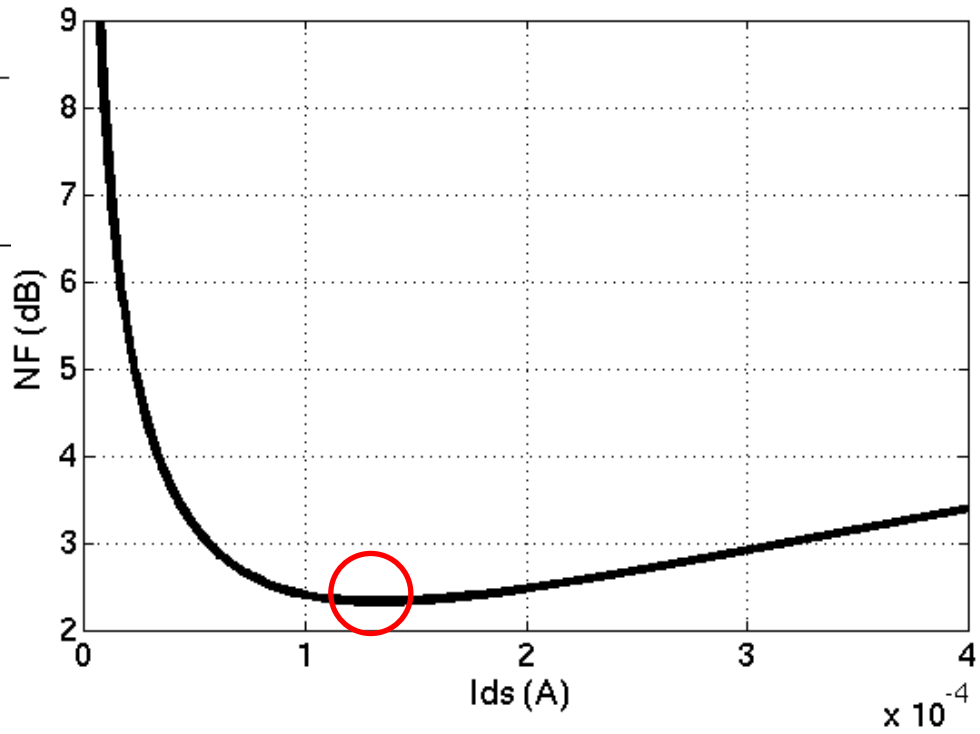
For different Ldeg values

⇒Re{Zin} independent of Lg

⇒Ldeg for:
Re{Zin}=50
Lg for:
Im{Zin}=0

NF of a MOS Transistor





Techno. 0.35µm
c= -0.4j
γ = 2/3

$$\text{Noise Factor} = 1+\left(\frac{w_o}{w_t}\right)\gamma\left(\frac{g_{do}}{g_m}\right)\frac{1}{2Q}\left(1-2|c|\chi_d+(4Q^2+1)\chi_d^2\right)$$

$$\chi_d = \frac{g_m}{g_{do}}\sqrt{\frac{\delta}{5\gamma}} \qquad g_{do} = \left.\frac{dI_d}{dV_{ds}}\right|_{V_{ds}=0} \qquad c = \frac{\overline{i_{nd}^* i_{ng}}}{\sqrt{\overline{i_{nd}^2}\,\overline{i_{ng}^2}}} \qquad Q = \frac{1}{w_o C_{gs} 2R_s} \qquad w_t \approx \frac{g_m}{C_{gs}}$$

NF Characterization

$$F = \frac{SNR_i}{SNR_o} = \frac{S_i / N_{i(source)}}{S_o / N_{o(total)}} = \frac{S_i / N_{i(source)}}{(S_i.G) / N_{o(total)}} = \frac{N_{o(total)}}{G.N_{i(source)}}$$

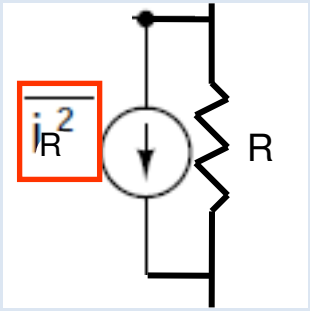
$$N_{o(total)} = N_{o(source)} + N_{o(added)}$$

$$\Rightarrow F = \frac{N_{o(total)}}{N_{o(source)}} = \frac{N_{o(source)} + N_{o(added)}}{N_{o(source)}} = 1 + \frac{N_{o(added)}}{N_{o(source)}}$$

1) **No(added) : Output Reffered Noise due to the LNA.**
2) **No(source): Output Reffered Noise due to the source.**

Noise Sources

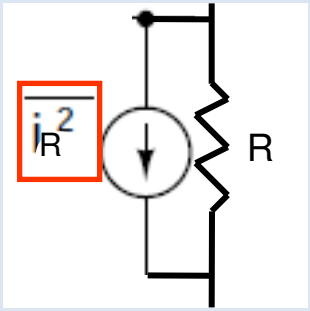
Résistance



$$\overline{i_R^2} = 4kT / R$$

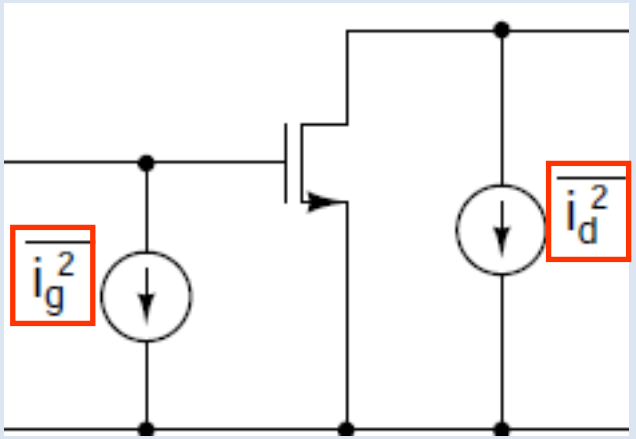
Noise Sources

Résistance



$$\overline{i_R^2} = 4kT/R$$

Transistor

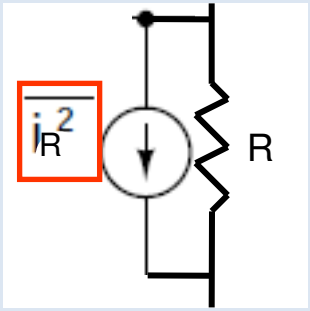


$$\overline{i_d^2} = 4kT\,\gamma g_{d0}\Delta f$$

$$\overline{i_g^2} = 4kT\,\delta g_{gs}\Delta f$$

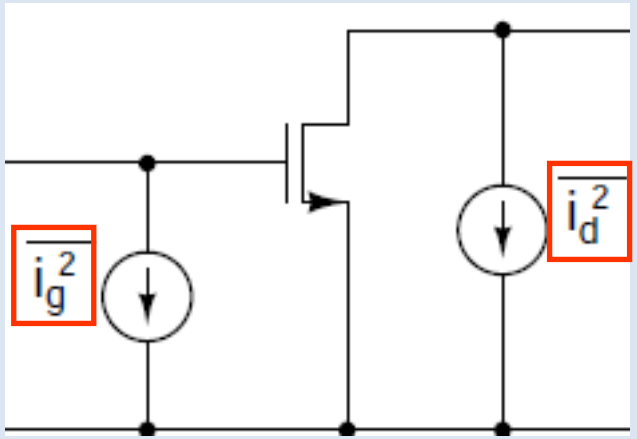
Noise Sources

Résistance



$$\overline{i_R^2} = 4kT/R$$

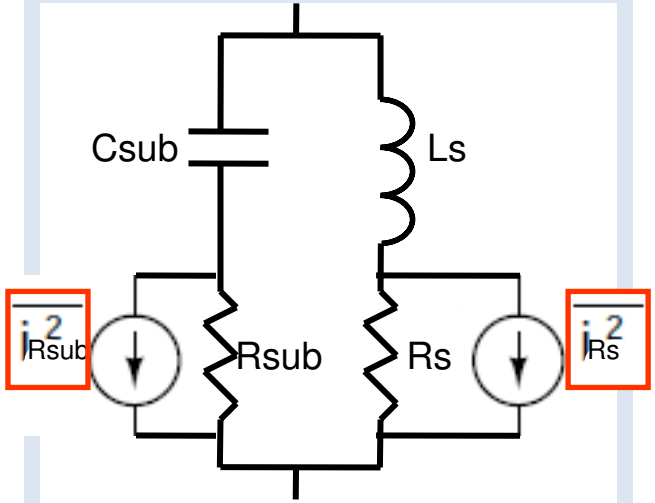
Transistor



$$\overline{i_d^2} = 4kT\,\gamma g_{d0}\Delta f$$

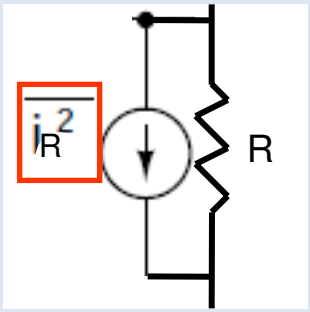
$$\overline{i_g^2} = 4kT\,\delta g_{gs}\Delta f$$

Inductance



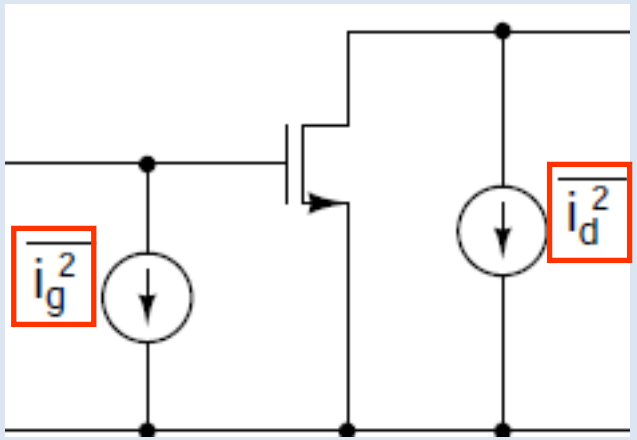
Noise Sources

Resistance



$$\overline{i_R^2} = 4kT/R$$

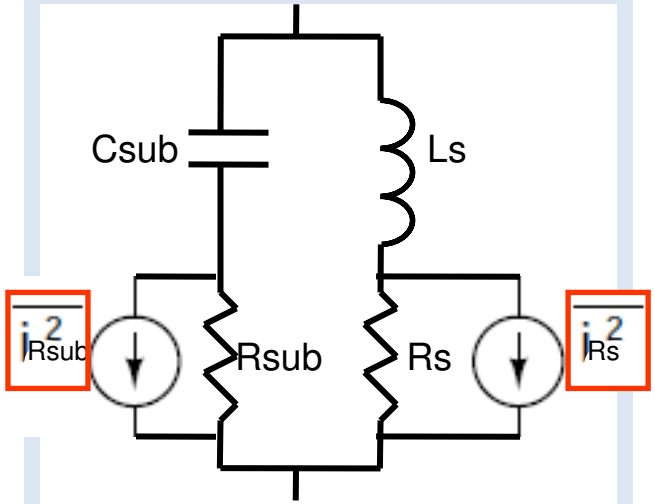
Transistor



$$\overline{i_d^2} = 4kT\,\gamma g_{d0}\Delta f$$

$$\overline{i_g^2} = 4kT\,\delta g_{gs}\Delta f$$

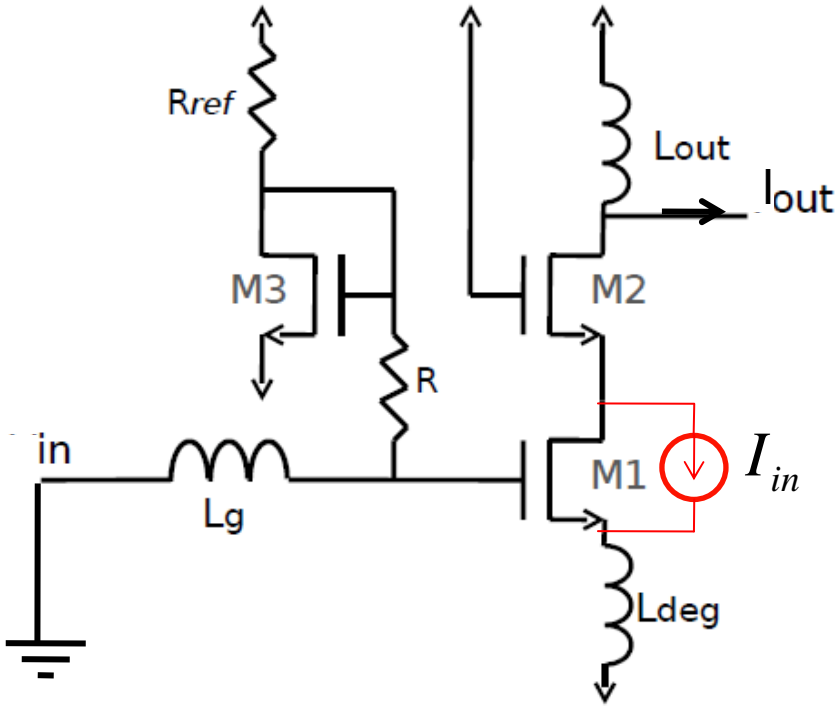
Inductance



$$F = 1 + \frac{N_{o(added)}}{N_{o(source)}}$$

$$NF = f\left(\underbrace{G.N_i}_{N_{o(source)}}, \overbrace{\overline{i_d^2}|H_d|, \overline{i_g^2}|H_g|, \overline{i_R^2}|H_R|, \overline{i_{Rs}^2}|H_{Rs}|, \overline{i_{Rsub}^2}|H_{Rsub}|}^{N_{o(added)}}\right)$$

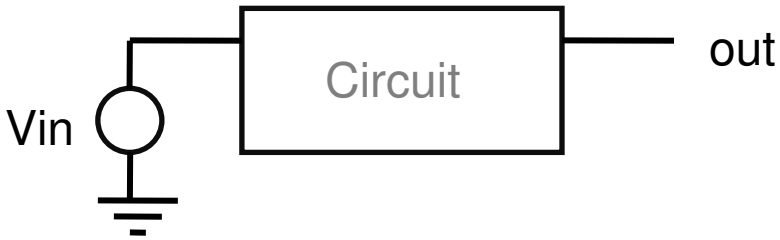
Noise Sources



$$|H_d(s)| = \left| \frac{I_{out}(s)}{I_{in}(s)} \right|$$

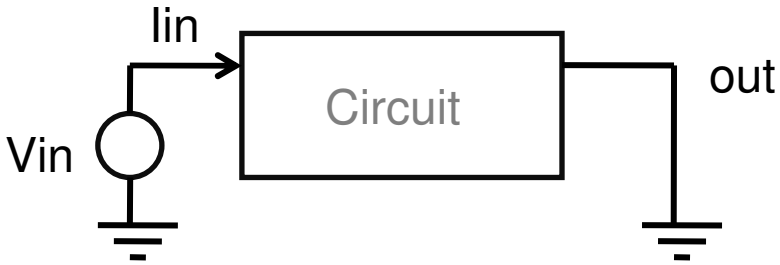
Characterization

Gain :



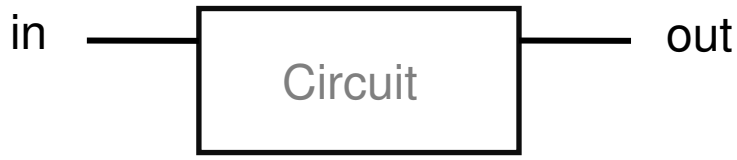
$$Gain(s) = \frac{Vout(s)}{Vin(s)}$$

Input Impedance:



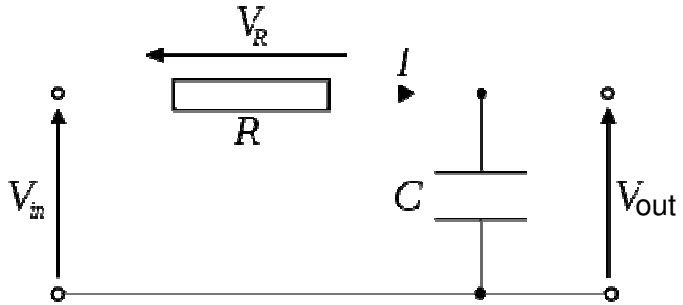
$$Zin(s) = \frac{Vin(s)}{Iin(s)}$$

Noise Factor:



$$F = 1 + \frac{N_{o(added)}}{N_{o(source)}}$$

Characterization Example



$$1) sCV_{out} = \frac{V_{in}(s) - V_{out}(s)}{R}$$

$$2) V_{in}(s) = 1$$

$$\begin{bmatrix} -1/R & 1/R + sC \\ 1 & 0 \end{bmatrix} \begin{bmatrix} V_{in}(s) \\ V_{out}(s) \end{bmatrix} = \begin{bmatrix} 0 \\ 1 \end{bmatrix}$$

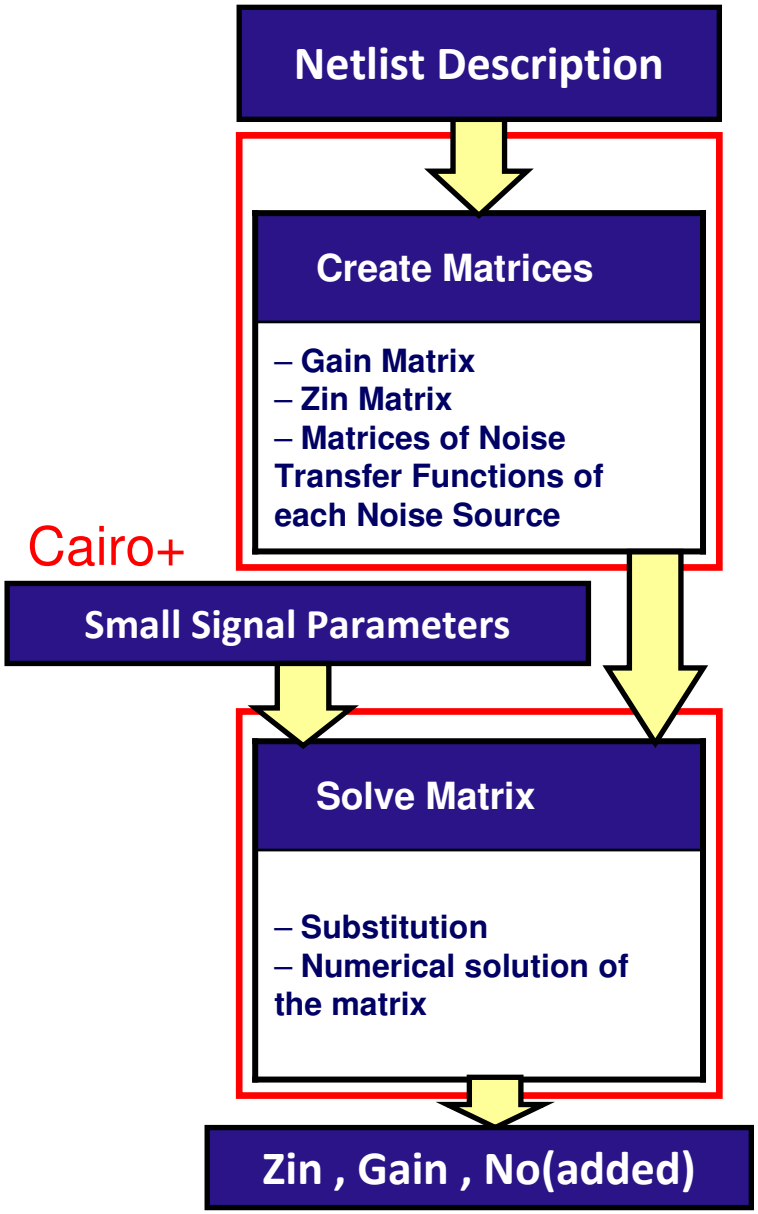
$$\left[\begin{array}{cc|c} -1/R & 1/R + sC & 0 \\ 1 & 0 & 1 \end{array}\right]$$

Gauss-Jordan

$$\left[\begin{array}{cc|c} 1 & 0 & 1 \\ 0 & 1 & 1/(1+sRC) \end{array}\right]$$

$$Gain(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{1+sRC}$$

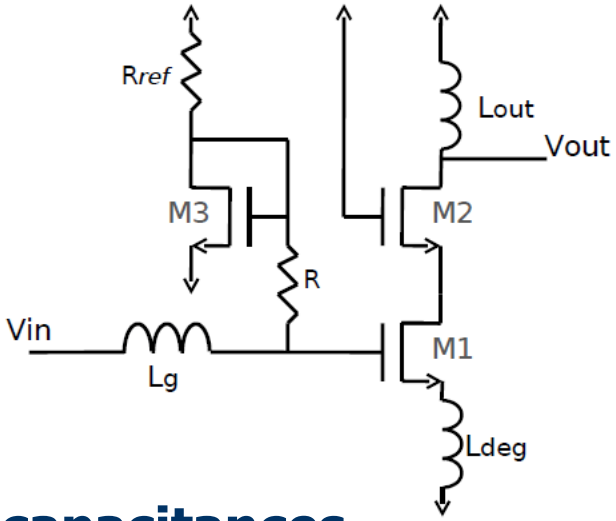
Automatic Characterization Procedure



Maxima

GiNaC (C++)

Design Procedure



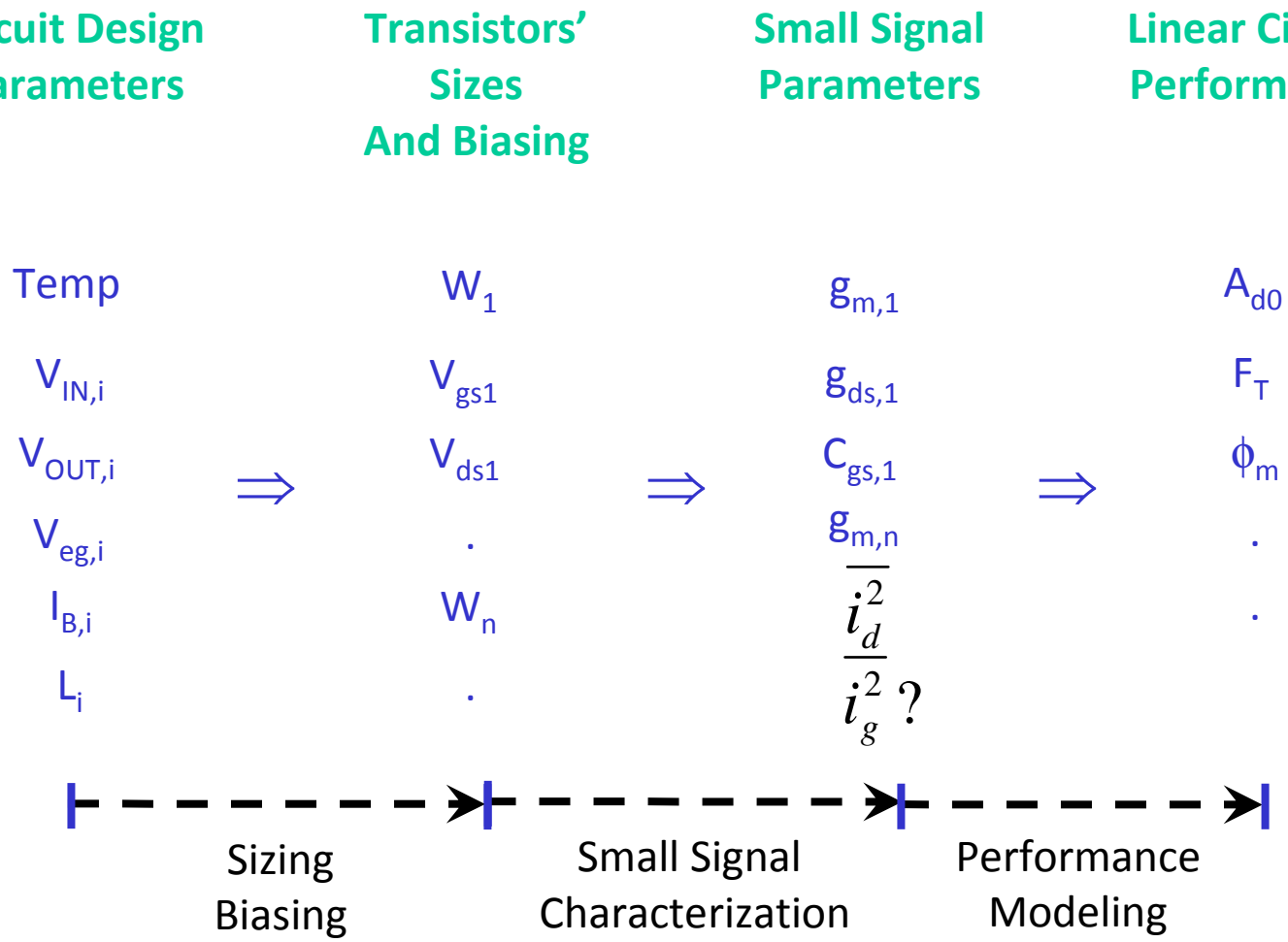
Transistors

- ***Length:*** **Minimum L to reduce parasitic capacitances.**
- ***Width:*** **Ids calculated for NFmin.**
- ***Layout:*** **Maximum number of fingers to reduce Gate resistance.**

Inductors

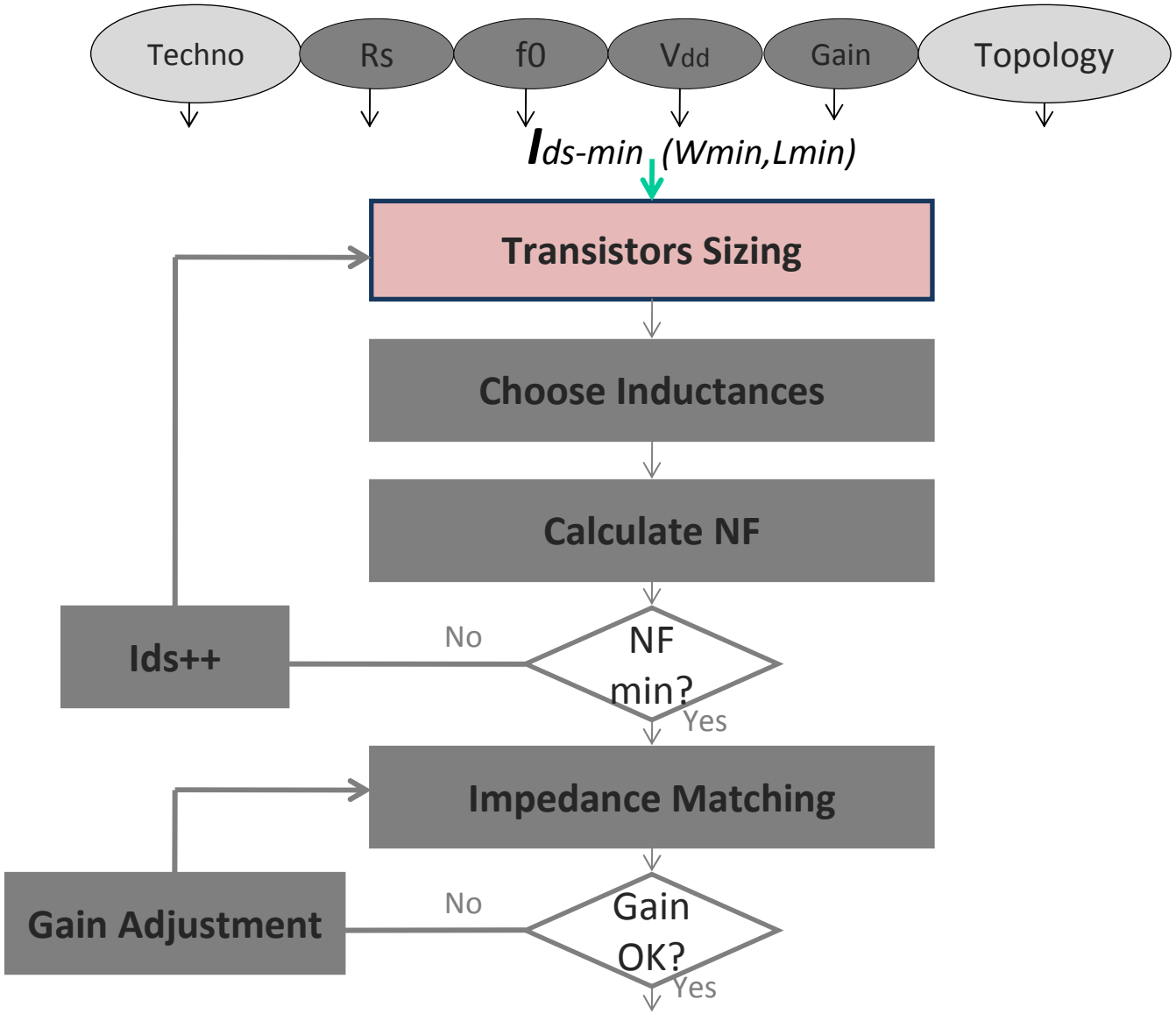
- ***Ldeg : Adjusted for Re*** **{Zin} = 50 Ω .**
- ***Lg : Adjusted for Im*** **{Zin} = 0 Ω .**
- ***Lout : Adjusted for the desired Zout and Gain.***

CAIRO+



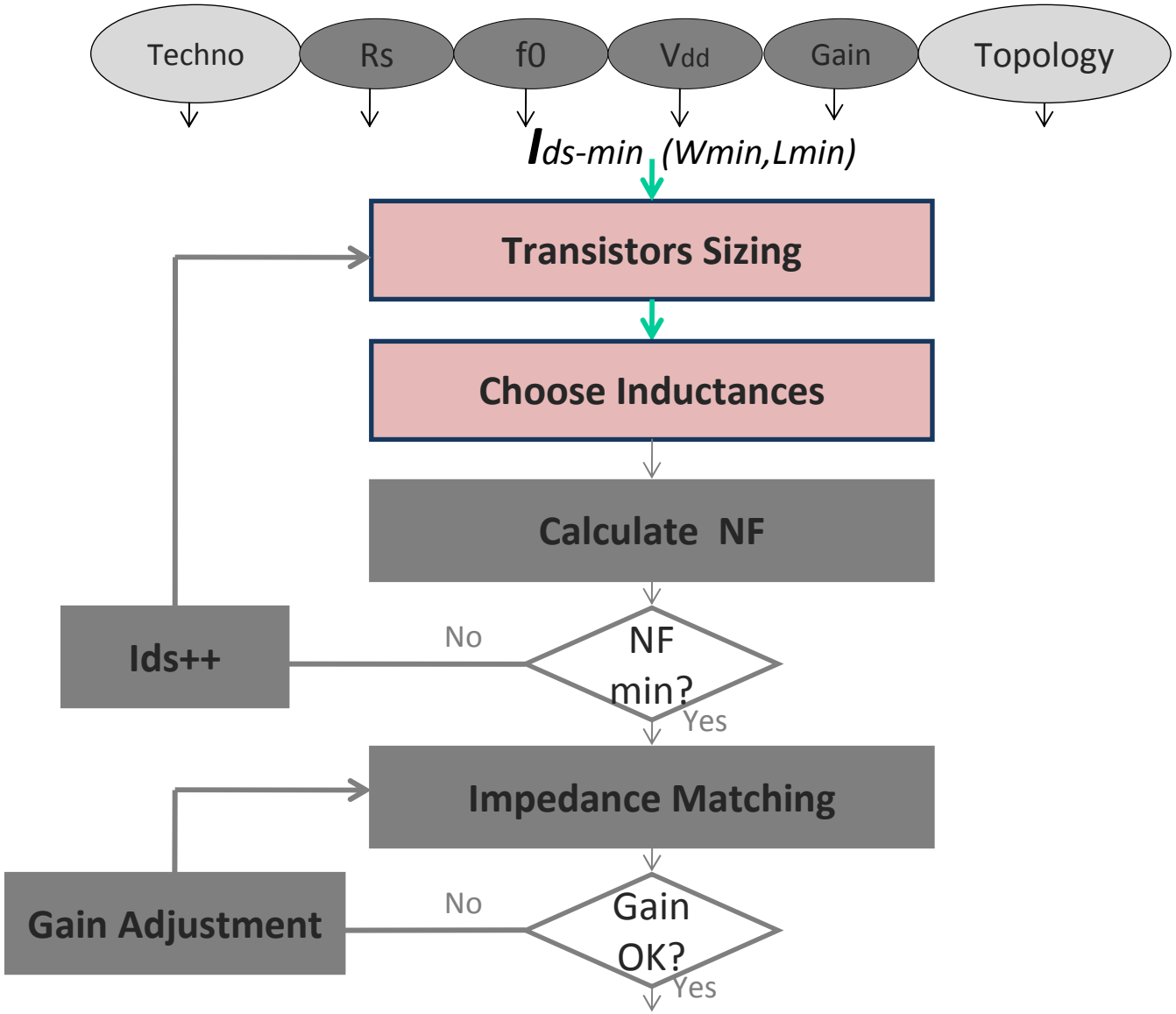
[Ramy ISKANDER "*Knowledge-aware synthesis for analog integrated circuit design and reuse*" Ph.D. Thesis UPMC,LIP6 2008]

Automatic Sizing Procedure



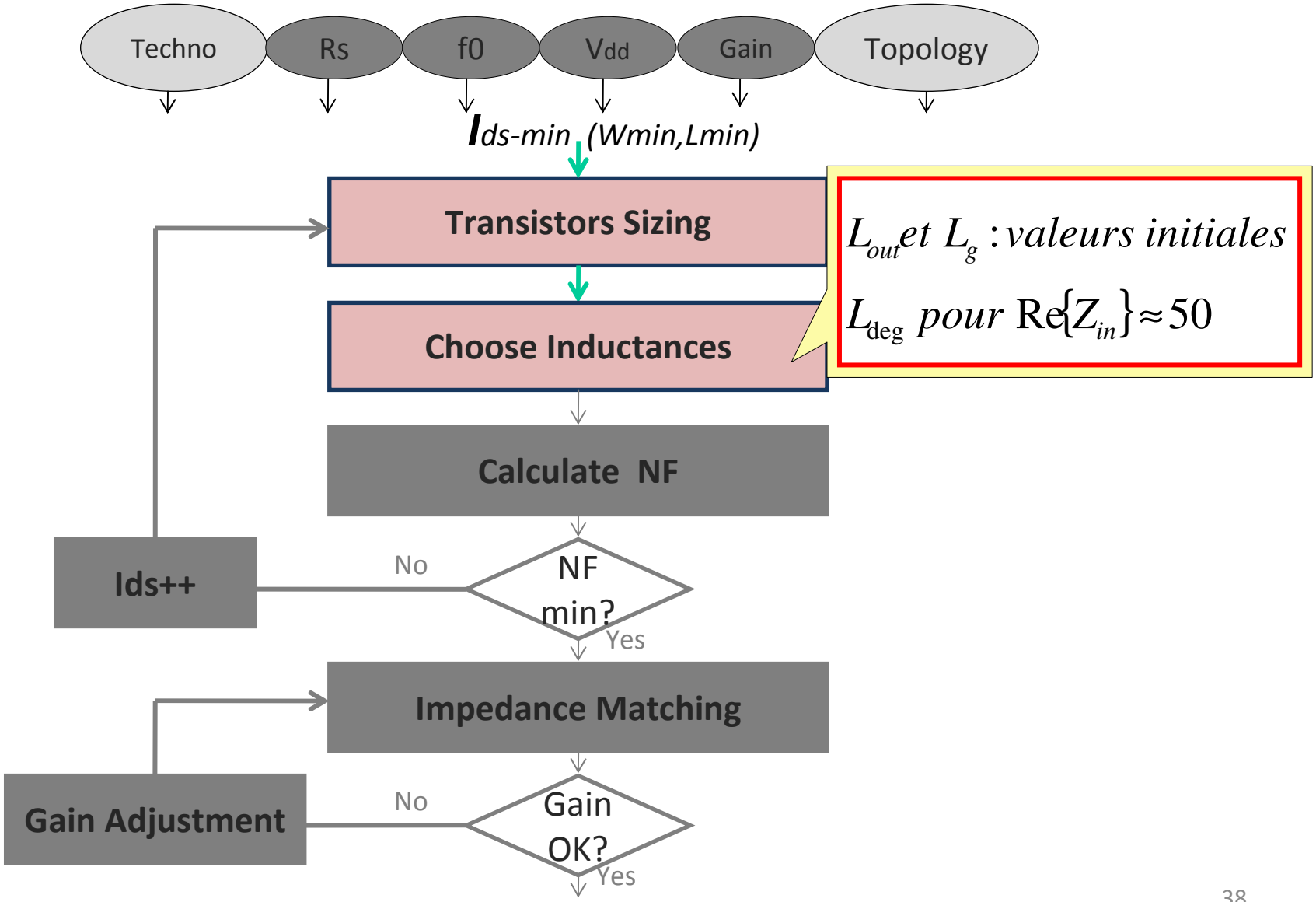
Caracterization of NF , Gain, Zin

Automatic Sizing Procedure



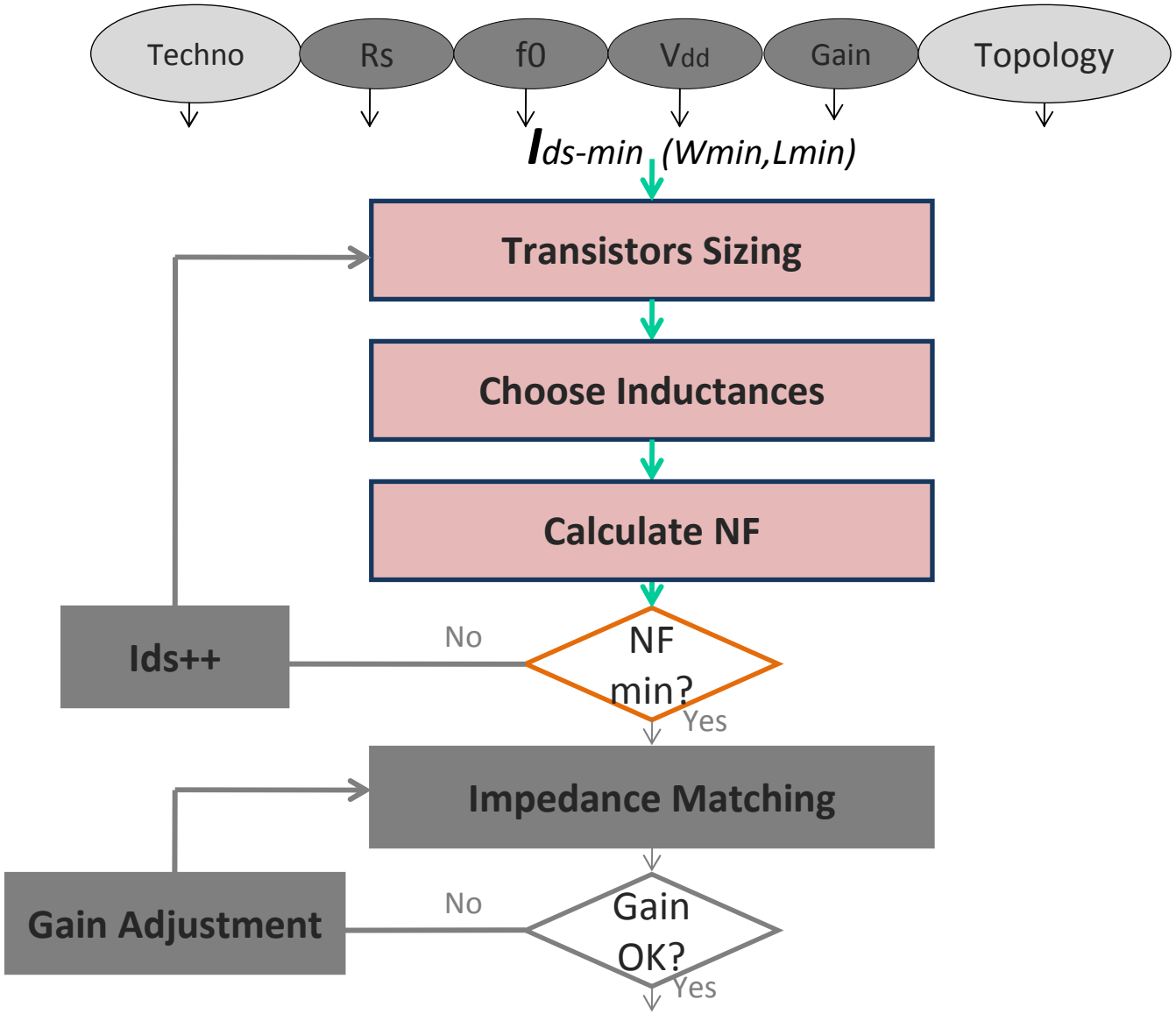
Caractérisation de NF , Gain, Zin

Automatic Sizing Procedure



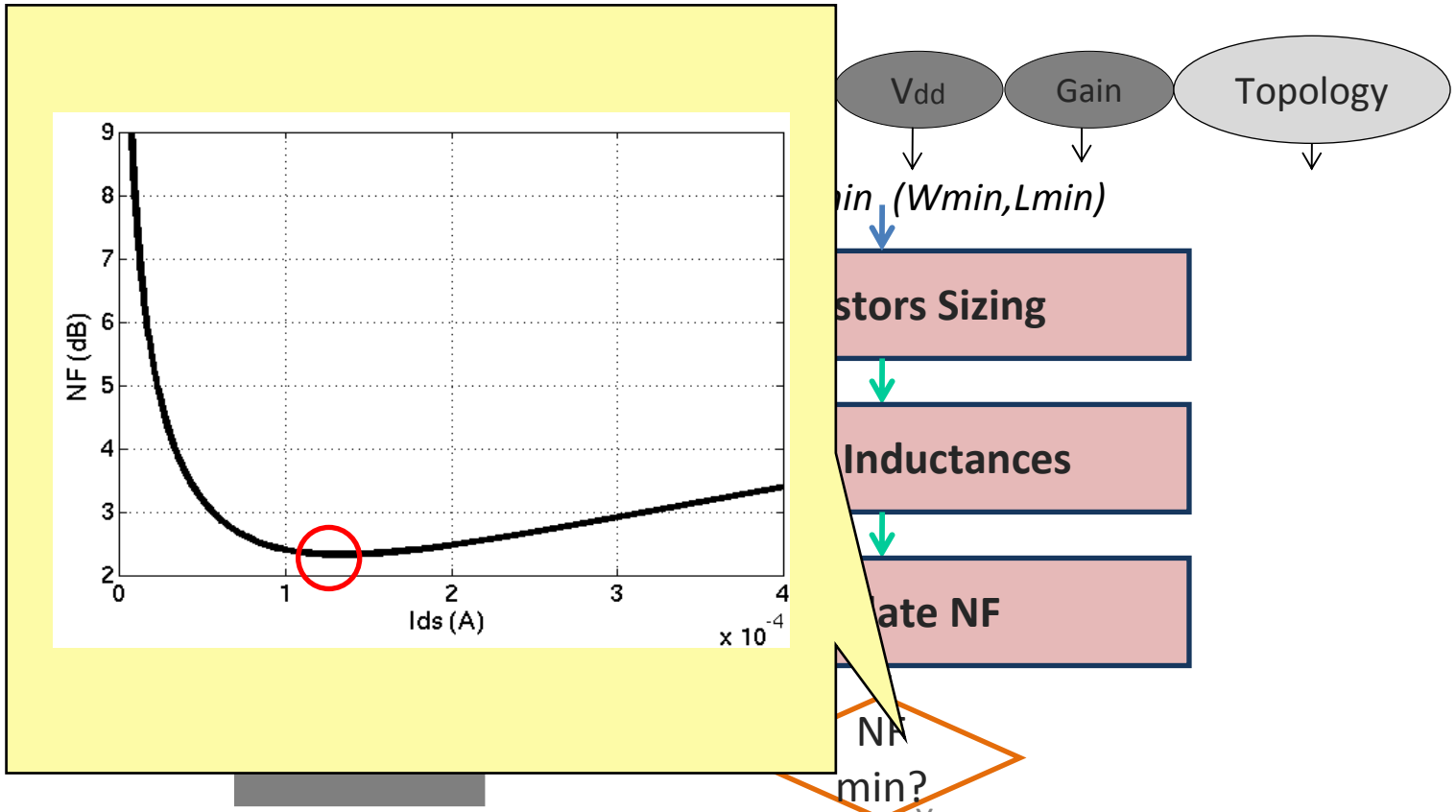
Caracterization of NF , Gain, Zin

Automatic Sizing Procedure



Caracterization of NF , Gain, Zin

Automatic Sizing Procedure



Vdd

Gain

Topology

in (Wmin,Lmin)

stors Sizing

Inductances

ate NF

NF min?

Yes

Impedance Matching

Gain Adjustment

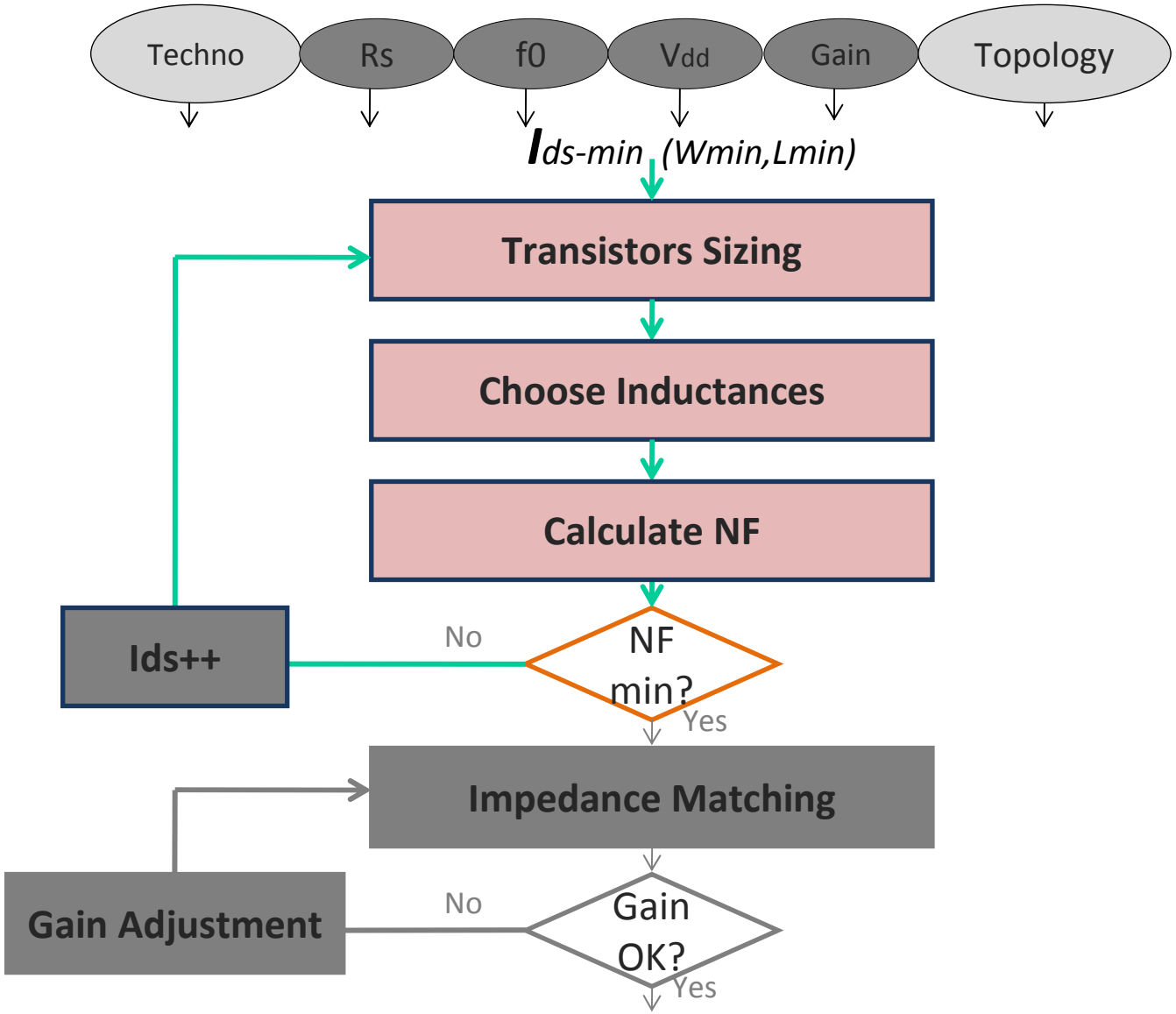
No

Gain OK?

Yes

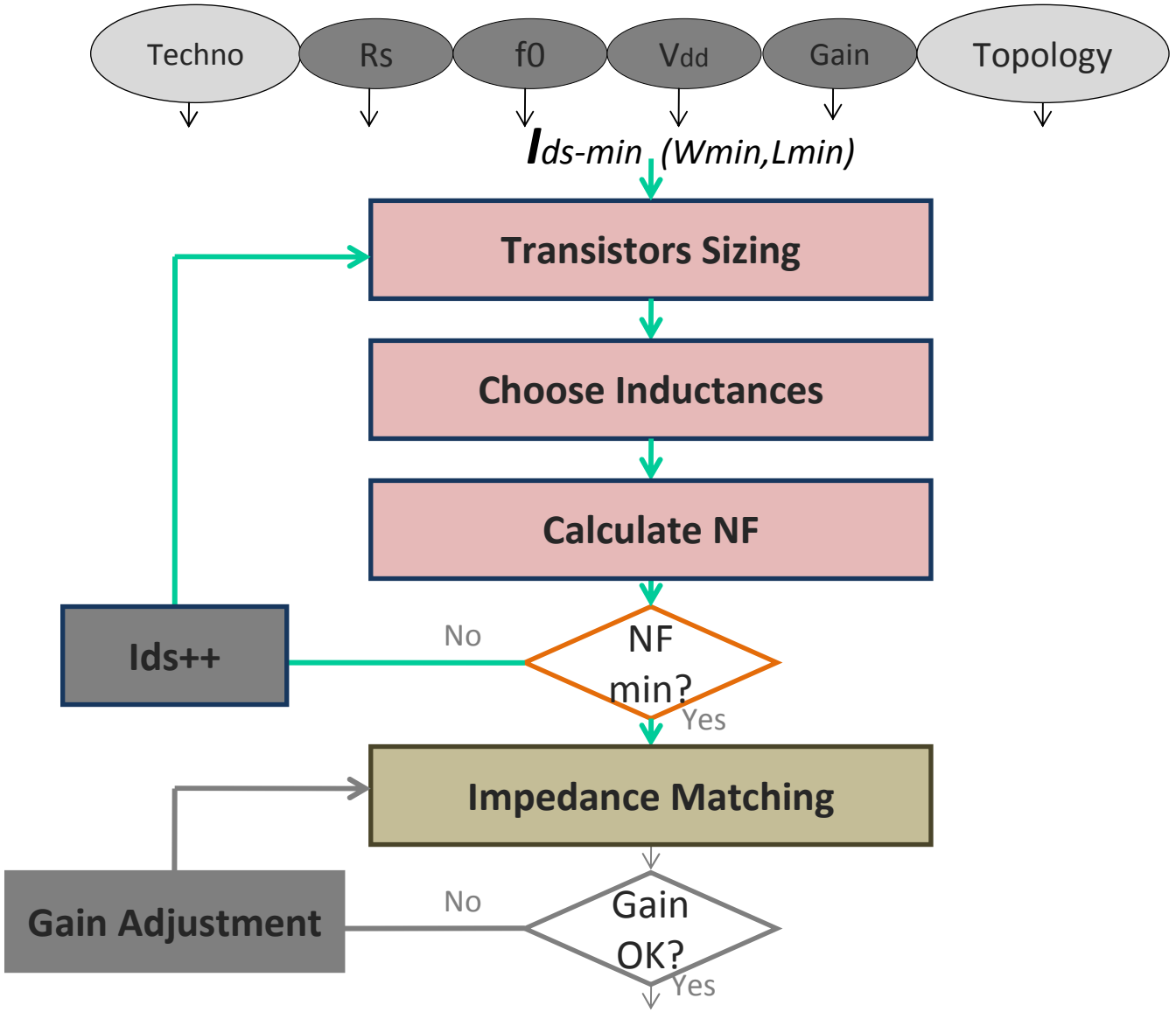
Caracterization of NF , Gain, Zin

Automatic Sizing Procedure



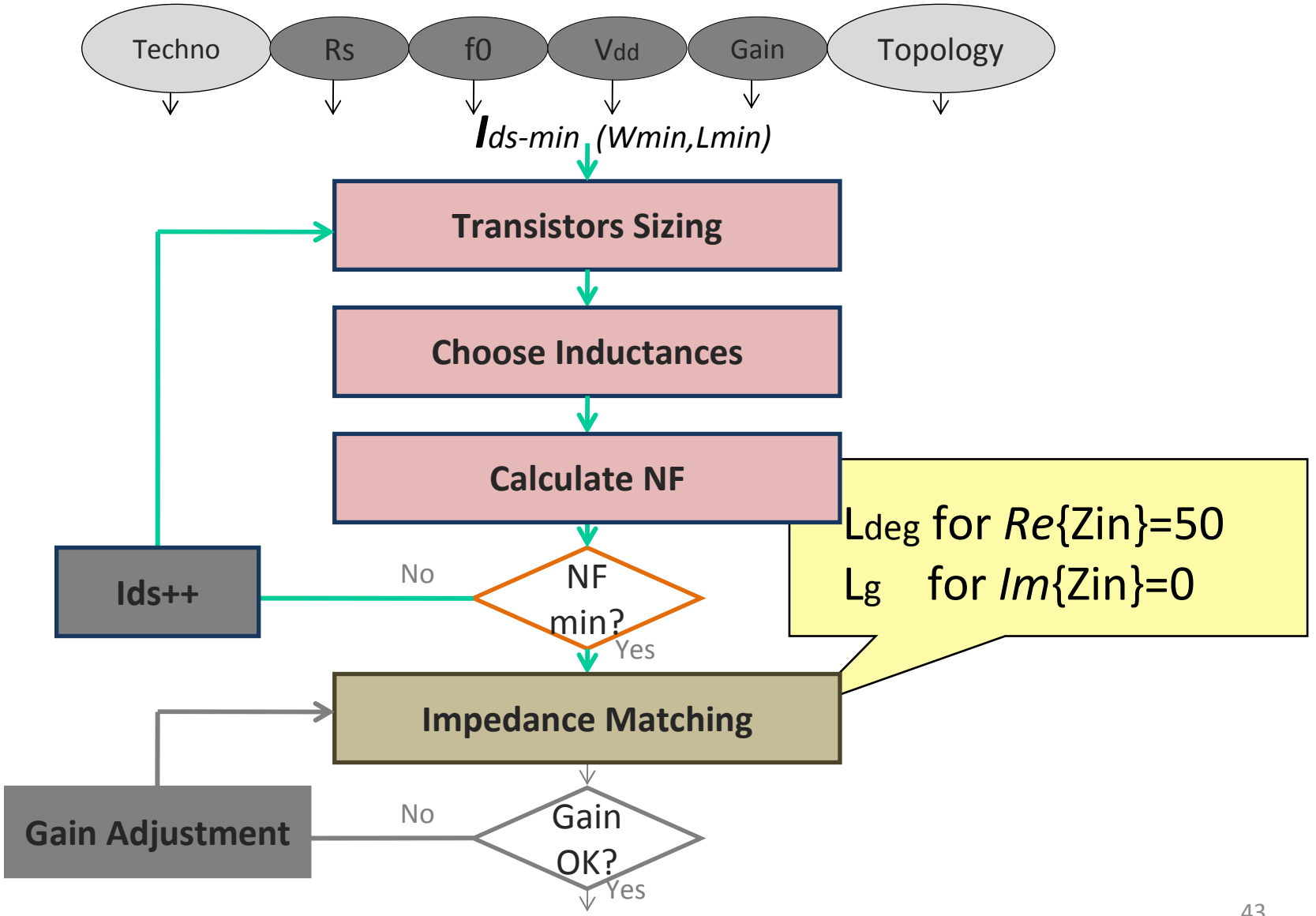
Caracterization of NF , Gain, Zin

Automatic Sizing Procedure



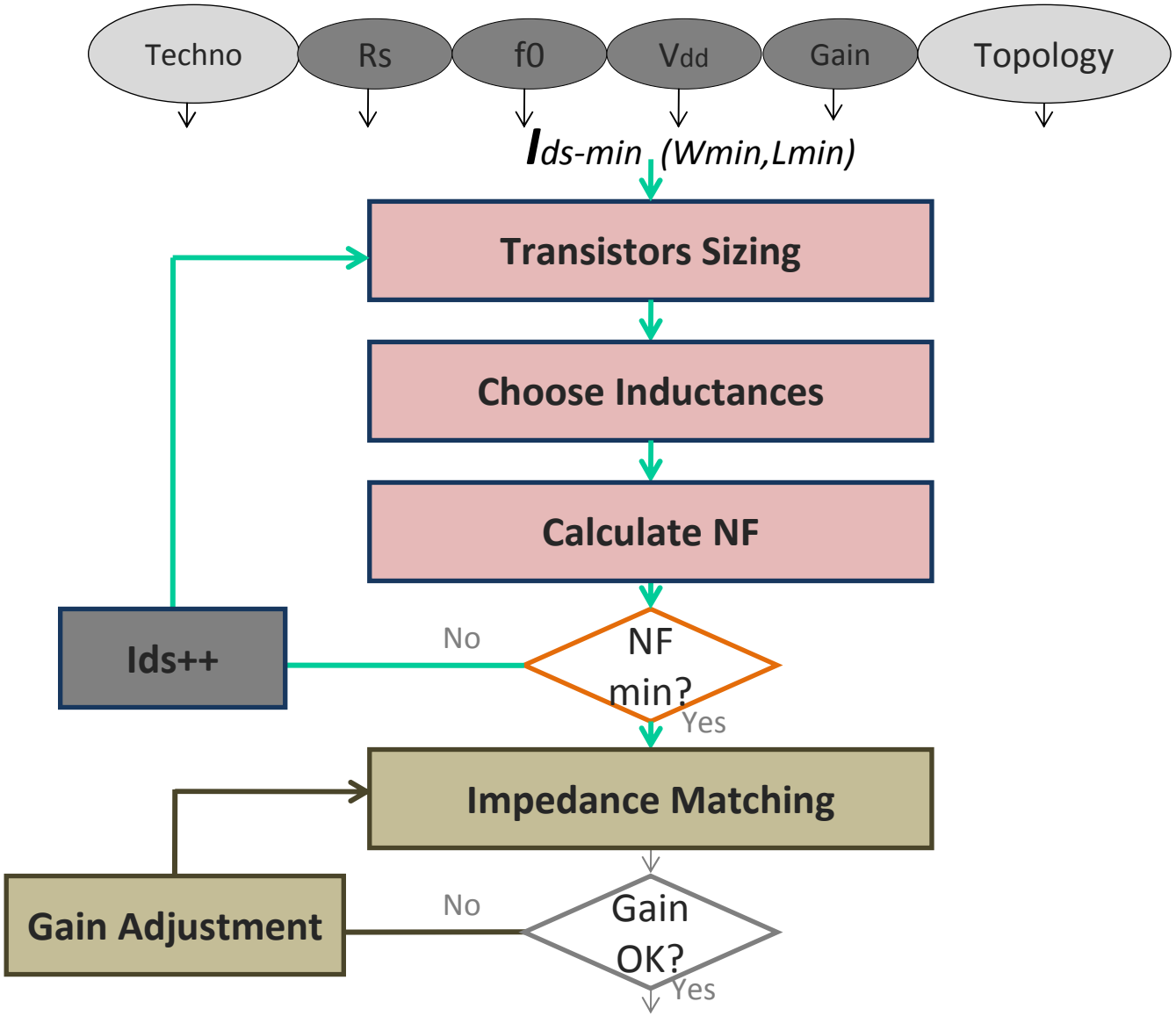
Caracterization of NF , Gain, Zin

Automatic Sizing Procedure



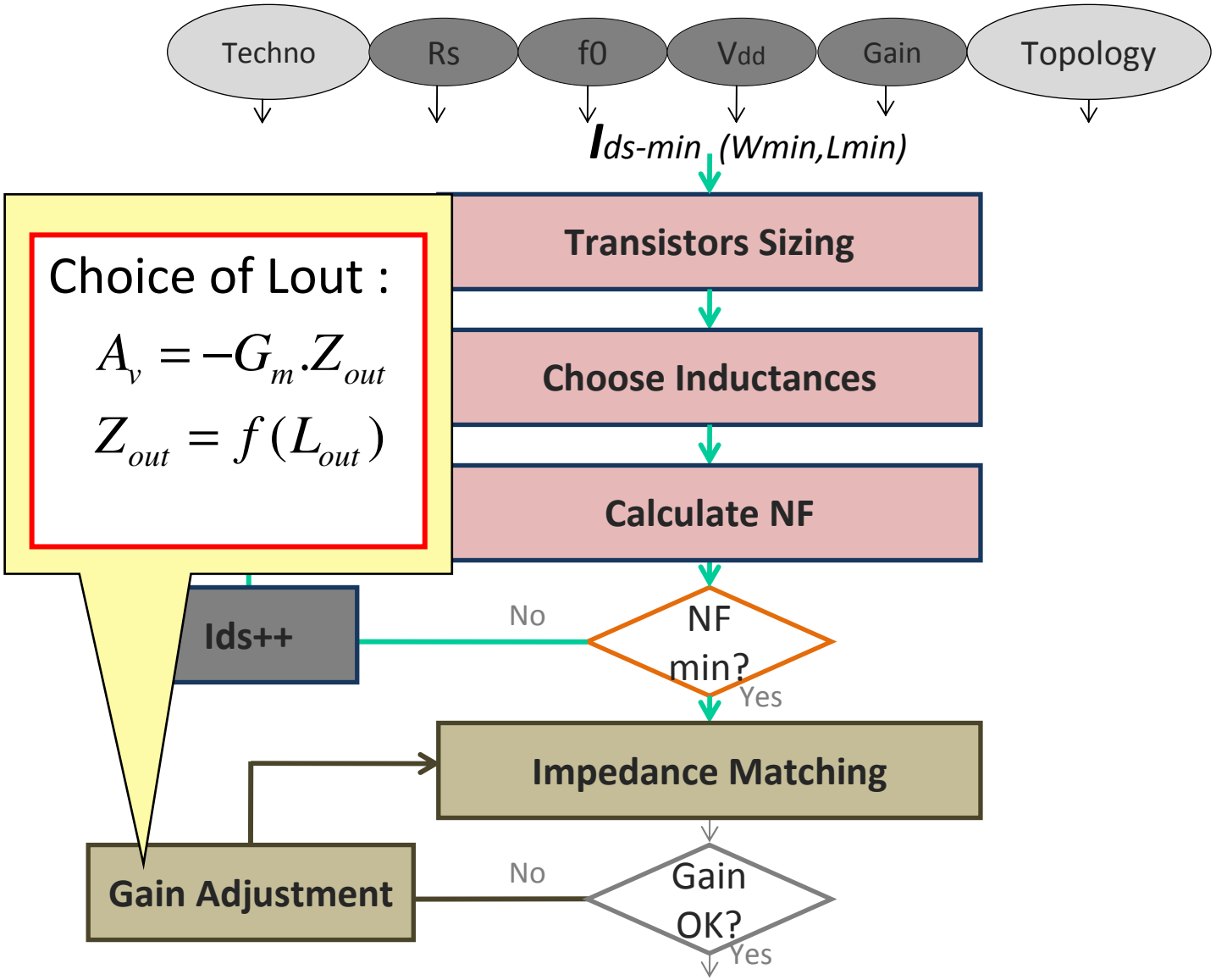
Caracterization of NF , Gain, Zin

Automatic Sizing Procedure



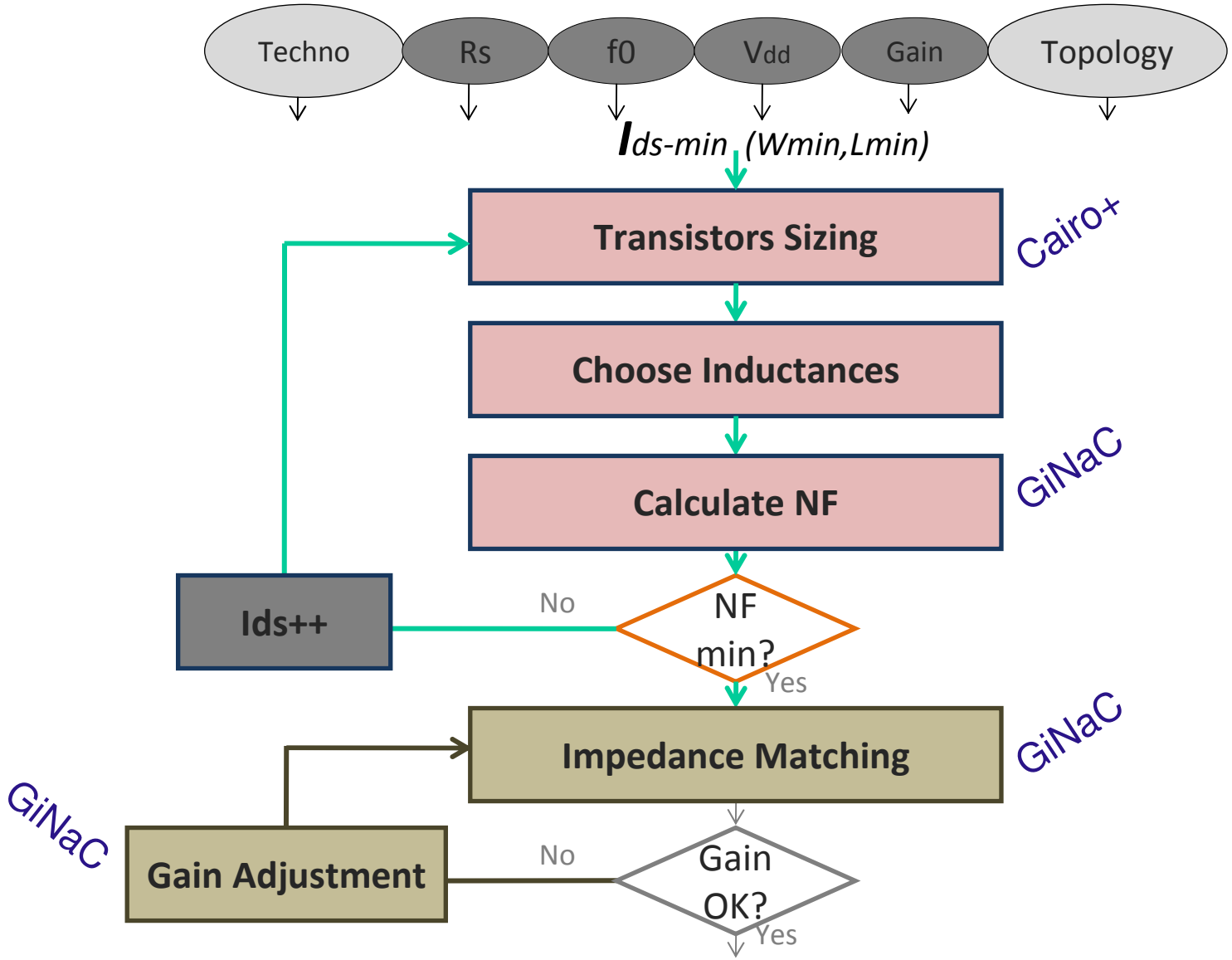
Caracterization of NF , Gain, Zin

Automatic Sizing Procedure



Caracterization of NF , Gain, Zin

Automatic Sizing Procedure

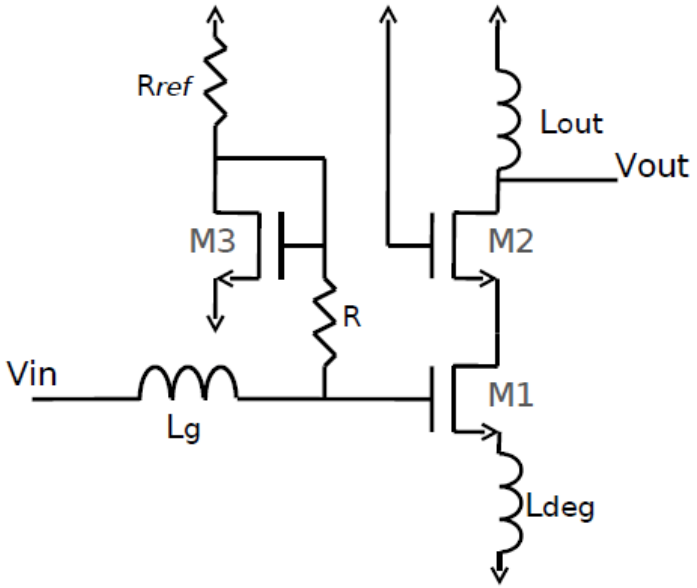


Caracterization of NF , Gain, Zin

Matching Input Impedance

- Introduction
- Les paramètres de conception
- Circuit proposé
- Méthode de conception
- Caractérisation automatique
- Conception automatique
- Exemple de conception

Design Example I: A 2.4GHz LNA in 130 nm CMOS



Spécifications

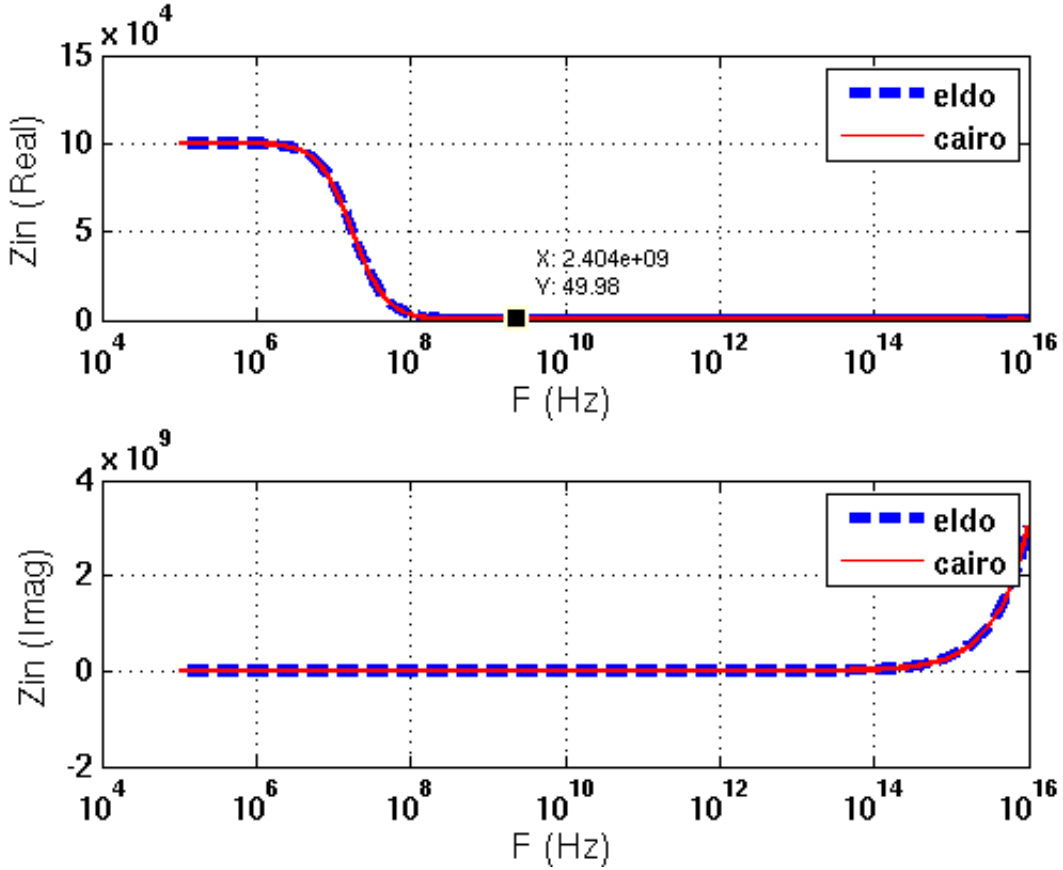
Technologie	0.13 um
Vdd	1.2 V
Résistance de source (Rs)	50 Ω
Fréquence centrale (f_0)	2.4 GHz
Gain	≥ 15 dB

Résultats de la procédure proposée

	W (um)	L (um)	Vgs (V)	Vds (V)	Ids(mA
M1	48.96	0.13	0.6	0.6	3.3122
M2	48.96	0.13	0.6	0.6	3.3122
M3	5.08	0.13	0.6	0.6	0.33122

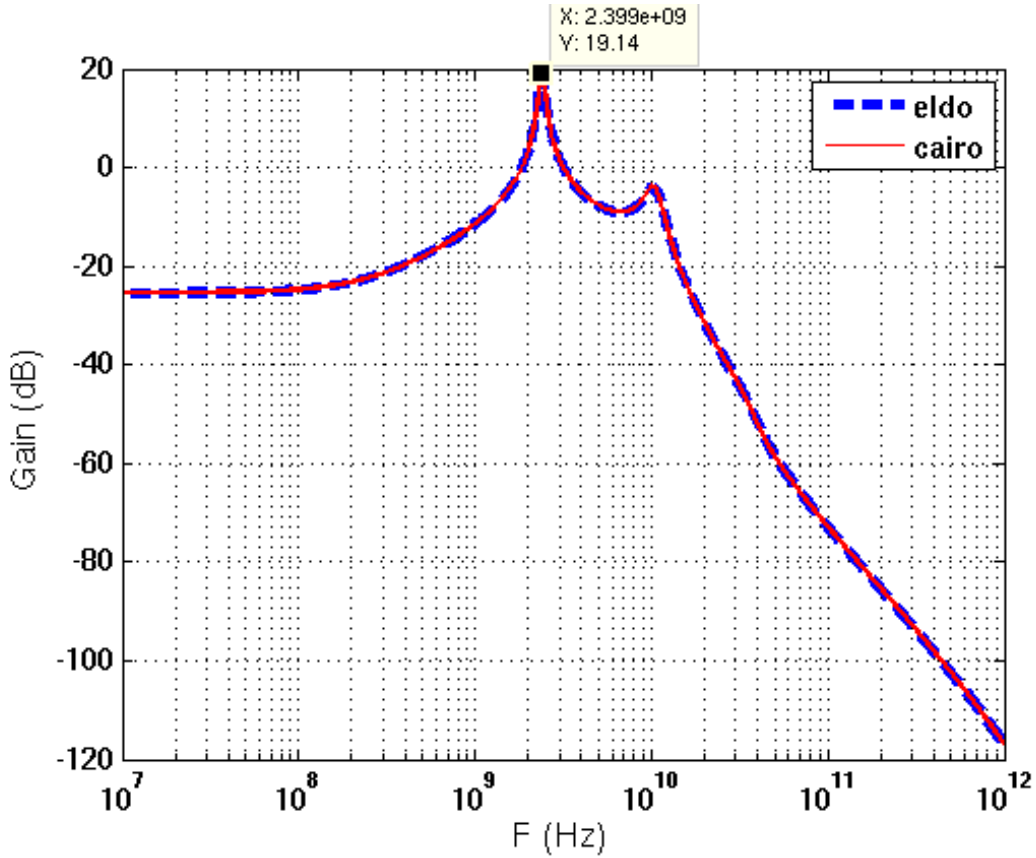
R= 100 KΩ , Rref = 1.811 KΩ , Ldeg = 0.3709 nH , Lg = 48.65 nH , Lout = 3 nH

Estimated and Simulated Input Impedance



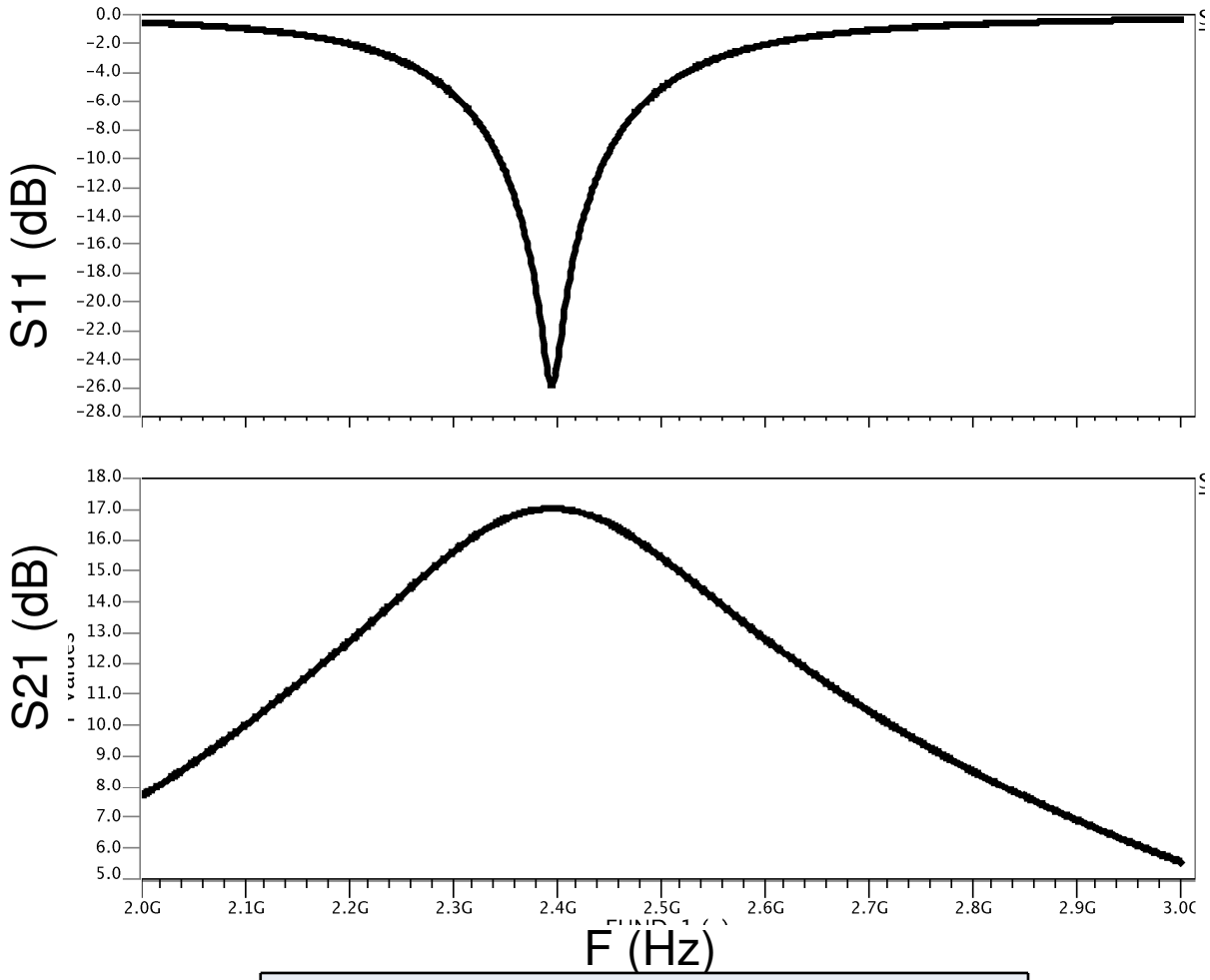
Zin (Cairo+) (Ω)	Zin (ELDO) (Ω)
50.00	49.57

Estimated and Simulated Gain and NF



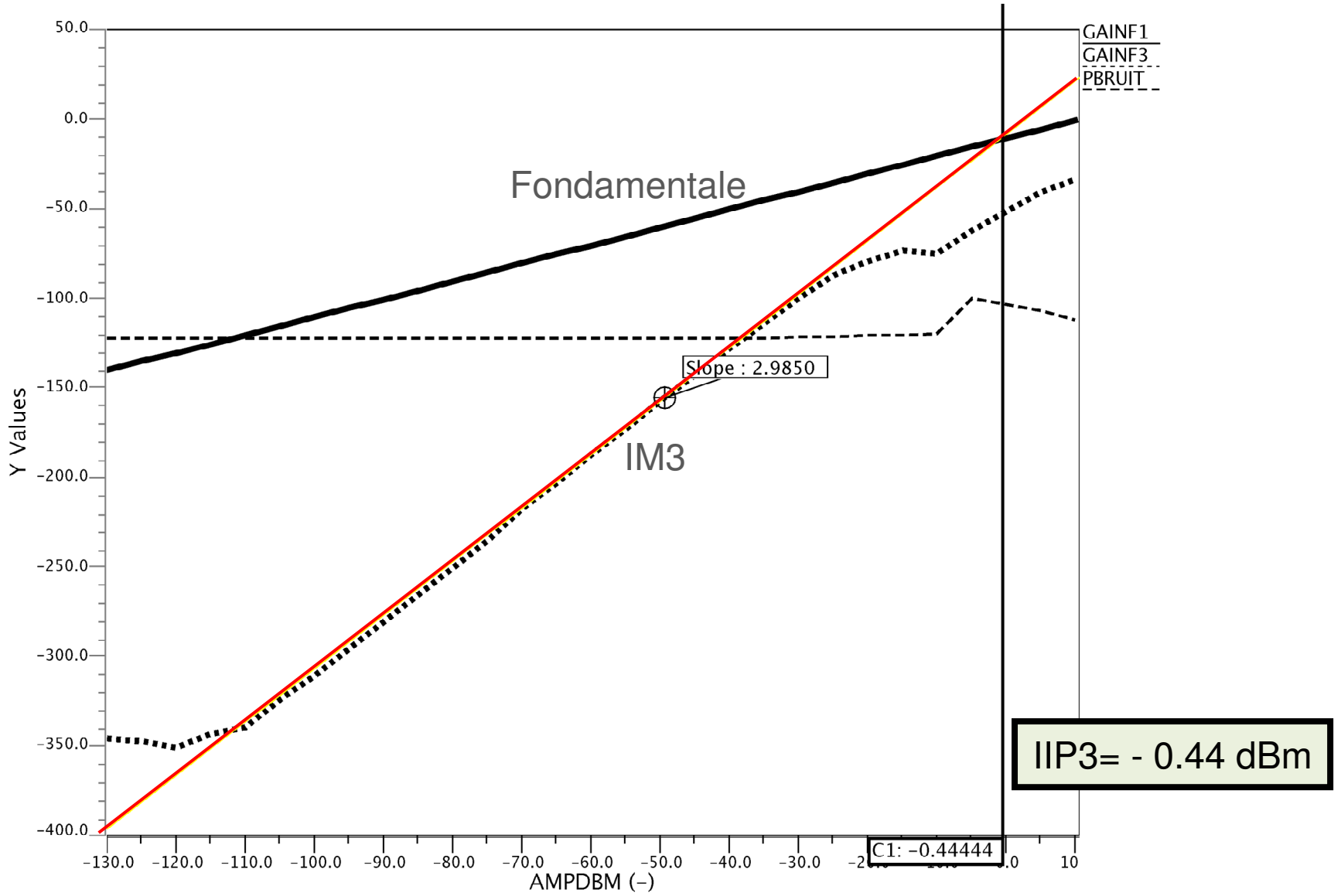
	Gain (dB)	NF (dB)
Cairo+	19.14	0.774099
ELDO	19.04	0.727277

Simulated S Parameters



S11 @ 2.4 GHz =-24.24 dB
S21 @ 2.4 GHz = 17.028 dB

Simulated IIP3



IIP3= - 0.44 dBm

Comparison with state of the art

$$FOM = 10\log\left(100\left(\frac{|S_{21}|_{(lineaire)} f_0^2}{(F-1)P_{dc(mW)}}\right)\right)$$

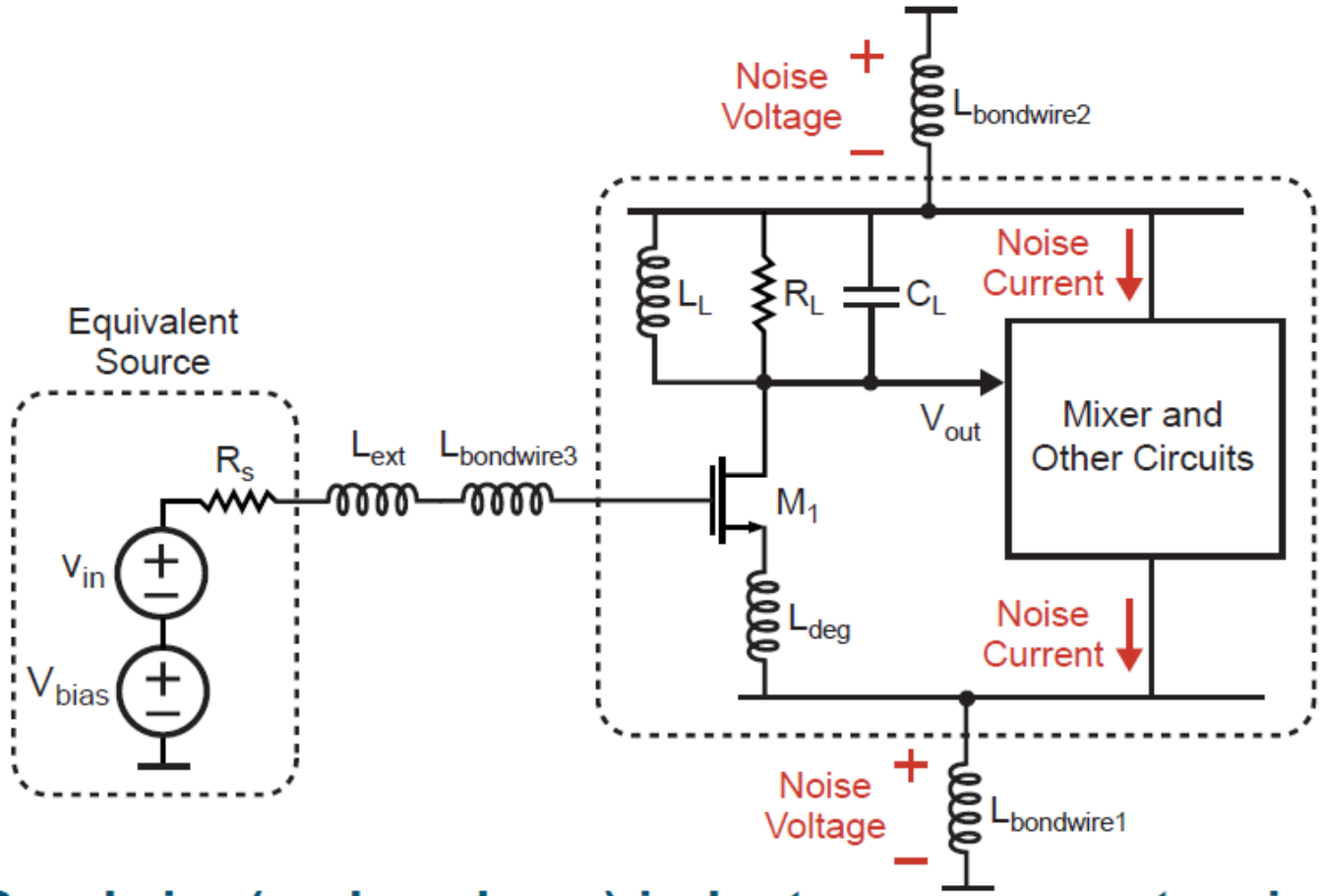
[Chandrasekhar 2002]

	Techno. (um)	NF (dB)	IIP3 (dBm)	Gain (dB)	S_{11} (dB)	S_{21} (dB)	P_{in} (mW)	V_{dd} (V)	I_{ds} (mA)	f_0 (Hz)	FOM
[1]	0.25	1.7	1.5	15	-	15	12	2.5	5	2G	205.92
[2] *	0.35	0.43	-2.87	19.8	-18	16	20	-	-	2.4G	212.42
[3]	0.18	0.77	-12.2	21.6	-17.7	-	11.2	1.8	-	2.4G	215.03
[4]	0.35	1.52	-4.3	20.2	-10.3	-	12.5	-	-	2.4G	210.51
[5]	0.25	2.5	0.5	14.7	-19.5	14.7	1.97	2	-	2.4G	213.09
[6]	0.13	0.76	-2.5	12	-6.5	12	4.2	1.2	3.5	2.14G	213.56
This work*	0.13	0.72	-0.44	19.04	-24.24	17.02	3.8	1.2	3.16	2.4G	217.75

(*) résultats de simulation

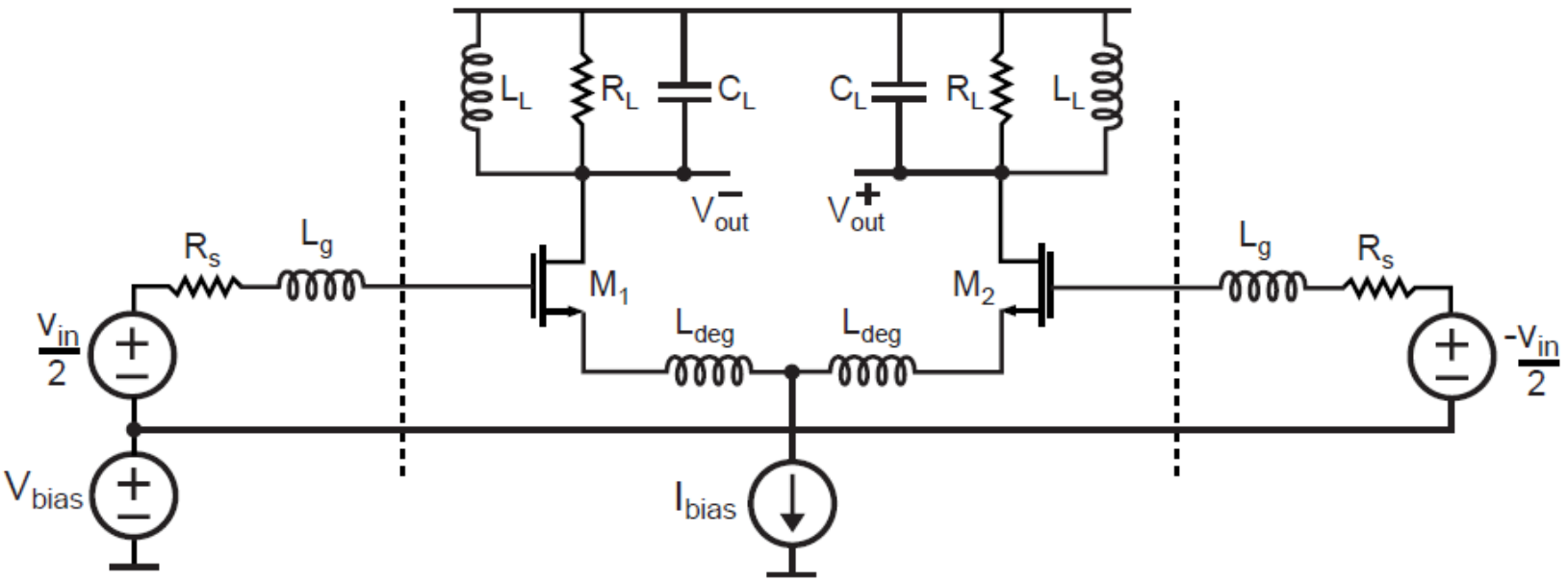
[V. Chandrasekhar, C.M. Hung, Y.C. Ho, and K. Mayaram. “A Packaged 2.4GHz LNA in a 0.15umCMOS Process with 2kV HBM ESD Protection” , ESSCIRC, 2002]

The Issue of Package Parasitics



- **Bondwire (and package) inductance causes two issues**
  - **Value of degeneration inductor is altered**
  - **Noise from other circuits couples into LNA**

Differential LNA



- **Advantages**
  - Value of L_{deg} is now much better controlled
  - Much less sensitivity to noise from other circuits
- **Disadvantages**
  - Twice the power as the single-ended version
  - Requires differential input at the chip