Automatic Synthesis and Simulation of Continuous-Time ΣΔ Modulators

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Abstract

This paper presents a mixed equation-based and simulation-based design methodology for continuous-time Sigma-Delta modulators from high level specifications down to Layout. The calculation and scaling of the Sigma-Delta coefficients as well as circuit sizing and layout generation are implemented in the same analog design environment CAIRO+. The design of a complete third order current-mode continuous-time Sigma-Delta modulator is taken as an example to show the effectiveness of the proposed design methodology.

1. Introduction

In this paper, we present a top-down design methodology for Continuous-Time (CT) ΣΔ modulators. The design methodology is mainly equation-based. Simulation is used in the system level to scale the calculated CT coefficients. In the circuit level, simulation is used to estimate harmonic distortion. It is shown that circuit non-linearity can be reduced only by modifying the CT ΣΔ coefficients and without increasing the power consumption. As shown in Figure 1, having almost all the calculations and simulations integrated in the same design environment permits strong interaction and optimization between the different design levels.

2. System-level synthesis

2.1 Equation-based synthesis of CT ΣΔ

A systematic technique for DT-to-CT transformation, based on the modified-z-transform technique, is used to get the CT ΣΔ coefficients [1]. Using a symbolic mathematical tool, it is possible to obtain the CT coefficients expressed in function of the DT coefficients and the feedback signal characteristics.

2.2 Simulation-based scaling of CT ΣΔ

Since ΣΔ modulators are non-linear systems, simulation is usually involved in the design procedure. In the CAIRO+ environment, functions have been developed in order to perform simulation of ideal CT ΣΔ modulators. Functions for Fast Fourier Transform (FFT) and Signal to Noise Ratio (SNR) calculation are also available for the analysis of the output signal.

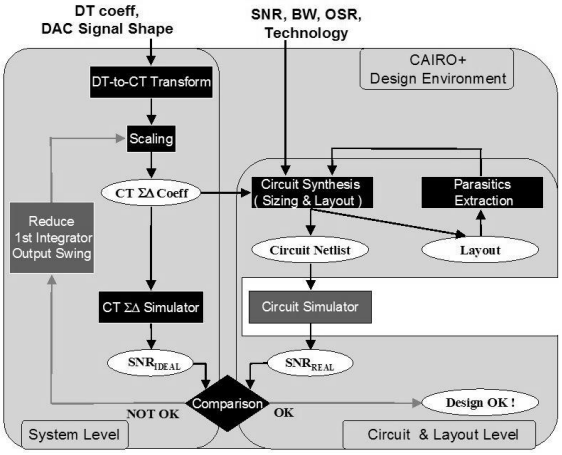

Figure 1. CT ΣΔ modulator synthesis in the CAIRO+ design environment.

Coefficients resulting from the DT-to-CT transformation tables, described in section 2.1, ensure that both Noise Transfer Functions (NTF) of the DT and CT systems are identical. On the other hand, these coefficients do not take into account any circuit limitations. These coefficients do not ensure that the integrators outputs are limited to the maximum signal swing permitted by the circuit realizing the integrators. Due to the non-linearity of ΣΔ systems, the integrators output swing are difficult to predict mathematically and are then estimated by simulation. In [2], a systematic simulation-based technique to scale the CT ΣΔ coefficients for limited integrators output swing is presented.

3. Circuit-level synthesis

3.1 Equation-based synthesis

Design procedures used to synthesize current-mode integrators, feedback DACs and comparators of CT ΣΔ mod-

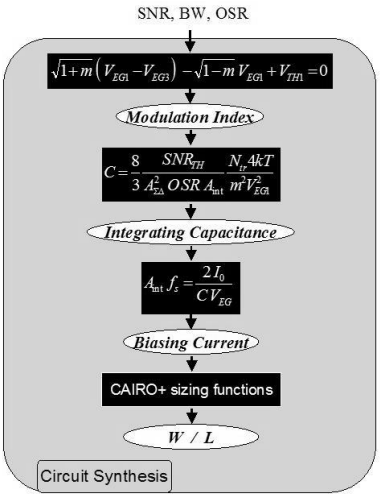

Figure 2. Integrator synthesis procedure.

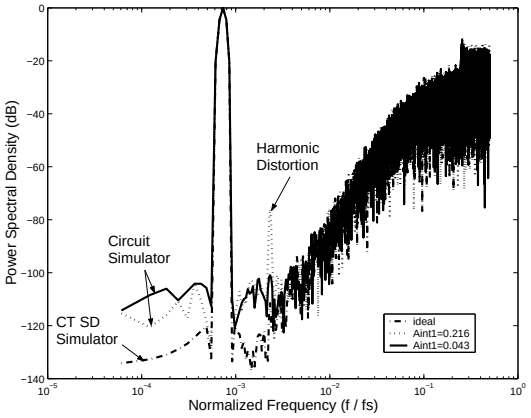

Figure 3. Comparison between ideal system-level ΣΔ simulation & circuit level simulation.

ulator have been presented in [3][4]. As shown in Figure 2, biasing currents and voltages are calculated using simplified MOS transistor models. Transistors' dimensions are then calculated using the accurate BSIM3v3 models integrated in CAIRO+ sizing functions. Using these functions, we can generate complete sized netlists of the entire circuit. Although the generated integrators satisfy the required Signal-to-Thermal Noise Ratio, the sizing procedure does not take integrators' non-linearity into account. The main source of harmonic distortion in current-mode integrators, is g_m variation with the input current. An approximate expression for the transconductance $g_m(t)$ in function of the nominal transconductance g_{m_0}, the input current $i_{in}(t)$, the biasing current I_0 and the integrator gain A_{int} is:

$$g_m(t) = g_{m_0}\sqrt{1+\frac{A_{int}}{I_0}\frac{1}{T}\int_0^t i_{in}(t)\;dt} \qquad (1)$$

From equation (1), we can see that it is possible to reduce the transconductance nonlinearity either by increasing the biasing current I_0 or by decreasing the integrator gain A_{int}. In a low-power design, it is preferable to decrease the integrator gain A_{int}. If A_{int} is changed, all the coefficients of the ΣΔ modulator must be scaled in order to preserve the same NTF.

Note that, although equation (1) is useful to identify the design parameters that influence the non-linearity of the integrator, it is very difficult to use this equation to estimate harmonic distortion of the CT ΣΔ modulator.

3.2 Simulation-based optimization

Circuit simulation is used to measure harmonic distortion due to the non-linearity of the integrator circuit. The simulated circuit consists of a CT ΣΔ modulator using sized netlists of the integrators along with ideal models for the comparator and feedback DACs. FFT_{REAL} and SNR_{REAL} calculations are performed on the simulation output. The CT ΣΔ simulator described in section 2.2 is used to obtain FFT_{IDEAL} and SNR_{IDEAL}. The results of the system level simulation and circuit level simulation are compared. If $SNR_{REAL} < SNR_{IDEAL}$, the gain of the 1st integrator is reduced and the remaining coefficients are scaled in order to maintain the same NTF. Another circuit is then generated for the new coefficients. These steps are repeated until the difference between SNR_{REAL} and SNR_{IDEAL} is small. This optimization procedure is described in Figure 1.

Figure 3 shows the results of such an optimization for a third-order continuous-time ΣΔ modulator. We can clearly see the large amplitude of the third harmonic for the first simulation done with coefficients scaled for maximum signal swing ($A_{int_1} = 0.216$). After several iterations, we find a suitable value ($A_{int_1} = 0.043$) which attenuates the third harmonic and gives an SNR_{REAL} very close to SNR_{IDEAL}.

4. Layout Synthesis

Layout is generated using layout templates with dedicated device generators. Relative placement and routing of devices and sub-circuits is described in a completely hierarchical structure.

References

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