Using excess loop delay to simplify LC-based ΣΔ modulators

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The excess loop delay in continuous-time LC-based ΣΔ modulators, which usually has negative effect on the stability and the signal-to-noise ratio of the modulator, can be used to simplify the modulator architecture and reduce the number of needed feedback branches. The proposed technique is discussed and validated using a design example of a fourth-order bandpass continuous-time LC-based modulator.

Introduction: Bandpass continuous-time (CT) ΣΔ analogue-to-digital converters (ADCs) that work at RF frequencies are receiving increasing attention, as they are considered a promising technique for realising software defined radio (SDR). Bandpass CT ΣΔ ADCs can achieve a reasonable dynamic range by converting only the band of interest around the desired centre frequency. Thus, the direct digitisation of the RF signal is possible and almost all the signal processing can be done in the flexible and programmable digital domain.

LC filters are usually chosen as the loop filter of RF ΣΔ ADC owing to their higher speed and dynamic range compared to their Gm-C and RC counterparts [1–5]. However, for LC-based modulators, the number of available nodes for feedforward or feedback coefficients is half the modulator order, while the number of the needed feedback DAC coefficients is equal to the modulator order [2]. To restore the needed degrees of freedom, more branches have to be added. One technique is to add an extra low-Q resonator in the feedforward path [3]. Another way to increase the degrees of freedom is to use a multi-feedback DAC, where a delayed replica of the DAC is added to the original DAC as in [4], or an integrator DAC is added as suggested in [5]. The multi-feedback DAC technique was generalised to FIR-DAC in [6], where the single coefficient DAC is replaced with a multi-coefficient FIR-DAC.

The common disadvantage of all these design approaches is the increased complexity of the DAC circuitry, which is usually accompanied by increased power consumption and thermal noise power. As the DAC is connected directly to the input node of the modulator, its thermal noise is not shaped by the loop filter, and can be the bottleneck for the overall signal-to-noise ratio (SNR) of the modulator. The objective of this work is to reduce the number of feedback DAC coefficients, while keeping the same noise transfer function (NTF) of the modulator.

Proposed design technique: To present the design idea, we use the common example of a fourth-order BP CT ΣΔ modulator shown in Fig. 1 [6]. The modulator is composed of the following parts: the loop filter, which is composed of two cascaded tank circuits, the comparator, and the DAC, which is composed of three branches:

– the main DAC, which is connected to the input node
– the internal DAC, which is connected to the internal node
– the excess loop delay compensation DAC, which is connected directly before the comparator

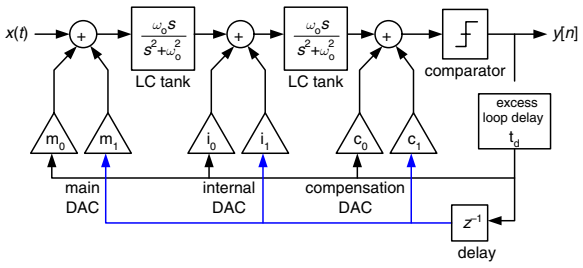

Fig. 1 *LC-based fourth-order CT ΣΔM*

At least two coefficients are needed for each DAC to obtain the needed degree of freedom to design the modulator [6]. The DAC coefficients are calculated such that the loop gain of the CT ΣΔM is equivalent to its DT counterpart to achieve optimum performance [2, 5].

The excess loop delay is defined as the delay of the DAC pulse due to the comparator and the DAC circuitry. The excess loop delay is one of the main sources of instability and SNR degradation in CT ΣΔMs. To restore the optimum performance of the modulator, the excess loop delay has to be accounted for during calculation of the DAC coefficients. This means that the optimum value of each DAC coefficient is dependent on the value of the excess loop delay.

By sweeping the value of the excess loop delay and calculating the optimum value of the DAC coefficients, we reached a very interesting result. As shown in Fig. 2, the second FIR coefficients for the three DACs (the main DAC, the internal DAC, and the compensation DAC) are approximately zero near 1.4Ts excess loop delay. This means that if the excess loop delay is adjusted to this value, the number of needed DAC coefficients can be reduced to a single coefficient per DAC.

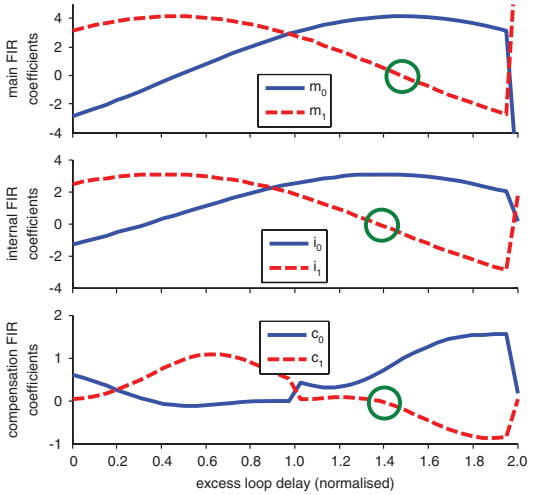

Fig. 2 *Feedback DAC coefficients against excess loop delay*

To validate this observation, the fourth-order BP CT ΣΔ modulator was redesigned with single coefficient DAC for different values of excess loop delay. The modulator was simulated and the maximum SNR for each excess loop delay was recorded as shown in Fig. 3. It can be deduced from the Figure that the single coefficient FIR is possible for a range of excess loop delay between $1.2T_s$ and $1.4T_s$ without significant loss in maximum SNR.

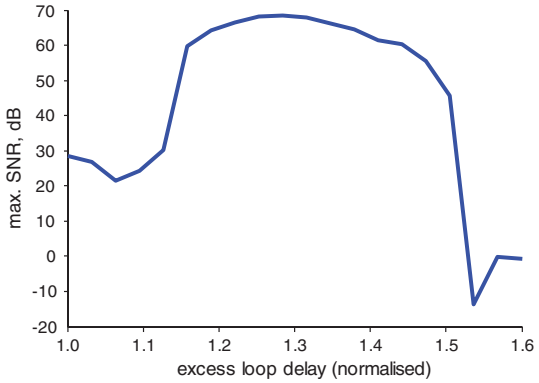

Fig. 3 *Maximum SNR achievable with single coefficient*

The value of the excess loop delay, which is mainly due to the comparator, can be tuned to be cascading more than one latch. Each latch increases the excess loop delay by a half clock cycle ($0.5T_s$). For fine tuning of the excess loop delay value, the latch circuit parameters, such as the current and the transistors sizes, can be modified to achieve the required value of the excess loop delay. However, using the circuit parameters to adjust the excess loop delay makes the design sensitive to process variations. To quantify this problem, the fourth-order BP CT ΣΔ modulator was designed for optimum value of the excess loop delay. The modulator was than simulated with different values of excess loop delay. The simulation results, shown in Fig. 4, indicate that the modulator is tolerant to excess loop delay variations of about ±10% without significant SNR loss.

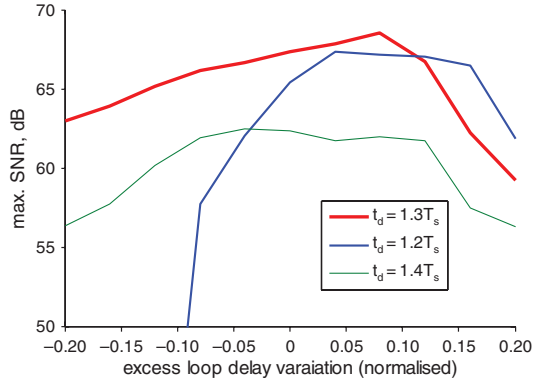

Fig. 4 *Effect of excess loop delay variation on modulator SNR*

Conclusion: A technique for simplifying the design of LC-based CT ΣΔMs is proposed. Adjusting the excess loop delay of the modulator at a certain value can reduce the number of needed feedback DAC coefficients by half. The concept has been validated by the design of a fourth-order CT ΣΔM with a single coefficient per DAC. The simulation results show that the proposed architecture is not sensitive to process variations and can work properly with up to ±10% variation of excess loop delay.

24 September 2009
doi: 10.1049/el.2009.2650

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