

# Fast and accurate jitter simulation technique for continuous-time $\Sigma\Delta$ modulators

A. Ashry and H. Aboushady

A fast and accurate technique for modelling and simulation of clock jitter in continuous-time sigma-delta ( $\Sigma\Delta$ ) modulators is introduced. In addition to its high speed compared to the traditional jitter simulation method, the proposed technique is still continuous-time based, which is more convenient than discrete-time based jitter modelling suggested in other publications. The mathematical principle of the proposed technique, as well as simulations results, are presented and compared to other simulation techniques.

**Introduction:** Continuous-time (CT)  $\Sigma\Delta$  analogue-to-digital converters (ADCs) are receiving increasing attention owing to their advantages compared to discrete-time (DT)  $\Sigma\Delta$  ADCs. Inherent anti-aliasing filtering, lower thermal noise, higher sampling rate and lower power consumption are all attractive advantages of the CT  $\Sigma\Delta$  ADCs that make them interesting solutions for high data-rate wireless communication systems [1].

The main disadvantage of the CT  $\Sigma\Delta$  is its sensitivity to the clock jitter of the feedback digital-to-analogue converter (DAC) which is not shaped with the loop filter owing to its direct connection to the input node. This clock jitter noise appears as a white noise in the signal band and can limit the modulator performance [1].

A major difficulty in modelling clock jitter noise is the very long simulation time, as the simulation time step has to be sufficiently smaller than the clock jitter which is usually much smaller than the sampling clock period. To overcome this problem, discrete-time based methods were suggested [2, 3]. Although these discrete-time based techniques are very fast, their discrete-time nature limits their ability to model other circuit non-idealities such as loop filter nonlinearity.

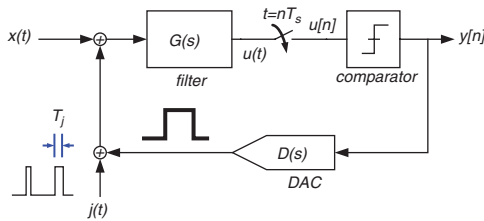


Fig. 1 Modelling jitter effect as an additive noise

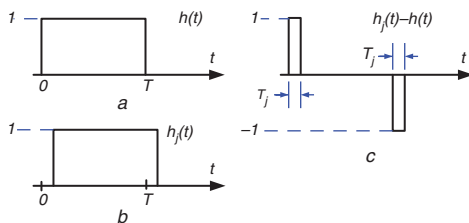


Fig. 2 Deducing jitter noise waveform

- a Ideal DAC pulse
- b Jittered DAC pulse
- c Jitter noise

**Proposed technique:** The clock jitter is defined as the time-deviation of the clock transitions with respect to the ideal clock. The jitter effect can be modelled as an additive noise, as shown in Fig. 1. The added jitter noise, is the instantaneous difference between the jittered DAC pulse and the ideal DAC pulse [2], Fig. 2:

$$j(t) = h_j(t) - h(t)$$

where  $h_j(t)$  is the jittered DAC pulse and  $h(t)$  is the ideal DAC pulse.

The proposed technique is based on the mathematical fact that the difference can be approximated as a differentiation as long as the time deviation due to clock jitter is much smaller than the clock period, which is usually the case. Thus, the jitter noise can be written in the

following form:

$$j(t) \approx T_j \frac{d}{dt} h(t)$$

where  $T_j$  is a Gaussian random variable of the same RMS value as the clock jitter. This indicates that the added jitter noise is extracted by differentiating the feedback DAC output and multiplying with a random number that has the same probability density function of the clock jitter as shown in Fig. 3

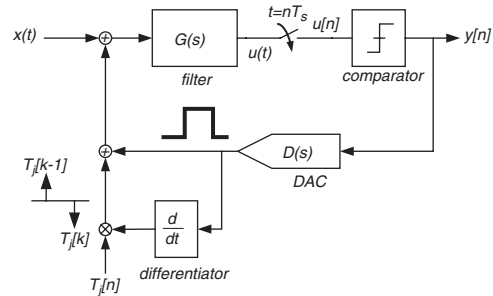


Fig. 3 Proposed jitter simulation model

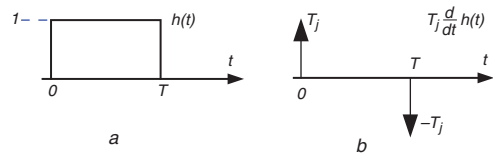


Fig. 4 Applying proposed technique to ideal DAC pulse

- a Ideal DAC waveform
- b Ideal differentiation

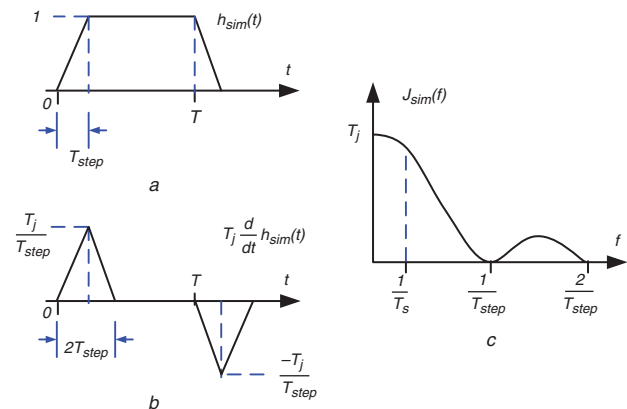


Fig. 5 Applying proposed technique in real simulation

- a Simulated DAC waveform
- b Simulated differentiation
- c Spectrum of jitter noise

**Model efficiency in real simulation:** For an ideal rectangular pulse, the proposed technique produces an impulse which is consistent with the traditional approximation [2], as shown in Fig. 4. However, for practical continuous-time simulations, the DAC waveform is trapezoidal rather than rectangular, Fig. 5a. For the trapezoidal pulse, the differentiation produces a triangular pulse instead of an impulse, Fig. 5b:

$$j(t) = T_j \frac{d}{dt} h_{sim}(t) = \frac{T_j}{T_{step}} \text{tri}\left(\frac{t}{T_{step}}\right)$$

where  $h_{sim}(t)$  is the simulated DAC waveform and  $\text{tri}(\cdot)$  represents the triangular pulse and  $T_{step}$  is the simulation time step. To ensure that the proposed technique produces acceptable performance in simulations, the spectrum of the jitter noise is found using Fourier transform:

$$J_{sim}(f) = T_j \text{sinc}^2(T_{step} f)$$

The output spectrum, which is shown in Fig. 5c, indicates that the jitter noise spectrum is almost flat in the Nyquist band. This result is valid as long as the simulation time step ( $T_{step}$ ) is sufficiently smaller than the

sampling time ( $T_s$ ), which is usually the case for any continuous-time based simulation.

**Simulation results:** To validate the proposed technique, the model proposed in Fig. 3 was used to simulate the jitter in a fourth-order bandpass continuous-time  $\Sigma\Delta$  modulator with a non-return-to-zero (NRZ) DAC. The clock jitter RMS value was swept from 0.01 to 10% of the sampling period. The same simulations were performed using the traditional continuous-time method used in [4] and also using the discrete-time method suggested in [2]. The simulation results illustrated in Fig. 6 show good agreement between the three methods. Table 1 summarises the main advantages and disadvantages of the three methods. The proposed technique provides fast simulation while preserving the continuous-time nature of the loop filter and feedback DAC.

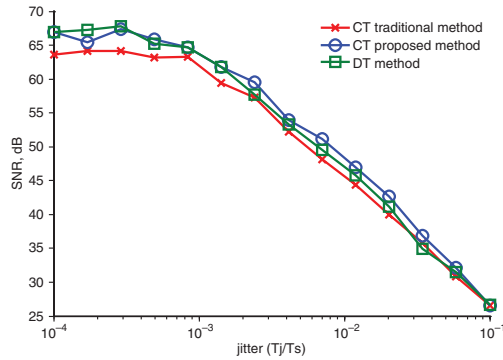


Fig. 6 Jitter simulation results

Table 1: Performance comparison

|   | Traditional method [4] | Discrete-time method [2] | Proposed method  |
|---|------------------------|--------------------------|------------------|
| Simulation nature                           | Continuous-time        | Discrete-time            | Continuous -time |
| Simulation time needed to produce (Fig. 6)  | Very slow (10 h)       | Very fast (10 s)         | Fast (10 min)    |
| Possibility to model circuit non-idealities | Easily modelled        | Very limited             | Easily modelled  |
| Spice compatibility                         | Compatible             | Not compatible           | Compatible       |

**Conclusion:** A technique for modelling the jitter in continuous-time  $\Sigma\Delta$  modulators that provides fast simulation while preserving the continuous-time nature of the loop filter and feedback DAC is introduced. The mathematical analysis shows that the proposed technique is reliable even with relaxed simulation time step requirements and the simulation results show good agreement between the proposed technique and traditional methods.

© The Institution of Engineering and Technology 2009

24 September 2009

doi: 10.1049/el.2009.2707

A. Ashry and H. Aboushady (*LIP6 Laboratory, University Pierre & Marie Curie, Paris VI, France*)

E-mail: ahmed.ashry@lip6.fr

## References

- 1 Oliaci, O., and Aboushady, H.: 'Jitter effects in continuous-time  $\Sigma\Delta$  modulators with delayed return-to-zero feedback'. Proc. IEEE ICECS, Lisbon, Portugal, 1998, Vol. 1, pp. 351–354
- 2 Benabes, P., and Kielbasa, R.: 'Fast clock-jitter simulation in continuous-time delta-sigma modulators'. IEEE Instrumentation Measurement Technology Conf., Budapest, Hungary, 2001, pp. 1587–1590
- 3 Chopp, P., and Hamoui, A.: 'Analysis of clock-jitter effects in continuous-time  $\Delta\Sigma$  modulators using discrete-time models', *IEEE Trans. Circuits Syst. I*, 2009, **56**, (6), pp. 1134–1145
- 4 Cherry, J., and Snelgrove, W.: 'Clock jitter and quantizer metastability in continuous-time delta-sigma modulators', *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, 1999, **46**, (6), pp. 661–676