A 5mW, 100kHz Bandwidth, Current-Mode Continuous-Time ΣΔ Modulator with 84dB Dynamic Range.

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Abstract

This current-mode continuous-time ΣΔ modulator achieves 84dB dynamic range. With a sampling frequency of 26MHz, the modulator consumes 5mW at 1.8V. The peak SNR is 79dB in 100kHz bandwidth. The Total Harmonic Distortion is −79dB for 25kHz input signal. The fully differential third order modulator is implemented in 0.18μm CMOS process with polysilicon n-well capacitors, and occupies 1.56mm².

1. Introduction

The continuously decreasing supply voltage of recent CMOS technologies is causing important limitations to the performances of Switched-Capacitors (SC) circuits. High switch resistance limits the signal range and limits the sampling frequency. Some circuit techniques, like bootstrapping switch and switched-opamp, have been developed to overcome this problem. These techniques are rather complex and still limit the sampling frequency. Continuous-Time (CT) circuits do not suffer from these limitations and are therefore capable of achieving higher performances in recent low-voltage CMOS processes [1]. Input-signal sampling errors, like settling-time errors and charge injection, are other Discrete-Time (DT) problems that do not exist in CT circuits.

On the other hand, CT ΣΔ modulators suffer from SNR degradation due to loop delay and from harmonic distortion due to DAC output waveform asymmetry. Both these errors can be highly attenuated by the use of a Return-to-Zero (RZ) feedback signal. CT ΣΔ modulators are also sensitive to clock jitter and extreme care must be taken to reduce jitter in the feedback signal.

Low-power CT filters have been implemented using current-mode circuit techniques [2]. It has also been shown in [3], that cascode current mirror based integrators can operate with low-power consumption at low-voltage supply.

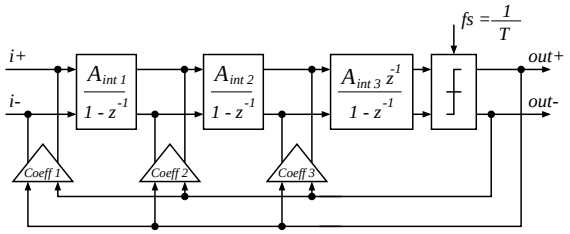

Figure 1. 3^{rd} order Discrete-Time ΣΔ modulator.

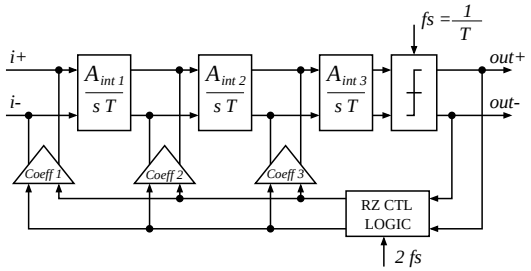

Figure 2. 3^{rd} order Continuous-Time ΣΔ modulator.

In this paper, we present a 13-bit third order current-mode CT ΣΔ modulator with RZ feedback. System level design issues are discussed in section 2. Low-power design techniques for low-voltage current-mode circuits are introduced in section 3. In section 4, measurement results of the fabricated chip are presented. Conclusion is given in section 5.

2. System Design

A third-order DT ΣΔ modulator and its equivalent CT modulator are shown in Figure 1 and Figure 2, respectively. The DT-to-CT transformation method based on the modified-z-transform technique, described in [4], is used to get the CT ΣΔ coefficients. This technique can be used to calculate the coefficients of a CT ΣΔ having an arbitrary RZ feedback signal. The DT coefficients [5], and their equivalent CT coefficients for a RZ feedback signal having

Table 1. DT ΣΔ modulator and its RZ feedback CT equivalent ($t_d = \frac{T}{4}$ and $\tau = \frac{3T}{4}$).

	A_{int_1}	A_{int_2}	A_{int_3}
DT ΣΔ	0.20	0.50	0.50
CT ΣΔ	0.03	0.50	2.00
	$Coeff_1$	$Coeff_2$	$Coeff_3$
DT ΣΔ	0.50	0.50	0.50
CT ΣΔ	0.50	0.10	0.11

a pulse delay, $t_d = \frac{T}{4}$, and a pulse width, $\tau = \frac{3T}{4}$, are listed in table 1. Note that, in this case, the maximum differential input signal should be limited to $\frac{3}{4}$ in order to maintain the system stable.

3. Circuit Design

3.1. Current-Mode Integrator

Figure 3 shows the fully differential current-mode integrator [2]. Neglecting output conductances and parasitic capacitances, and assuming identical transistors, small-signal analysis of this circuit yields the following transfer function:

$$H_{int}(s) = \frac{i_{inp}(s) - i_{inn}(s)}{i_{outp}(s) - i_{outn}(s)} = \frac{g_m}{s\ C} \qquad (1)$$

where g_m is the transconductance of the mirror transistors $M_1 - M_{111}$ and $M_2 - M_{222}$.

Operating at an oversampling ratio of 128, the quantization-noise-power of the modulator is sufficiently low and will be masked by the circuit noise. Based on the thermal noise calculations [3], the biasing current I_{01} of the first integrator is calculated such that the signal-to-thermal-noise ratio is 80dB for −6dB input signal.

The mirror transistors $M_1 - M_{111}$ and $M_2 - M_{222}$ have a fairly large length, L, in order to reduce the $1/f$ noise. This also applies to the biasing transistors, $M_7 - M_{777}$ and $M_8 - M_{888}$.
The differential input voltage-to-current conversion is performed using two 48kΩ resistors.

Cascode current-mirrors are used to increase the gain and the output resistance of the integrator. It has been shown in [3], that the maximum modulation index, $m = \frac{I_{in}}{I_0}$, can be obtained using the following relation:

$$\sqrt{1+m}\ (V_{EG_1} + V_{EG_3}) - \sqrt{1-m}\ V_{EG_1} - V_{TH_1} = 0 \qquad (2)$$

where V_{EG_1} and V_{EG_3} are the effective gate voltages of the mirror transistor M_1 and the cascode transistor M_3, respectively. By biasing the input nodes to $V_{DD}/2 = 0.9$V and by taking $V_{EG_3} = 0.15$V, we get a modulation index of 0.7 with $V_{CP} = 0.6$V and $V_{BC} = 1.4$V.

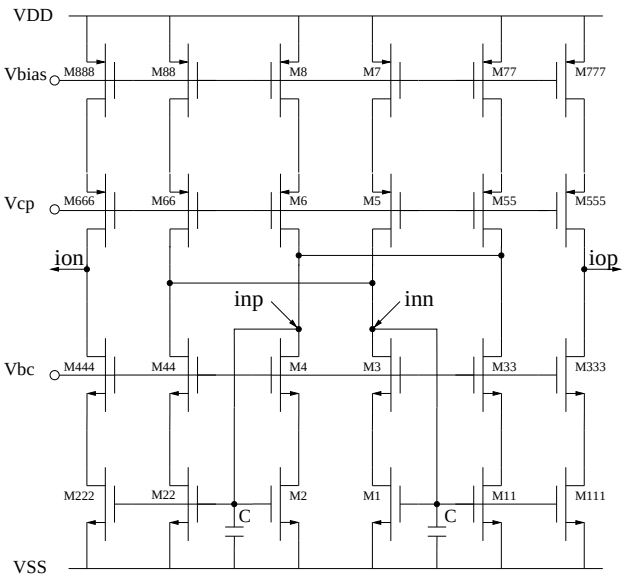

Figure 3. The current-mode integrator.

The main source of harmonic distortion in the current-mode integrator, shown in Figure 3, is g_m variation with the input current. It has been shown in [6], that it is possible to find an approximate expression for the transconductance $g_m(t)$ in function of the nominal transconductance g_{m_0}, the input current $i_{in}(t)$, the biasing current I_0 and the integrator gain A_{int}:

$$g_m(t) = g_{m_0}\sqrt{1 + \frac{A_{int}}{I_0}\frac{1}{T}\int_0^t i_{in}(t)\ dt} \qquad (3)$$

From equation (3), we can see that it is possible to reduce the transconductance nonlinearity either by increasing the biasing current I_0 or by decreasing the integrator gain A_{int}. In a low-power design, it is preferable to decrease the integrator gain A_{int}. The main disadvantage of decreasing A_{int} is the corresponding increase in the integrating capacitance C. In this design, $A_{int_1} = 1/30$ which leads, for a biasing current $I_{01} = 150\mu$A and a sampling frequency $f_s = 26$MHz, to an integrating capacitance $C_1 = 790$pF. This huge value is implemented using high-density polysilicon n-well capacitors.
Note that if A_{int_1} is modified the rest of the CT ΣΔ modulator coefficients have to be scaled in order to keep the Noise Transfer Function (NTF) unchanged. It should also be verified that the Signal Transfer Function (STF) has not been significantly modified within the band of interest.

Since linearity and noise of the ΣΔ modulator are determined by the performance of the first integrator, the biasing current of the first integrator is large. In voltage-mode ΣΔ modulators, we usually significantly reduce the biasing current of the subsequent

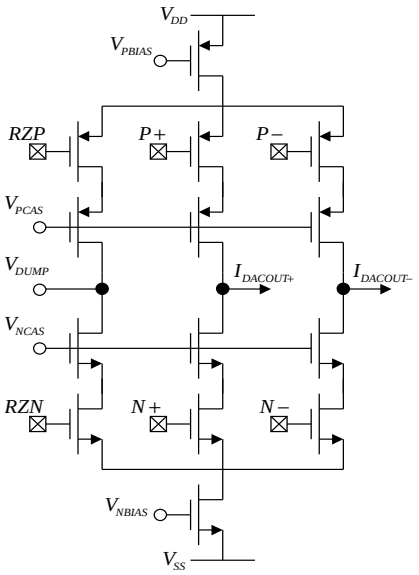

Figure 4. DAC circuit.

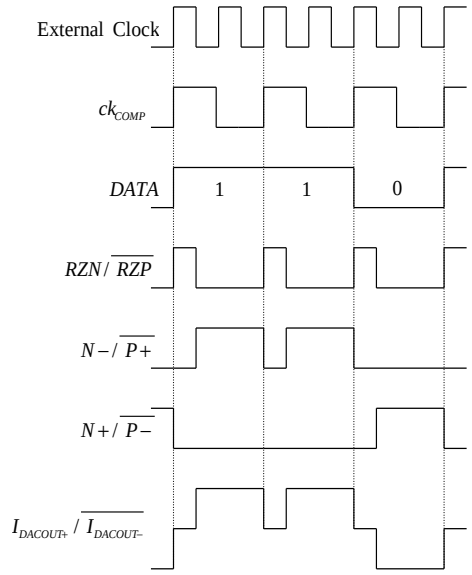

Figure 5. DAC control signals.

integrators [1]. Unfortunately, in current-mode circuits, the maximum signal swing at the output of each integrator is equal to mI_0. Significant reduction of the biasing currents of the second and third integrators is not possible. Nevertheless, the fact that A_{int_1} is very small has led to a small signal swing, which permitted a 40% reduction of the biasing current in the second integrator and a 64% reduction in the third integrator.

3.2. Return-to-Zero Feedback DAC

The RZ feedback DAC circuit and the corresponding control signals are shown in Figures 4 and 5, respectively. An external clock frequency equal to twice the sampling frequency is required in order to get a $T/4$ RZ phase at the beginning of each cycle. The output current is directed either to $I_{DACOUT+}$ or $I_{DACOUT-}$ depending on the comparator's output DATA. During the RZ phase, the positive and negative current sources are connected together through the DUMP node. In addition to reducing errors due to comparator delay and DAC output waveform asymmetry, connecting the current sources to the DUMP node at the beginning to each cycle has 2 other important features:

- The switching sequence is DATA independent. This reduces the switches charge injection DATA dependency and then no harmonic distortion is produced.
- The drain of the current source transistor is always charged to the same potential before the new DATA signal connects the current source to one of the outputs. This reduces the error current due to residual charges on this node from previous output connections.

The purpose of cascoding the switch transistor is to prevent voltage variations at the output from reaching the drain of the current source transistor and to increase the output resistance of the current source. To ensure that the current from the current source can flow to either one of the outputs, the signals controlling the NMOS switches (RZN, N+, and N-) have a high-crossing point. In the same way, the PMOS switches control signals (RZP, P+ and P-) have a low-crossing point. In order to reduce clock jitter on the control signals, the inverters driving the DAC switches are supplied from analog V_{DD}.

3.3. Comparator

The comparator circuit is depicted in Figure 6. This circuit is similar to the current-mode comparator presented in [7]. At its inputs, current mirrors, biased with the same current as the third integrator, copy the input signal to a clocked CMOS cross-coupled latch.

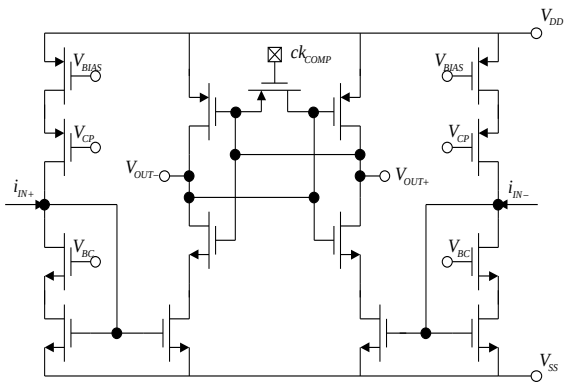

Figure 6. Current-mode comparator.

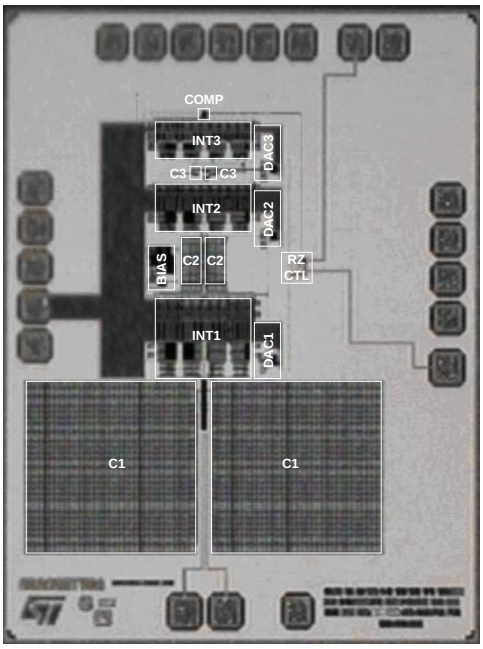

Figure 7. Chip Micrograph/Layout.

4. Measurements Results

The third order modulator was fabricated in 0.18μm CMOS process. A fixed transconductance biasing circuit was used to generate all the biasing currents and voltages of the modulator. This biasing circuit required only one external resistance of 5.75kΩ.

A die-photo of the chip is shown in Figure 7. Note that the two capacitors of the first integrator (790pF each) occupy 33% of the active area of the complete circuit. Figure 8 shows the measured SNR in function of I_{in}/I_{ref}, where I_{ref} is defined as the maximum input current of the first integrator ($I_{ref} = mI_{01}$). When clocked at 26MHz, the modulator achieves a dynamic range of 84dB and a peak SNR of 79dB. For a 25kHz input signal the THD is -79dB. The power consumption is 5mW at a supply voltage of 1.8V. Key performance parameters are summarized in Table 2.

5. Conclusion

In this paper, we presented the first implementation of a high performance current-mode CT $\Sigma\Delta$ modulator. When compared to other recently published CT and DT $\Sigma\Delta$ implementations having similar bandwidth specifications, the presented circuit achieves good performances. The circuit has a low-power consumption and operates at low-voltage supply. Large integrating capacitors are required in order to obtain high linearity.

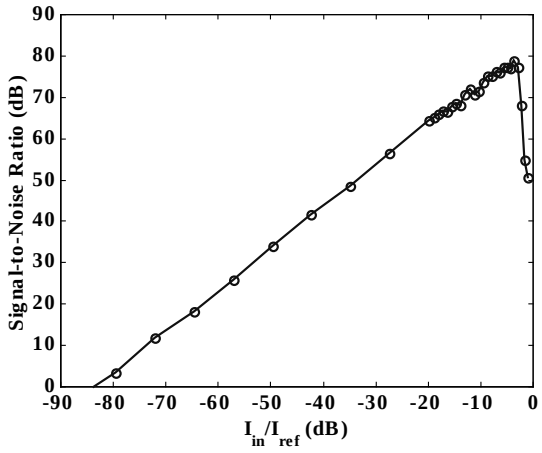

Figure 8. Measured SNR.

Table 2. Performance Summary.

Dynamic Range	84 dB
SNR	79 dB
THD	-79 dB
Signal Bandwidth	100 kHz
Sampling Frequency	26 MHz
Oversampling Ratio	128
Power Consumption	5 mW
Supply Voltage	1.8 V
Active Area	1.2 x 1.3 mm^2
Technology	0.18 μm, 1PS, 6 AL, CMOS

References

[1] E.J. van der Zwan and E.C. Dijkmans, "A 0.2mW CMOS $\Sigma\Delta$ Modulator for Speech Coding with 80 dB Dynamic Range", *IEEE Journal of Solid-State Circuits*, vol.31, no.12, pp.1873-1880, Dec. 1996.

[2] R. Zele and D. Allstot, "Low-Power CMOS Continuous-Time Filters", *IEEE Journal of Solid-State Circuits*, vol.31, no.2, pp.157-168, Feb. 1996.

[3] H. Aboushady and M.M. Louërat, "Low-Power Design of Low-Voltage Current-Mode Integrators for Continuous-Time $\Sigma\Delta$ Modulators", *IEEE International Symposium on Circuits And Systems*, May 2001.

[4] H. Aboushady and M.M. Louërat, "Systematic Approach for DT-to-CT $\Sigma\Delta$ Modulators", *IEEE International Symposium on Circuits And Systems*, May 2002.

[5] A. Marques, V. Peluso, M. Steyaert and W. Sansen, "Optimal Parameters for $\Delta\Sigma$ Modulator Topologies", *IEEE Transactions on Circuits and Systems II*, vol.45, no.9, pp. 1232-1241, Sept. 1998.

[6] H. Aboushady, "Design for Reuse of Current-Mode Continuous-Time $\Sigma\Delta$ A/D Converters", *Ph.D. Thesis, University of Paris VI*, Jan. 2002.

[7] L.G. Roeintan and A.M. Sodagar, "High-speed Current-Mode Sense Amplifier", Electronics Letters, vol.30, no.17, 18th Aug. 1994.