

Low-Power Cell-level ADC for a MEMS-based Parallel Scanning-probe Storage Device

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Abstract—We present a low-power, small-area solution for a cell-level ADC in a large array of MEMS-based sensors. First- and second-order switched-capacitor $\Sigma\Delta$ modulators were identified as suitable candidates for minimum power and area consumption of signals having moderate bandwidth (50 kHz) and resolution (7 bits). Three different solutions to minimize the area and power (optimization of architecture, modulator, and bias current) were analyzed, fabricated, and experimentally verified. Through this systematic analysis, the power consumption could be minimized and was measured to be only 14 μ W, a factor of 10 lower than in the initial design.

I. INTRODUCTION

Probe storage is one of the most promising candidates for a future mobile storage device with ultra-high densities well beyond 1Tb/in². The approach currently being developed in our lab [1, 2] uses a large array of heated micromachined cantilevers based on atomic force microscopy (AFM) probes to write/read/erase information in a thin polymer layer. The high precision required to navigate the probe tips over the storage medium is achieved by MEMS-based x/y actuators that position the large arrays of probe tips for parallel write/read/erase operations (see Fig. 1).

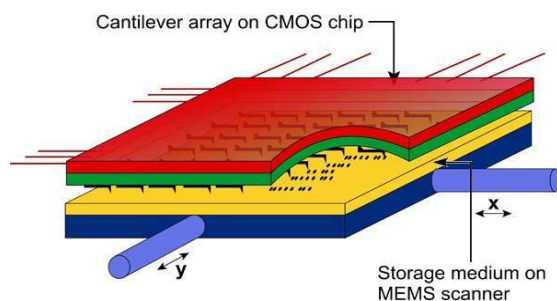


Figure 1. The probe-storage concept being developed in our lab

High data rates are achieved by parallel operation of large 2D arrays with hundreds of micro/nanomechanical cantilevers/tips operating in parallel. This leads to stringent power/area requirements for the read-out circuitry (< 0.5 mW, < 0.1 mm² per channel). This paper presents an investigation of the solutions and trade-offs for the analog-to-digital conversion (ADC) of the signals obtained from the analog front-end [3]. $\Sigma\Delta$ converters are an attractive choice for a cell-level (per-channel) ADC solution [4]. Three designs with variations of critical parameters for power/area optimization have been designed, fabricated, and characterized. Section II of the paper presents the area optimization of a first-order $\Sigma\Delta$ converter. Section III gives the details about the power optimization of the first-order $\Sigma\Delta$ converter and Section IV investigates the suitability of higher-order converters and presents a second-order design. Section V describes the decimation, and Section VI gives some conclusions.

The specifications for the converter are summarized in Table I. All designs were fabricated in a 0.25- μ m CMOS process with RF options (thick metal, MIM-capacitors).

TABLE I. ADC SPECIFICATIONS

| | |
|-------------------|--|
| accuracy | 7 bit |
| signal bandwidth | 50 kHz |
| input signal | ± 1.0 V differential |
| supply voltage | 2.5 V |
| power consumption | minimize ($\ll 0.5$ mW) |
| area | minimize ($\ll 0.1$ mm ²) |

II. AREA OPTIMIZATION OF FIRST-ORDER $\Sigma\Delta$ ADC

For modern processes the area occupied by a switched-capacitor $\Sigma\Delta$ modulator is increasingly being dominated by the sampling and integration capacitor area. This is all the

more true when we consider submicron technology migration with its continuously shrinking transistor and interconnection areas. The scaling of the integration capacitor also affects the power optimization (see Section III). Therefore, we first studied the scaling of the sampling/integration capacitor as the key element for area optimization.

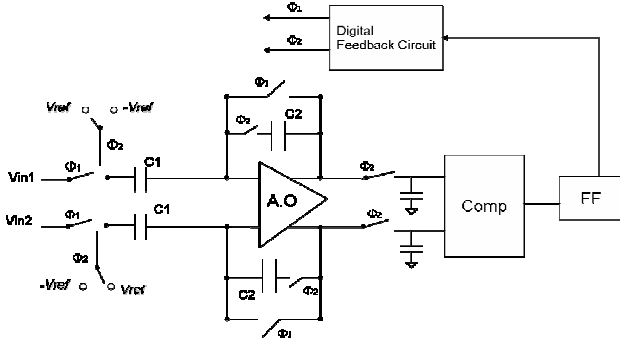


Figure 2. Schematic of first-order $\Sigma\Delta$ modulator.

The effect of capacitor scaling was studied using a fully differential first-order switched-capacitor $\Sigma\Delta$ modulator (see Fig. 2) with an oversampling ratio of 46 and a sampling frequency of 4.6 MHz to fulfill the ADC requirements (see Table I). The values were calculated and verified using a system-level model (Matlab [5]) that also includes the decimation filter (see Section V). The design shares the sampling capacitor between the input and the feedback DAC, therefore reducing the number of capacitors from 3 to 2. The chip includes an array of modulators with integration capacitors of 500, 400, 300, 200 and 100 fF (the sampling capacitors were scaled accordingly to achieve an integrator gain of $\frac{1}{2}$). An array of eight integrators (500-fF integration capacitor) was also included to study crosstalk effects, whereby special care was taken in the layout to shield the individual converters.

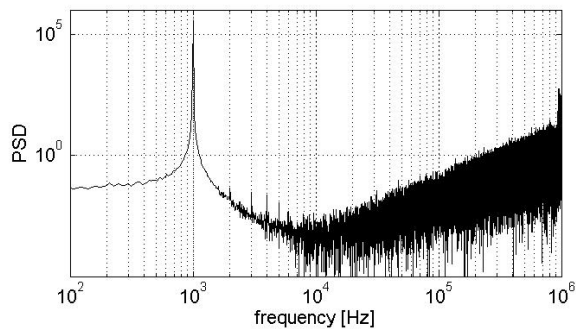


Figure 3. Measured PSD of first-order $\Sigma\Delta$ modulator (500 fF)

Fig. 3 shows the measured power spectral density PSD of the 500-fF $\Sigma\Delta$ converter for an input signal of 600 mVpp (1V full scale) with all converters in the array operating in

parallel. The crosstalk as well as the effects due to nonlinearities is below the noise level.

Table II summarizes the results for the scaling of the capacitors. The SNDR remains constant down to 200 fF and sharply decreases for 100 fF where the capacitors input are comparable to the parasitics of the input transistors (a few tens of femtoFarads). As expected, the thermal noise floor increases for smaller capacitors but this would only be reflected in the SNR for a signal bandwidth below 1 kHz. Finally, Fig. 4 shows that the nonlinearities (third harmonic) increase substantially for smaller capacitors.

TABLE II. PERFORMACE SUMMARY OF FIRST-ORDER $\Sigma\Delta$ MODULATOR

| C_1 | 500 fF | 400 fF | 300 fF | 200 fF | 100 fF |
|-------|--------|--------|--------|--------|--------|
| SNDR | 39.86 | 39.82 | 39.67 | 40.00 | 29.72 |

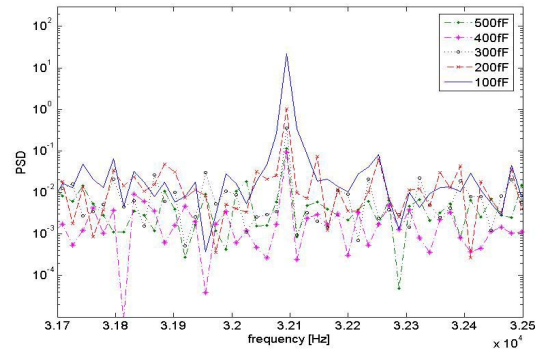


Figure 4. Measured PSD for scaled capacitors. The third harmonic increases with decreasing capacitance.

III. POWER OPTIMIZATION OF FIRST-ORDER ADC

The main limiting factor that determines the power-consumption of a first-order switched-capacitor ADC is given by the requirement that the output amplifier has to reach its final value during the integration phase. In other words, we need:

$$T_{\text{slewing}} + T_{\text{settling}} < T_{\text{integration}} \quad (1)$$

$T_{\text{integration}}$ is set to half of the frequency clock in switched capacitor techniques. We find that a high slew rate, governed by the availability of the biasing current to charge the capacitance at the dominant pole, is required:

$$SR = I / C_{\text{load}} \geq V_{\text{step}} \times \beta \times GBW, \quad (2)$$

where V_{step} is the input signal amplitude, β is the feedback factor of the closed-loop amplifier, and GBW is the amplifier's gain bandwidth product. At the same time, also a fast settling time for a given settling error \mathcal{E} and gain A_v is desired:

$$T_{\text{settling}} = \frac{A_v}{2\pi GBW} \ln\left(\frac{1}{\epsilon}\right) \quad (3)$$

There are two parameters that can be adjusted to decrease the power consumption of the switched-capacitor $\Sigma\Delta$ ADC. First, the amplifier topology can be optimized for maximum slew-rate at minimal power consumption, and second the bias current can be decreased.

A. Amplifier topology of first-order $\Sigma\Delta$ modulator

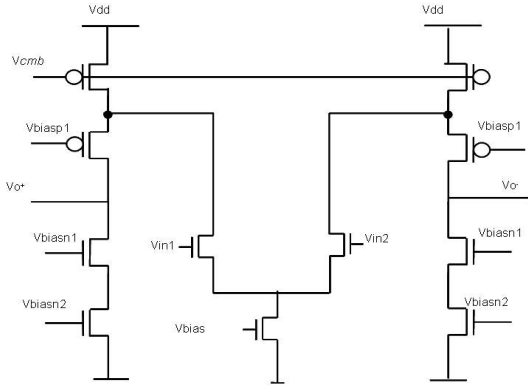


Figure 5. Schematic of the folded-cascode amplifier

Fig. 5 shows the schematic of the OpAmp that was used for the integrator in the first-order $\Sigma\Delta$ modulator presented in the previous section. A fully differential folded cascode was chosen to achieve high gain, low noise, small area, and good power supply rejection. The V_{cmo} voltage is regulated by a common-mode feedback circuit (CMFB). For low power considerations we design a switched capacitor CMFB. The amplifier biasing is done by an external input current to enable bias-current scaling. In this design, the bias current is only dominated by the slewing requirement, which demands a bias current of $27 \mu\text{A}$ (I_{SR}). A few 100 nA (I_{bias}) are sufficient to achieve the required gain bandwidth product of 4.2 MHz for this amplifier:

$$I_{\text{bias}} = \frac{(2 \times \pi \times C_L \times GBW)^2}{2 \times K_n \times (W/L)} = 200 \text{ nA} \ll I_{\text{SR}} \quad (4)$$

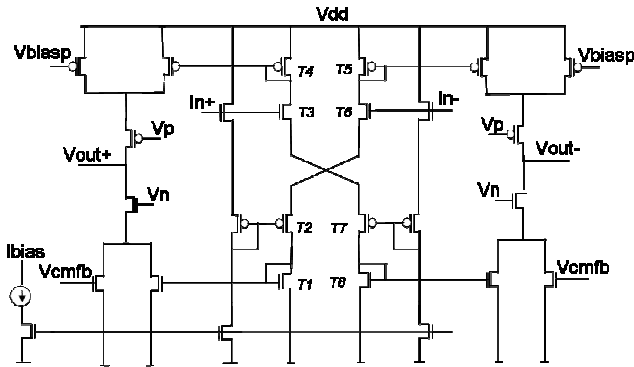


Figure 6. Schematic of class-AB amplifier

Therefore, a class AB amplifier can be used to reduce the power consumption. The design shown in Fig. 6 [6] with a class-AB input stage was found to offer the best ratio between peak and quiescent current. This design is difficult to implement for low supply-voltages because it requires a minimum V_{dd} of $2V_{\text{th}} + 4V_{\text{dsat}}$. We used the zero- V_{th} NFETs available in our technology for the input-stage ($T3$, $T6$) to achieve the necessary headroom. This leads to a nominal power consumption of $135 \mu\text{W}$ for the folded-cascode amplifier and $30 \mu\text{W}$ for the class AB amplifier. The total power-consumption including the comparator (not optimized) is $145 \mu\text{W}$ and $40 \mu\text{W}$.

B. Bias-current scaling

The bias currents used for the nominal designs assume a settling to less than 0.5 LSB in a half clock period. It has previously been shown that this rule can be neglected if a clock with low jitter is used. Fig. 7 shows the measured effect of bias-current scaling for the two first-order modulators. This leads to a minimum power consumption of $60 \mu\text{W}$ for the folded-cascode amplifier and $6 \mu\text{W}$ for the class-AB design.

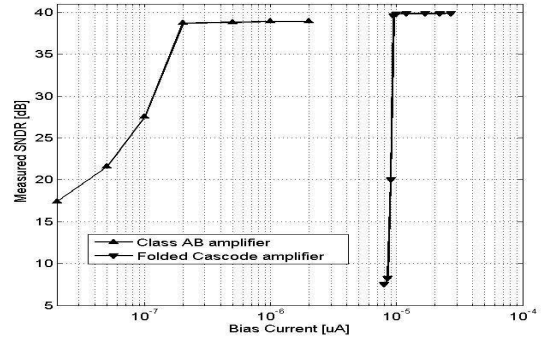


Figure 7. Effect of bias-current scaling.

IV. SECOND-ORDER $\Sigma\Delta$ CONVERTER

A further option to save power is to increase the order of the $\Sigma\Delta$ modulator. This decreases the required OSR and, therefore, the power consumption of the amplifiers and the comparator can be reduced. Table III shows the sampling frequencies and potential power savings, taking into account the increased number of amplifiers

TABLE III. COMPARISON OF POWER-CONSUMPTION FOR DIFFERENT ORDERS OF $\Sigma\Delta$ MODULATORS

| | first-order modulator | second-order modulator | third-order modulator |
|-------|-----------------------|------------------------|-----------------------|
| OSR | 46 | 23 | 12 |
| power | 100 % | 70 % | 50 % |

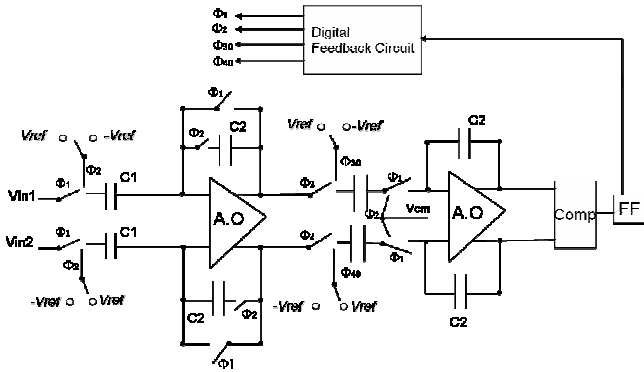


Figure 8. Schematic of second-order $\Sigma\Delta$ modulator

As only the second-order converter offers substantial power savings without a large increase in area, we integrated an array of four second-order modulators for the same specifications design (see Fig. 8). For our design we find an OSR of 23 based on Matlab system-level simulations compared with a value of 46 for the first-order design. The gain of both integrators is 0.5. For the first integrator we used a $C_1 = 500$ fF and $C_S = 250$ fF, and for the second one we used a $C_1 = 250$ fF and $C_S = 125$ fF to reduce the area.

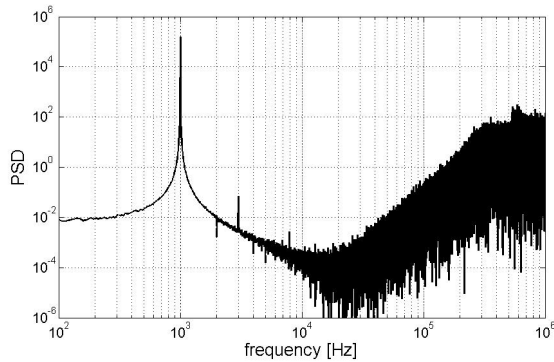


Figure 9. PSD of second-order $\Sigma\Delta$ modulator

Fig. 9 shows the measured PSD of the second-order $\Sigma\Delta$ converter. The SNDR for an input signal of 600mV (-5 dB full scale) was measured to be 37 dB. Despite the power savings offered by the second-order modulator, the penalty in area for the second integrator and the decimation filter make the first-order modulator a more favorable choice.

V. DECIMATION FILTER DESIGN

The standard combination of a comb-filter of order $k+1$ ($k \dots$ order of $\Sigma\Delta$ modulator) and a FIR filter consumes too much area and power for a cell-level implementation. Therefore, the $\Sigma\Delta$ modulators were designed such that a single comb-filter of order $k+1$ is sufficient. The comb-filter for the first-order modulator consumes an area of 0.015 mm^2 (automatic layout, no manual optimization). The use of a second-order modulator increases the area by 50%.

VI. CONCLUSIONS

In this paper, we present the analysis, design, and experimental verification of a cell-level ADC solution for a large array of micromachined sensors. The main focus of the design was to minimize the area and power consumption and switched-capacitor $\Sigma\Delta$ modulators were identified as the architecture of choice for the specifications given. The power and area can be minimized by scaling the capacitances and optimizing the architecture of the OpAmp in the integrator. All optimization approaches have been implemented in silicon and have been experimentally verified. Fig. 10 shows the chip-photograph of the chip including the two arrays of first-order converter with class AB amplifier and the second-order converter (the first-order modulator with cascode amplifier has been integrated on a different chip).

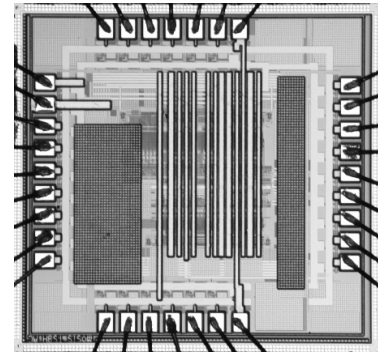


Figure 10. Chip photograph, size is 2.9 mm^2

The results obtained here can now be used together with an optimized comparator to fabricate a larger array and combine it with the complete analog front-end circuitry and the MEMS part of the storage device.

VII. REFERENCES

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