A 4^{th} order Subsampled RF $\Sigma\Delta$ ADC centered at 2.4GHz with A Sine-Shaped Feedback DAC.

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***Abstract*— A 4^{th} order subsampled RF LC $\Sigma\Delta$ ADC suitable for Software Defined Radio applications is presented. The ADC is clocked at 3.2GHz and centered at 2.4GHz. The simplicity of the ADC architecture combined with the subsampling technique result in a significant performance enhancement and power consumption reduction. A sine-shaped feedback DAC is used, not only for its reduced sensitivity to clock jitter but also for its more convenient frequency response to subsampled $\Sigma\Delta$ ADCs. An efficient algorithm for the tuning and calibration of the LC-based loop filter is presented. The ADC is implemented in a standard 130nm CMOS technology. It achieves a 51dB SFDR and a 40dB SNDR in a 25MHz BW and consumes only 19mW from a 1.2V supply.**

I. Introduction

The continuous improvement of both speed and density of digital circuits in CMOS technologies makes it attractive to push most of the chip functionality from the RF and analog domain to the digital domain. In an RF receiver, this means to push the Analog-to-Digital Converter (ADC) near the antenna to achieve what is commonly known as Software Defined Radio (SDR). In SDR receivers, as shown in Fig. 1, most of the analog blocks such as the down-conversion mixer and the channel selection filter are moved to the digital domain. In this case, most of the signal processing is done in the flexible and programmable digital domain.

One of the main challenges in implementing an SDR receiver is the stringent ADC requirements. The ADC must have a large bandwidth and a high dynamic range to be able to deal with the targeted RF band in the presence of strong out-of-band blockers. A promising technique to achieve these ADC specifications is to use a bandpass LC $\Sigma\Delta$ ADC with an RF center frequency.

In this paper, we present an efficient realization of an RF bandpass $\Sigma\Delta$ ADC centered at 2.4GHz. The ADC is implemented in a standard low-cost CMOS technology and it has a power consumption significantly lower than recent SiGe realizations [1]. Compared with other CMOS implementations [2], [3], the proposed RF bandpass $\Sigma\Delta$ ADC has a simple 4^{th} order architecture with a single-bit quantizer and a minimum number of feedback coefficients [4].

Subsampling is used to reduce the sampling frequency [2], [3]. Despite the use of the subsampling technique, the sampling frequency f_s is kept equal to 4 times the output frequency f_o, Fig. 1. This greatly simplifies the digital single-bit down-conversion mixer and the subsequent decimation filter [2].

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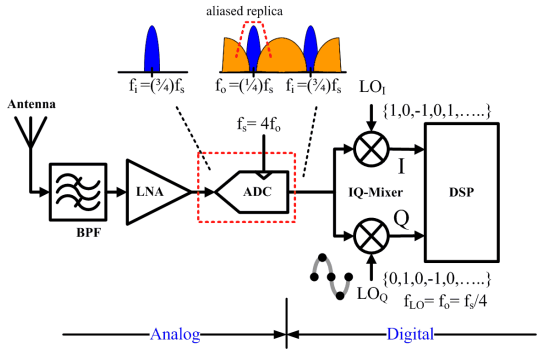


Fig. 1. A Software Defined Radio receiver based on a subsampled RF $\Sigma\Delta$ ADC. Input center frequency $f_i = (3/4)\, f_s$ and output center frequency $f_o = (1/4)\, f_s$.

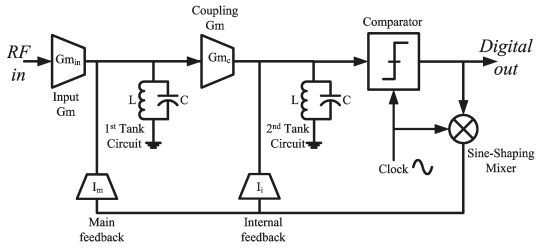
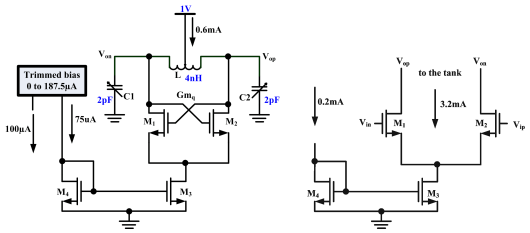


Fig. 2. A simple architecture for a subsampled $4th$ order LC-based $\Sigma\Delta$ ADC. The loop delay is optimized for a minimum number of feedback DAC coefficients.

Sine-shaped feedback DAC is used in this ADC, due its immunity to clock jitter and its convenience for subsampling [2]. We present a robust sine-shaping technique that does not require an additional source. In fact the sine-shaped DAC is driven by the same clock source applied to the comparator.

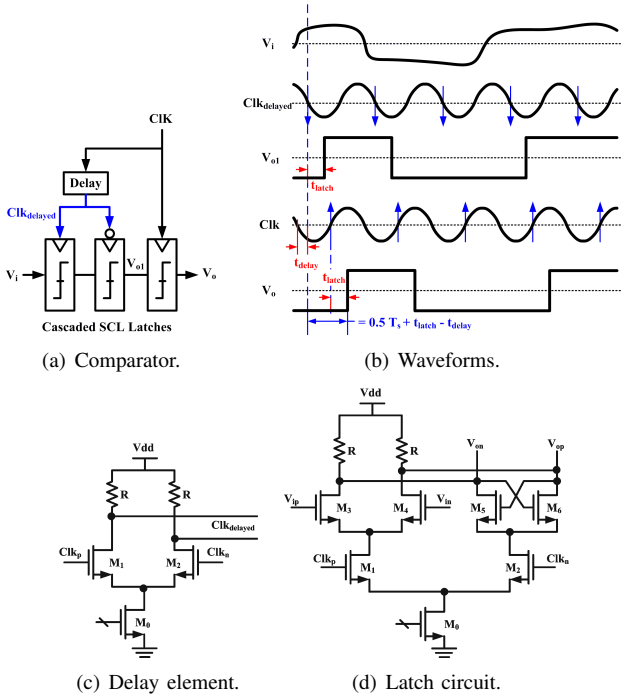
We also present the calibration algorithm used to tune the center frequency and the quality factor of the loop filter.

The paper is organized as follows: section II introduces the ADC architecture, section III discusses the circuit implementation of the main ADC blocks, section IV gives details about the proposed tuning and calibration algorithm, and finally, section V presents the measurement results.



(a) Tank circuit. (b) Input transconductor.

Fig. 3. Loop filter circuit implementation.



(a) Comparator. (b) Waveforms.

(c) Delay element. (d) Latch circuit.

Fig. 4. Comparator architecture, waveforms and circuit implementation.

II. Architecture

In RF $\Sigma\Delta$ ADCs, it is usually preferred to make the sampling frequency f_s 4 times the input center frequency f_i, to simplify the design of the digital down-sampling mixer, as the Local Oscillator (LO) sinusoidal signal becomes a series of $\{1, 0, -1, 0\}$ [2]. However, when the input center frequency is very high, this requirement becomes very difficult, especially in standard CMOS technologies. An efficient solution to overcome this problem is to decrease the sampling frequency below the Nyquist limit such that the output from ADC is the aliased replica of the input signal instead of the signal itself [2], [5].

If a subsampling factor of 3 is used, the sampling frequency becomes: $f_s = (4/3)\, f_i$ = 3.2GHz, and the output becomes the aliased replica of the input, i.e. $f_o = f_s - f_i = (1/4)\, f_s$ = 800MHz. Thus, the subsampling in this case achieves several goals:

1) Reducing the sampling frequency f_s from $4f_i$=9.6GHz to $(4/3)\, f_i$=3.2GHz.
2) Inherent down-conversion, as the input signal is down-converted from f_i=2.4GHz to f_o=800MHz.
3) Keeping the ratio between the sampling frequency f_s and the output frequency f_o at 4, i.e $f_s = 4f_o$.

The ADC architecture is shown in Fig. 2. The main advantage of this architecture is the few number of feedback DAC branches. The number of FIR DAC coefficients is reduced to one coefficient per LC resonator using the optimization method described in [4]. Notice also the absence of the loop delay compensation coefficient which is usually fed-back at the input of the comparator. In high-speed CT $\Sigma\Delta$ modulators, the loop delay compensation coefficient renders the circuit design of the comparator more complex due to the additional summing node it introduces. The proposed architecture leads to a simple comparator design and to relaxed thermal noise requirements for the LC loop filter and the feedback DACs.

Sine-shaped feedback DAC is used in this ADC, because it has the best immunity to clock jitter [6]. Sine-shaped feedback DACs are also more convenient to subsampling than conventional Rectangular-Shaped NRZ feedback DACs. This is due to the fact that a Sine-Shaped DAC gives a higher amplification to the image of the ADC output around the input frequency, f_i, than the rectangular-shaped NRZ DAC [2].

III. Circuit Design

A. Loop Filter

The loop filter is mainly composed of two cascaded LC tank circuits. Each tank circuit consists of a center-tapped inductor and two identical banks of capacitors, as depicted in Fig. 3(a). The inductor has 3-turns with around $4nH$ inductance and quality factor of about 14. The capacitor bank has a nominal value of $2pF$ and can be trimmed in $15fF$ steps to allow for center frequency tuning and calibration.

The cross-coupled transconductor Gm_q acts as a negative resistance and compensates the losses in the tank circuit [1]. The value of the negative resistance can be adjusted by controlling its current which has a nominal value of $600\mu A$ and can be trimmed in $40\mu A$ steps. If the current of the negative resistance is increased above a certain limit, oscillation will occur, which can be used in center frequency tuning and calibration, as will be described in section IV.

The input transconductor Gm_{in} circuit is shown in Fig. 3(b). The coupling transconductor Gm_c has the same circuit but with a lower current (0.6mA), due to its relaxed specifications compared to Gm_{in}.

B. Comparator

The proposed architecture achieves the optimum performance when the loop delay is 0.7 times the sampling time, i.e $t_d = 0.7T_s$ [4]. A comparator composed of 3 cascaded latches has, ideally, $0.5T_s$ delay. After circuit implementation of the complete feedback loop (Comparator+Mixer+Feedback Gm), it was found that the loop delay exceeds $0.8T_s$, which is far from the optimum value.

To reduce the loop delay, we used a delay compensation technique similar to what was published in [7]. The technique is to eliminate the comparator delay by clocking the last latch with an early clock as shown in Fig. 4(a). This reduces the comparator delay by the value of the clock delay:

$$t_{comp} = 0.5\,T_s + t_{latch} - t_{delay} \quad (1)$$

The Source-Coupled Logic (SCL) latch is used, because it can work at significantly higher speed than the CMOS latch. The design of the SCL latch, shown in Fig. 4(d), is a trade-off between power consumption, voltage swing and high operation speed. The same SCL topology is used for the delay element as shown in Fig. 4(c). Using the same topology for both the latch and the delay element makes t_{latch} and t_{delay} have similar variation with process and temperature and makes the comparator delay almost constant as suggested by (1).

C. Sine-Shaping Mixer

The traditional implementation of the sine-shaped DAC is to add a sine-shaped tail current to the DAC circuit [2]. The main disadvantages of this implementation is the additional sine source needed and the synchronization between the clock and the sine source.

The proposed implementation is based on doing the sine-shaping directly after the comparator by adding a mixer [8]. The mixer is driven with the same clock source applied to the comparator as shown in Fig. 5(a). A delay element is added to adjust the sine phase to get a smooth sine-shaped output as shown in Fig. 5(b). The mixer circuit shown in Fig. 5(c) has a similar topology as the latch and the delay element for better stability with process and temperature variations [8].

In order to inject the sine-shaped feedback signal into the loop filter, two feedback transconductors are used to generate the feedback currents I_m and I_i. As shown shown in Fig. 5(d), the cascode structure is used to increase the output resistance of the feedback transconductors to avoid degrading the tank circuit quality factor.

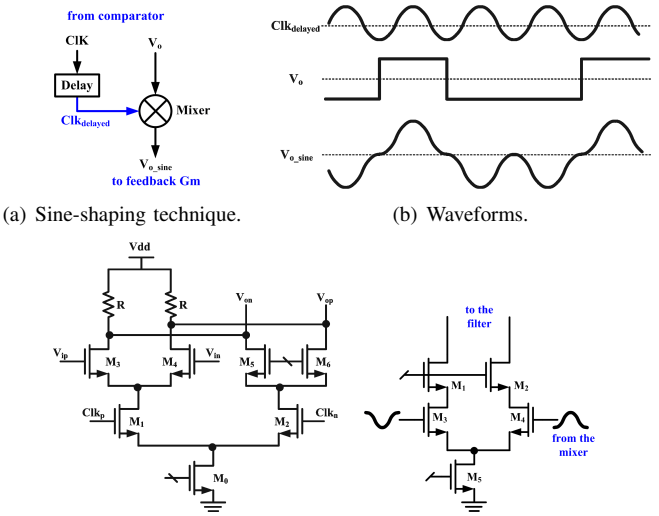
IV. Tuning and Calibration

One of the main issues in CT $\Sigma\Delta$ ADCs is the poor accuracy and the sensitivity to process variations. Trimming is needed to compensate the drift in circuit components to obtain the optimum performance from the ADC. The most important parameters that must be calibrated are the resonance frequency f_o and the quality factor Q of the two LC tank circuits.

An efficient calibration algorithm was suggested in [3] that is based on putting the tank circuit in oscillation mode, then detecting its oscillation frequency.

The calibration procedure, illustrated in Fig. 6, is performed by the following steps:

1) The SCL latches are configured as buffers by deactivating their driving clock.
2) Tank$_1$ is put in oscillation mode by setting its Q-enhancement transconductor Gm_{q1} to its maximum.
3) Capacitor of tank$_1$ C_1 is tuned, till the output frequency is equal to the desired center frequency.



(a) Sine-shaping technique. (b) Waveforms.

(c) Proposed mixer circuit. (d) Feedback transconductor.

Fig. 5. Circuit implementation of the proposed Sine-shaping technique.

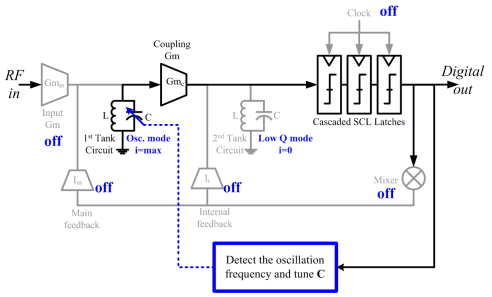


Fig. 6. ADC in calibration mode.

4) Q-enhancement transconductor Gm_{q1} is reduced gradually till oscillation vanishes.
5) Tank$_2$ is calibrated using the same procedure as tank$_1$.

The measurements showed that the digitally-controlled tank circuit covers an 800MHz frequency tuning range with an 8MHz resolution.

V. Measurement Results

The chip was fabricated in a 130nm CMOS technology. The chip micrograph is shown in Fig. 7. The active area is about $0.84mm^2$. Most of the active area is occupied by the two inductors, the two capacitor banks and the empty space that separates the two inductors.

An IQ vector signal generator was used to generate the input signal centered at 2.4GHz. The ADC was clocked with a 3.2GHz clock, and the output bit stream was captured using a 40Gs/s digital oscilloscope. FFT is then applied to the captured bit-stream to obtain the spectrum shown in Fig. 8. It can be seen from the figure that the Spurious Free Dynamic Range (SFDR) is about 51dB. The Signal to Noise and Distortion Ratio (SNDR) is then measured for different values of the input signal power, as shown in Fig. 9. The ADC achieves 40dB of SNDR in a 25MHz bandwidth (OSR=64).

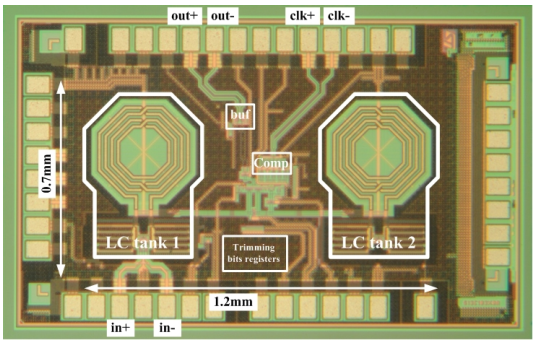


Fig. 7. Chip micrograph.

Table I compares the achieved performance to some recently published RF $\Sigma\Delta$ ADCs. ADCs are usually compared according to their FoM ($P_{dc}/\left(2\,BW\,2^{ENOB}\right)$). Another FoM proposed in [9] is more adapted to bandpass $\Sigma\Delta$ ADCs (FoM$_{BP}$ = FoM$/\left(1+6f_o/f_s\right)$).

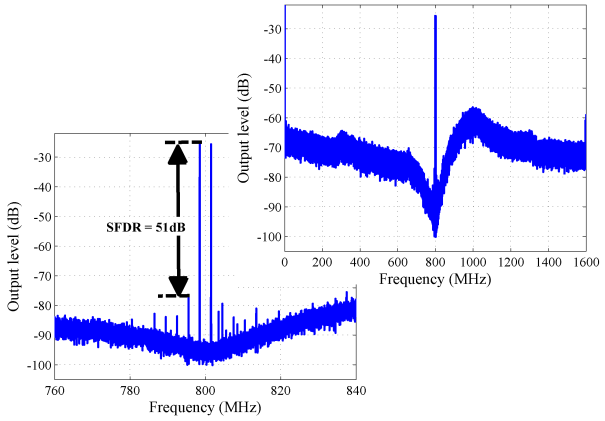


Fig. 8. Output spectrum obtained from a 2^{17} points FFT and averaged 4 times on the output digital bit stream for a two-tones input signal at 2.4GHz $\pm$ 1.5MHz.

VI. Conclusion

A 4^{th} order subsampling RF $\Sigma\Delta$ ADC clocked at 3.2GHz and centered at 2.4GHz was presented. The $\Sigma\Delta$ ADC architecture is composed of 2 LC tank circuits with Q-enhancement, 2 transconductors, 1 single-bit comparator and a sine-shaped feedback DAC. In order to tune and calibrate the $\Sigma\Delta$ loop filter, a simple algorithm, suitable for integration, was presented. The ADC is implemented in a standard 130nm CMOS technology and achieved a 51dB SFDR and a 40dB SNDR in a 25MHz BW with only 19mW power consumption.

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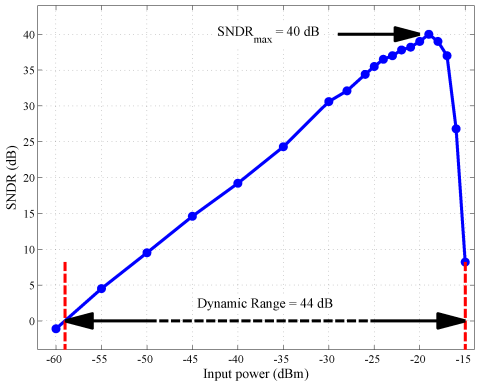

Fig. 9. Measured SNDR versus the input power.

TABLE I
Comparison with recent RF $\Sigma\Delta$ ADCs

Reference	this work	[3]	[2]	[5]	[1]
Order	4^{th}	4^{th}	2^{nd}	6^{th}	4^{th}
Center frequency	2.4GHz	2.4GHz	2.4GHz	2.4GHz	950MHz
Sampling frequency	3.2GHz	6.1GHz	3.2GHz	3GHz	3.8GHz
SNDR	40dB	40dB	34dB	40dB	59dB
Bandwidth	25MHz	80MHz	25MHz	60MHz	1MHz
Power consumption	19mW	53mW	26mW	40mW	75mW
Technology	CMOS 130nm	CMOS 40nm	CMOS 130nm	CMOS 90nm	SiGe 250nm
FoM (pJ/bit)	4.7	3.6	12.7	4.1	51.5
FoM$_{BP}$ (pJ/bit)	0.8	1.1	2.3	0.7	20.6
$f_s = 4\,f_o$?	Yes	No	Yes	No	Yes

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