A Q-Enhanced LC Bandpass Filter using CAIRO+

Diomadson Belfort[1], Nicolas Beilleau[1], Hassan Aboushady[1], Marie-Minerve Louërat[1] and Sebastian Catunda[2]
[1]University Pierre & Marie Curie, LIP6 Laboratory, Paris, France
[2]Federal University of Maranhão - UFMA, Department of Electrical Engineering, São Luís, MA, Brazil

***Abstract*—In this paper, we present a systematic design procedure for Q-enhanced integrated LC filters, which does not require any simulations and is thus suitable for design automation. The design procedure has been described in the CAIRO+ analog design environment, containing the BSIM3v3 models of the MOS transistors. Precise estimations of the quality factor and the resonance frequency were made possible by adding the integrated inductance π-model into the design environment. Several design examples of 2.4 GHz Q-enhanced LC filters are given in a 0.13 μm CMOS process.**

I. Introduction

Advances in highly integrated wireless communication transceivers provide applications for integrated RF bandpass filters. Active filters can achieve a high quality factor but with a poor dynamic range when operating at gigahertz frequencies. Passive LC filters can achieve high dynamic range at very low power consumption but on-chip inductors have very low quality factor Q. Q-enhanced LC filters are a good compromise between these two types of filters [1]. Q-enhanced LC filters are not only used to realize integrated RF bandpass filters [2] but they are also used in the design of RF bandpass $\Sigma\Delta$ modulators [3], [4]. Fig.1 presents a popular implementation of a Q-enhanced LC filter using a differential negative resistor. The design of such a circuit usually requires a significant amount of simulation iterations with a SPICE-like circuit simulator.

In this work, we propose a systematic design procedure for a Q-enhanced LC filter that provides the desired quality factor and resonance frequency and does not require any iterations with a circuit simulator. In this procedure, the quality factor and the resonance frequency of the LC filter are calculated using the π-model for the inductor and the BSIM3v3 models for the transistors. The design procedure is described in the analog design environment CAIRO+ [5].

In section II-A, we present the procedure used to size the transistors of the negative resistance based on the estimation of the quality factor of the original lossy LC tank. In section II-B, it is shown how the resonance frequency is adjusted based on a empirical model [6] and accurate estimation of the transistors parasitic capacitance. The complete design automation procedure is presented in section III. Comparisons between predicted performances and simulation results for several design examples are given in section IV.

II. Design Method Including Parasitics

A. Quality Factor Enhancement

Due to its nature, an integrated inductor presents some parasitics resistances and capacitances. Resistances are due to intrinsic resistance of the employed metal, interconnections, skin effect at high frequencies and lossy substrate.

The inductor with these parasitics can be modeled in function of the inductor layout and material parameters using the π-model shown in Fig.2, where R_S represent the total loss in the inductor, C_{Sub} is the capacitance between the trace and the substrate and R_{Sub} is the substrate loss [7]. To enhance the quality factor, we have to insert an active negative resistance in series [8] with the lossy inductor or a series-to-parallel impedance transformation can be performed on the lossy inductor and a negative resistance can be added in parallel mode [9] as shown in Fig.3.

In this work the parallel solution was used.

As shown in Fig.4, we transform this π-model to a parallel model.

In this case we take:

$$\begin{gathered} R_{pl} = R_S(1+Q_{rl}^2) \qquad R_{pc} = R_{Sub}(1+Q_{rc}^2) \\ C_p = C_{Sub}\frac{Q_{rc}^2}{1+Q_{rc}^2} \qquad L_p = L_S\frac{1+Q_{rl}^2}{Q_{rl}^2} \\ R_p = R_{pl}//R_{pc} \\ Q_{rc} = \frac{1}{\omega_0 R_{Sub} C_{Sub}} \qquad Q_{rl} = \frac{\omega_0 L_S}{R_S} \end{gathered} \tag{1}$$

where

- Q_{rc} is the quality factor of the series-RC circuit;
- Q_{rl} is the quality factor of the series-RL circuit;
- R_{pl} is the resistance in parallel-RL circuit equivalent to the series-RL circuit;
- R_{pc} is the resistance in parallel-RC circuit equivalent to the series-RC circuit;
- C_p is the capacitance in the parallel-RC circuit equivalent to the series-RC circuit;
- L_p is the inductance in the parallel-LC circuit equivalent to the series-LC circuit.

Then we can replace the π-model by a RLC bridge with R_p resistor, C_p capacitor and L_p inductor. From the parallel resistor and parallel capacitor, the quality factor of the resonator can be derived as:

$$Q_0 = R_p\sqrt{\frac{C_{P_C}+C_p}{L_p}} \tag{2}$$

where C_{P_C} is the capacitance needed to adjust to resonance frequency. The effective quality factor can be found from [9] as

$$Q_{enh} = \frac{Q_0}{1 - G_{m_0}R_p} \tag{3}$$

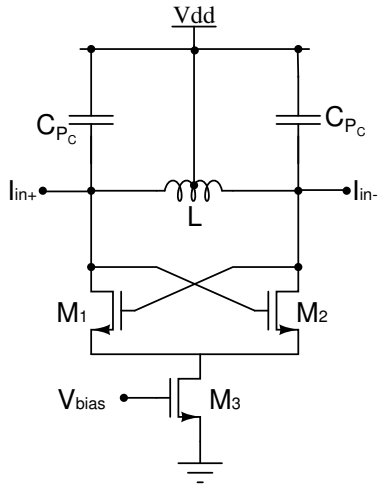

Fig. 1. Q-enhanced LC filter with differential negative resistance.

where G_{m_0} is the equivalent transconductance of the differential negative resistance. So, choosing an appropriate value for G_{m_0} one can improve the value of the quality factor of the original lossy LC tank from Q_0 to a desired quality factor Q_{enh}. G_{m_0} is calculated using the approximations:

$$G_{m_0} = G_m - G_{ds} \tag{4}$$

where G_m and G_{ds} are respectively the transconductance and the output conductance of transistor M_1 Fig.1. In the CAIRO+ analog design environment, it is possible to perform an accurate sizing of a transistor in order to obtain a certain transconductance G_m. Once the dimensions of the transistor are known, it is also possible to extract accurate value of G_{ds}. A few iterations are then required to size transistors M_1 and M_2 according to the required overall G_{m_0} of the differential negative resistance.

B. Resonance frequency

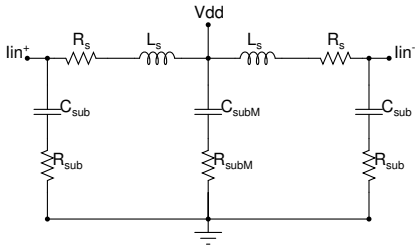

Fig. 2. Simplified π-model for a differential center-tapped spiral inductor.

In order to calculate C_{P_C} the required capacitor value for a desired resonance frequency ω_0, the following relation is used:

$$C_{par} = C_p + C_{dg} + C_{gd} + C_{gs} + C_{ds} \tag{5}$$

$$C_{P_C} = \frac{1}{\omega_0^2 L_p} - C_{par} \tag{6}$$

where C_{par} is the total parasitic capacitance, due to the inductor and the transistors. The MOS parasitic capacitance

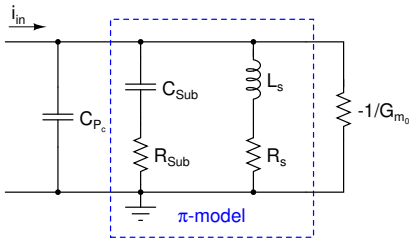

Fig. 3. LC filter with Q-enhancement

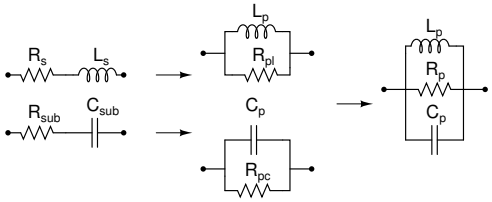

Fig. 4. π-model to parallel model transformation in small signal.

are easily obtained from the transistors BSIM3v3 model. C_{sub} is extracted from the inductor π-model. Both models are integrated, available in the CAIRO+ design environment.

III. Design Automation and Performance Evaluation

A. CAIRO+ Design Environment

CAIRO+, is a framework, developed at the LIP6 laboratory, which aims to help analog circuit designers to describe their design procedure [5]. It provides a library of functions to describe the netlist template, layout template, specification template, design space exploration procedure and layout generation. The general method in CAIRO+ is to design modules using devices. Each module has a list of defined parameters, and one or more procedures. In the case of designing a bandpass Q-enhanced LC filter, the input parameters are: the desired quality factor, the resonance frequency, the input bias voltage, and the value of the inductor with its geometrical parameters. The procedure will calculate and return the sizes of the transistors, and the value of the capacitor, C_{P_C}, of the resonator.

B. Thermal Noise

The method we have implemented to compute the noise generated by the filter is described as follows. The noise in the circuit are presented in Fig. 6. The thermal noise generated by transistors ($\overline{In_M^2}$) is computed using CAIRO+ transistor device, which includes a procedure to compute thermal noise. The thermal noise of the resonator is computed using the total parallel resistor as approximated in section II-A so:

$$\overline{I_{n_R}^2} = \frac{4kT}{R_p} \tag{7}$$

Considering we have two current noise sources and that they are uncorrelated we add the two spectral noise density to obtain the total current noise spectral density at the input. The

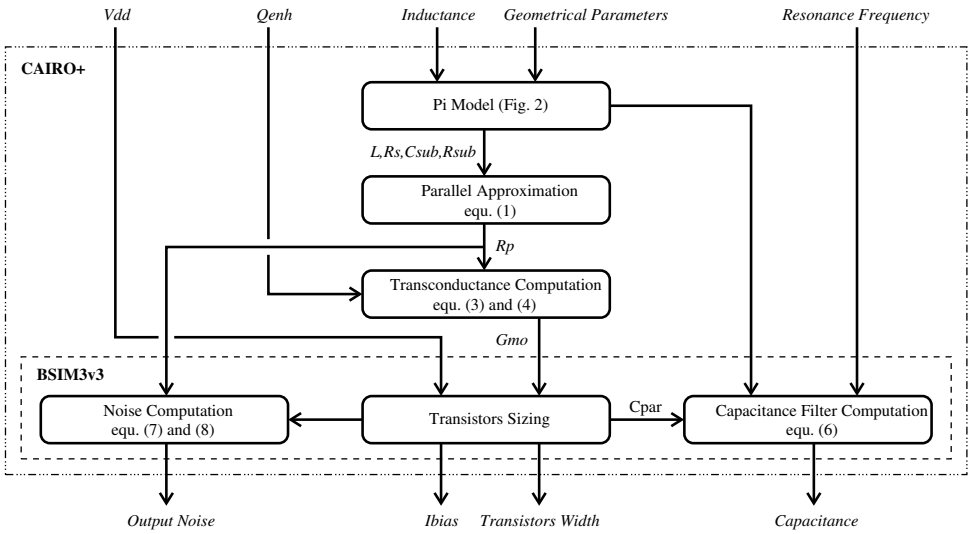

Fig. 5. Q-enhanced LC filter design procedure based on Cairo+ design environment including BSIM3v3 models.

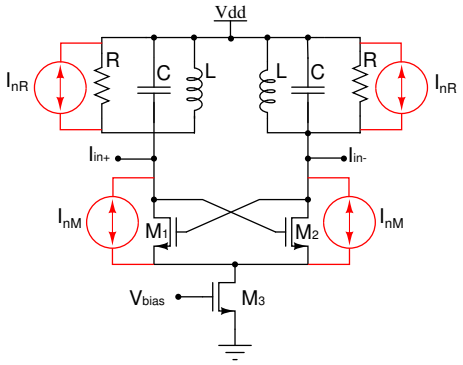

Fig. 6. Thermal Noise Circuit

equivalent voltage noise can be computed at the output by multiplying it by the total gain (the total impedance at the given frequency of the filter) and integrated over the useful bandwidth (BW) to have the output noise power :

$$P_n = 2\int_{BW} |Z(j\omega)|^2(\overline{I_{n_R}^2} + \overline{I_{n_M}^2})df. \qquad (8)$$

As shown in section IV, the approximation by a parallel resistor is sufficiently accurate for the quality factor and resonance frequency computations.

A flowchart of the proposed design procedure, described in section II-A and II-B, using the CAIRO+ environment is presented in Fig.5.

IV. Simulation Results

Once the filter is sized, CAIRO+ can generate the netlist file, which can be simulated. Simulations results are presented in the following.

A. Quality factor and resonance frequency

In table I, the calculated transistors dimensions and the values of the resonator capacitors are listed, for a resonance frequency of 2.442 GHz and different quality factors (Q=30, 60, 80). Table II shown the comparison between the performances calculated by CAIRO+ and the simulation results. In Fig.7, simulation results of the impedance versus input frequency are presented. Effective Q and resonance frequency can be extracted from Fig. 7. The parameters of the inductance are: 5 nH inductor (4 turns, 12 μm width and 10 μm spacing, which give a $Q_0 = 15$) for a 130 nm technology. The bias conditions are : V_{dd} = 0.9 V, V_{bias} = 0.3 V. As we can see, the automatic design procedure is precise for the effective quality factor and the resonance frequency.

B. Linearity

Using this systematic design procedure it is easily possible to study the importance of the input bias voltage on the linearity of the filter. Several filters with different input bias voltages have been designed. Their linearities can be measured from the output versus input power graphs (V_{bias} is set to 0.3V). In Fig. 8 we show the intermodulation distortion (IM3) with a two-tone signal. Its also possible to measure the third-order intercept point (IP3) of each filter.

C. Process Variations

The center frequency f_0 of a Q-enhanced LC resonator is a function of the inductance, of the capacitance of the spiral inductor, number of turns and connected circuitry. The inductance value is defined by inductor dimensions and is

TABLE I
TRANSISTORS DIMENSIONS AND CAPACITOR VALUE CALCULATED BY CAIRO+ FOR A 130 nm TECHNOLOGY

Q	C_{P_C} (pF)	$M_1/M_2(W/L)_{\mu m}$	$M_3(W/L)_{\mu m}$
30	1.519	1.21/0.13	39.5/0.13
60	1.518	1.93/0.13	60.4/0.13
80	1.517	2.10/0.13	65.8/0.13

TABLE II
COMPARISON BETWEEN CAIRO+ AND SIMULATION RESULTS.

CAIRO			Simulation		
f_0 (GHz)	Q	P_n (dBm)	f_0 (GHz)	Q	P_n (dBm)
2.442	30	-71.07	2.4422	30.15	-71.50
2.442	60	-66.17	2.4404	60.29	-66.53
2.442	80	-64.72	2.4401	79.10	-64.97
2.442	100	-63.63	2.4397	99.33	-63.77

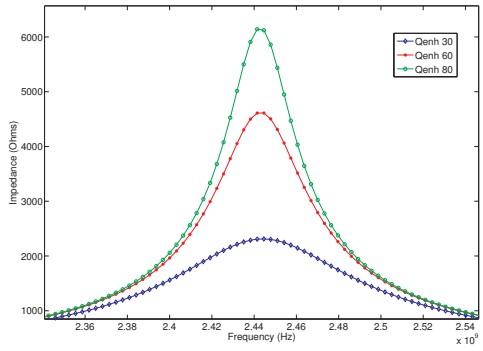

Fig. 7. Total impedance for different values of Q (Simulation results).

relatively unaffected by process variations. On other hand, the parasitics capacitances has a considerable variation. Since for RLC circuits the sensitivity of the center frequency, f_0, to the total capacitance is -0.5 [10], i.e., for a $\pm 10\%$ in capacitance variation this implies in a $\pm 5\%$ in central frequency shift.

Effects of the process variations on Q_{enh} are generally more severe than those for f_0 [9], so to identify these effects the sensitivity of Q_{enh} to G_{m_0} was analysed. Following the analysis presented in [10], the mathematical definition of circuit sensitivity is:

$$S_x^y = \lim_{\Delta x \to 0} \left\{ \frac{\frac{\Delta y}{y}}{\frac{\Delta x}{x}} \right\} = \frac{x}{y} \frac{\partial y}{\partial x}. \qquad (9)$$

Using (1) and (3), we get

$$S_{G_{m_0}}^{Q_{enh}} = \frac{Q_{enh}}{Q_0} - 1 = \frac{1}{1 - G_{m_0} R_p} - 1 \qquad (10)$$

from Eq.10 we can see the high sensitivity of the quality factor to the process variation for a large Q_{enh}, for example, for a Q_{enh} of 80, a Q_0 of 15 and considering a Gm_0 variation of 2%, we have a $\pm 8.6\%$ of variation for Q_{enh}. Following this analysis it is clear that it is necessary to use tuning circuits for the quality factor, Q_{enh}, and the center frequency, f_0 [11].

V. CONCLUSION

In this paper, we have presented a systematic design procedure for Q-enhanced LC filters using the analog design environment CAIRO+. The procedure is based upon the inductor π-model and the BSIM3v3 transistor's model. Several design examples have been presented to demonstrate the validity of the approach. Very little difference has been observed between

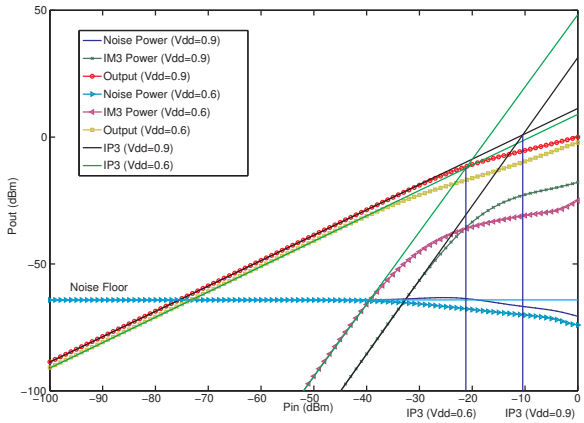

Fig. 8. Input output power of fundamental, output noise floor and IM3 versus Input power for different values of inductor biasing voltage, V_{dd} (Simulation results)(Fig. 1).

the estimated performances of the circuits generated using the proposed design procedure and the performances measured from simulation.

REFERENCES

[1] D. Li and Y. Tsividis, "Active LC filters on silicon",*IEE Proceedings on Circuits, Devices and Systems*, Vol 147, p 49-56, No.1, February 2000.

[2] S. Li, N. Stanić, K. Soumyanath and Y. Tsividis, "An Integrated 1.5V 6 GHz Q-enhanced LC CMOS Filter with Automatic Quality Factor Tuning using Conductance Reference",Radio Frequency Integrated Circuits Symposium, RFIC'05, Vol 147, p 49-56, No.1, February 2000.

[3] N. Beilleau, H. Aboushady, F. Montaudon and A. Cathelin, "A 1.3V 26mW 3.2GS/s Undersampled LC Bandpass Sigma-Delta ADC for a SDR ISM-band Receiver in 130nm CMOS", IEEE Radio Frequency Integrated Circuits Symposium, RFIC'09, Boston M.A., U.S.A, June 2009.

[4] Thandri, B. K.; Silva-Martinez, J., "A 63 dB SNR, 75-mW Bandpass RF $\Sigma\Delta$ ADC at 950 MHz Using 3.8-GHz Clock in 0.25-m SiGe BiCMOS Technology", IEEE Journal of Solid-State Circuits, Volume: 42, Issue: 2, pp. 269-279, February 2007.

[5] R. Iskander, L. de Lamarre, A. Kaiser and M.M. Louërat, "Design Space Exploration for Analog IPs using CAIRO+",*IEEE International Conference on Electrical Electronic and Computer Engineering*, ICEEC'04, p 473-476, Cairo, Egypt, September 2004.

[6] H. Ronkainen, H. Kattelus, E. Tarvainen, T. Ruhisaari, M. Andersson, P. Kuivalainen, "IC compatible planar inductors on silicon" Circuits, Devices and Systems, IEE Proceedings -. 01/03/199703/1997; 144(1):29-35. ISSN: 1350-2409.

[7] I. J. Bahl, Lumped Elements for RF and Microwave Circuits. Artech House, 2003

[8] Duncan, R. and Martin, K.W. and Sedra, A.S., "A Q-enhanced active-RLC bandpass filter", "Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on",vol.44, no.5, pp 1057-7130, May 1997

[9] W. B Kuhn, Dan Nobbe, D. Kelly and A. W. Osborn : "Dynamic Range performance of On-chip RF bandpass filter", *IEEE Transaction on circuit and system*, Vol. 50 , 10 October 2003, p 685-694.

[10] M. Fortunato, Circuit Sensitivity: With Emphasis on Analog Filters, Texas Instruments Developer Conf. 2007

[11] Li, D.; Tsividis, Y., "Design techniques for automatically tuned integrated gigahertz-range active LC filters," Solid-State Circuits, IEEE Journal of , vol.37, no.8, pp. 967-977, Aug 2002